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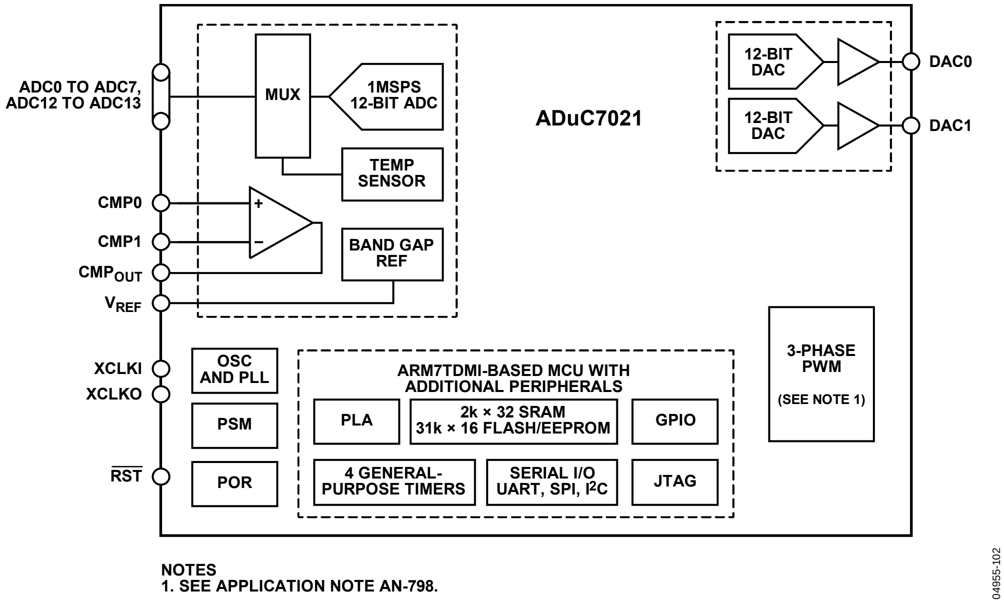
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

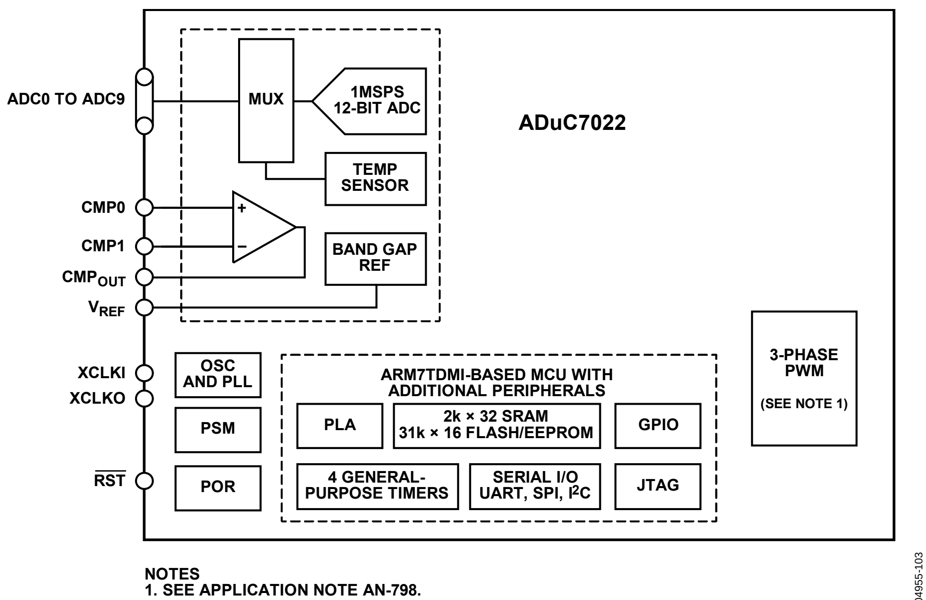
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12 x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7026bstz62i-rl



NOTES
1. SEE APPLICATION NOTE AN-798.

Figure 3.



NOTES
1. SEE APPLICATION NOTE AN-798.

Figure 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MCU CLOCK RATE					
From 32 kHz Internal Oscillator		326		kHz	CD[12] = 7
From 32 kHz External Crystal		41.78		MHz	CD[12] = 0
Using an External Clock	0.05		44	MHz	T_A = 85°C
	0.05		41.78	MHz	T_A = 125°C
START-UP TIME					Core clock = 41.78 MHz
At Power-On		130		ms	
From Pause/Nap Mode		24		ns	CD[12] = 0
		3.06		µs	CD[12] = 7
From Sleep Mode		1.58		ms	
From Stop Mode		1.7		ms	
PROGRAMMABLE LOGIC ARRAY (PLA)					
Pin Propagation Delay		12		ns	From input pin to output pin
Element Propagation Delay		2.5		ns	
POWER REQUIREMENTS[13, 14]					
Power Supply Voltage Range					
AV_{DD} to AGND and IOV_{DD} to IOGND	2.7		3.6	V	
Analog Power Supply Currents					
AV_{DD} Current		200		µA	ADC in idle mode; all parts except ADuC7019
		400		µA	ADC in idle mode; ADuC7019 only
$DACV_{DD}$ Current[15]		3	25	µA	
Digital Power Supply Current					
IOV_{DD} Current in Normal Mode					Code executing from Flash/EE
		7	10	mA	CD[12] = 7
		11	15	mA	CD[12] = 3
		40	45	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode		25	30	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode		250	400	µA	T_A = 85°C
		600	1000	µA	T_A = 125°C
Additional Power Supply Currents					
ADC		2		mA	@ 1 MSPS
		0.7		mA	@ 62.5 kSPS
DAC		700		µA	per DAC
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			4	kV	
FCIDM Passed Up To			0.5	kV	

[1] All ADC channel specifications are guaranteed during normal MicroConverter core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 59. Based on external ADC system components; the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22m, Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] See the POWCON register.
[13] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[14] IOV_{DD} power supply current decreases typically by 2 mA during a Flash/EE erase cycle.
[15] On the ADuC7019/20/21/22, this current must be added to the AV_{DD} current.

Table 4. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Slave Min	Slave Max	Master Typ	Unit
t_L	SCL low pulse width[1]	200		1360	ns
t_H	SCL high pulse width[1]	100		1140	ns
t_{SHD}	Start condition hold time	300			ns
t_{DSU}	Data setup time	100		740	ns
t_{DHD}	Data hold time	0		400	ns
t_{RSU}	Setup time for repeated start	100			ns
t_{PSU}	Stop condition setup time	100		400	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCL and SDA		300	200	ns
t_F	Fall time for both SCL and SDA		300		ns
t_{SUP}	Pulse width of spike suppressed		50		ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

Table 5. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Slave Min	Slave Max	Master Typ	Unit
t_L	SCL low pulse width[1]	4.7			µs
t_H	SCL high pulse width[1]	4.0			ns
t_{SHD}	Start condition hold time	4.0			µs
t_{DSU}	Data setup time	250			ns
t_{DHD}	Data hold time	0	3.45		µs
t_{RSU}	Setup time for repeated start	4.7			µs
t_{PSU}	Stop condition setup time	4.0			µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7			µs
t_R	Rise time for both SCL and SDA		1		µs
t_F	Fall time for both SCL and SDA		300		ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

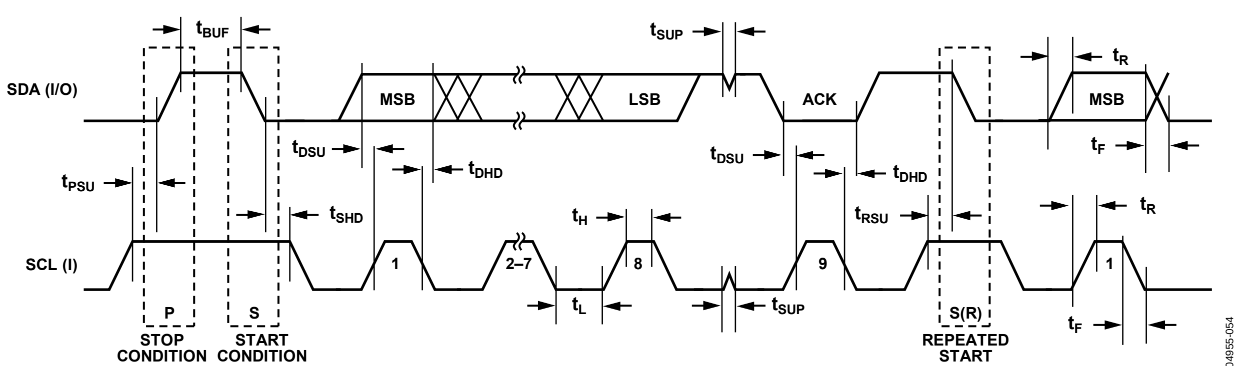


Figure 14. I²C Compatible Interface Timing

Table 9. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			25	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.
[2] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

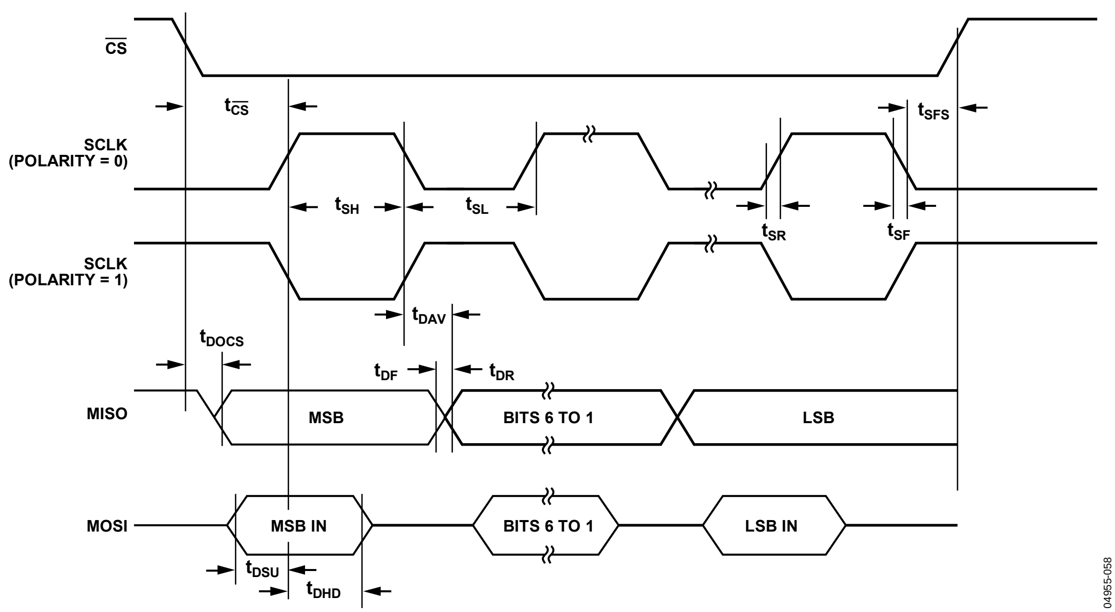


Figure 18. SPI Slave Mode Timing (Phase Mode = 0)

ADuC7024/ADuC7025

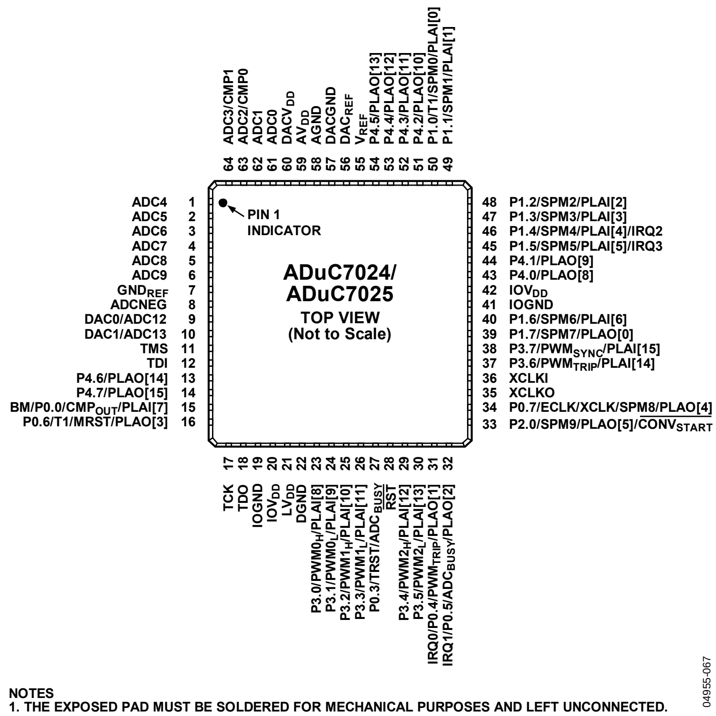


Figure 23. 64-Lead LFCSP_VQ Pin Configuration (ADuC7024/ADuC7025)

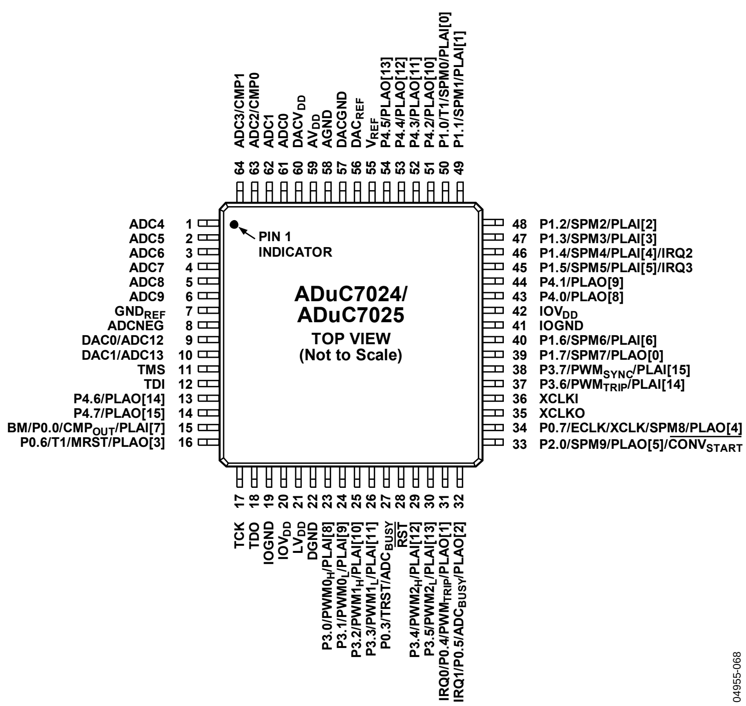


Figure 24. 64-Lead LQFP Pin Configuration (ADuC7024/ADuC7025)

Pin No.	Mnemonic	Description
37	P3.6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
38	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization Input and Output/ Programmable Logic Array Input Element 15.
39	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
40	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
41	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
42	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
43	P4.0/PLAO[8]	General-Purpose Input and Output Port 4.0/Programmable Logic Array Output Element 8.
44	P4.1/PLAO[9]	General-Purpose Input and Output Port 4.1/Programmable Logic Array Output Element 9.
45	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
46	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
47	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
48	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
49	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
50	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
51	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
52	P4.3/PLAO[11]	General-Purpose Input and Output Port 4.3/Programmable Logic Array Output Element 11.
53	P4.4/PLAO[12]	General-Purpose Input and Output Port 4.4/Programmable Logic Array Output Element 12.
54	P4.5/PLAO[13]	General-Purpose Input and Output Port 4.5/Programmable Logic Array Output Element 13.
55	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
56	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
57	DACGND	Ground for the DAC. Typically connected to AGND.
58	AGND	Analog Ground. Ground reference point for the analog circuitry.
59	AV_{DD}	3.3 V Analog Power.
60	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
61	ADC0	Single-Ended or Differential Analog Input 0.
62	ADC1	Single-Ended or Differential Analog Input 1.
63	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
64	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
0	EP	Exposed Pad. The pin configuration for the ADuC7024/ADuC7025 LFCSP_VQ has an exposed pad that must be soldered for mechanical purposes and left unconnected.

ADUC7028

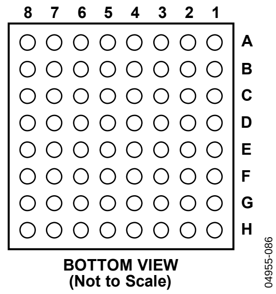


Figure 26. 64-Ball CSP_BGA Pin Configuration (ADuC7028)

Table 14. Pin Function Descriptions (ADuC7028)

Pin No.	Mnemonic	Description
A1	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
A2	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
A3	AV_{DD}	3.3 V Analog Power.
A4	AGND	Analog Ground. Ground reference point for the analog circuitry.
A5	DACGND	Ground for the DAC. Typically connected to AGND.
A6	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
A7	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
A8	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
B1	ADC4	Single-Ended or Differential Analog Input 4.
B2	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
B3	ADC1	Single-Ended or Differential Analog Input 1.
B4	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
B5	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
B6	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0.
B7	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
B8	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
C1	ADC6	Single-Ended or Differential Analog Input 6.
C2	ADC5	Single-Ended or Differential Analog Input 5.
C3	ADC0	Single-Ended or Differential Analog Input 0.
C4	P4.5/PLAO[13]	General-Purpose Input and Output Port 4.5/Programmable Logic Array Output Element 13.
C5	P4.3/PLAO[11]	General-Purpose Input and Output Port 4.3/Programmable Logic Array Output Element 11.
C6	P4.0/PLAO[8]	General-Purpose Input and Output Port 4.0/Programmable Logic Array Output Element 8.
C7	P4.1/PLAO[9]	General-Purpose Input and Output Port 4.1/Programmable Logic Array Output Element 9.
C8	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
D1	ADCNEG	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
D2	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
D3	ADC7	Single-Ended or Differential Analog Input 7.
D4	P4.4/PLAO[12]	General-Purpose Input and Output Port 4.4/Programmable Logic Array Output Element 12.
D5	P3.6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
D6	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.

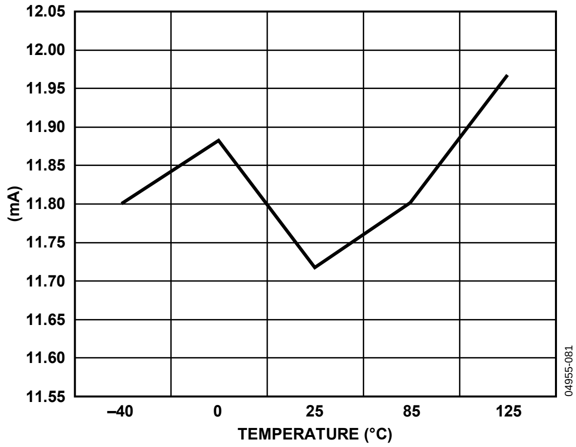


Figure 40. Current Consumption vs. Temperature @ CD = 3

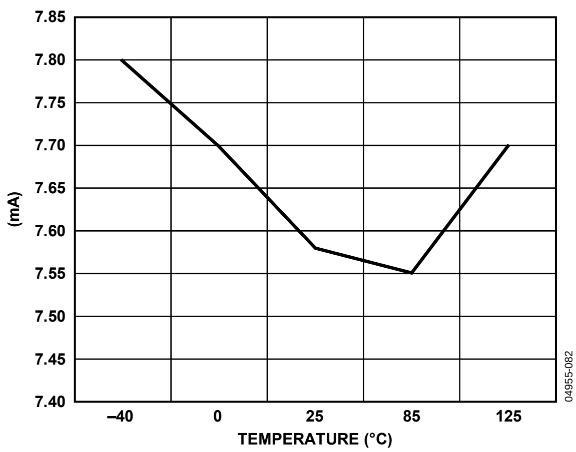


Figure 41. Current Consumption vs. Temperature @ CD = 7

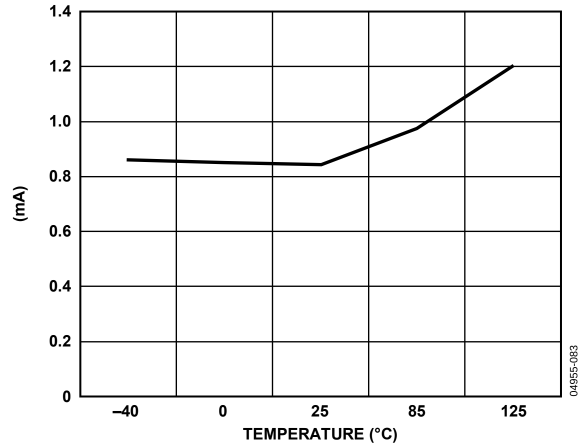


Figure 42. Current Consumption vs. Temperature in Sleep Mode

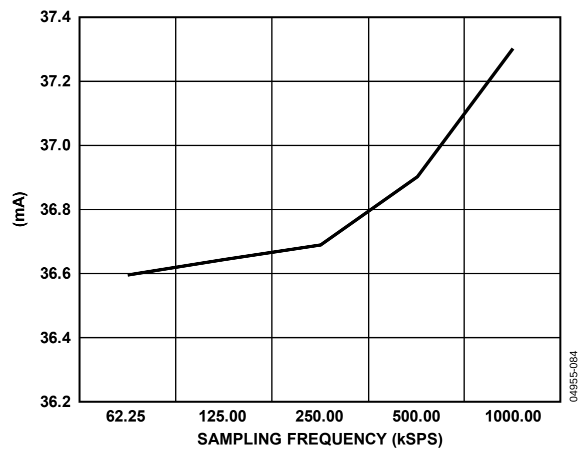


Figure 43. Current Consumption vs. Sampling Frequency

MEMORY ORGANIZATION

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate two separate blocks of memory: 8 kB of SRAM and 64 kB of on-chip Flash/EE memory. The 62 kB of on-chip Flash/EE memory is available to the user, and the remaining 2 kB are reserved for the factory-configured boot page. These two blocks are mapped as shown in Figure 45.

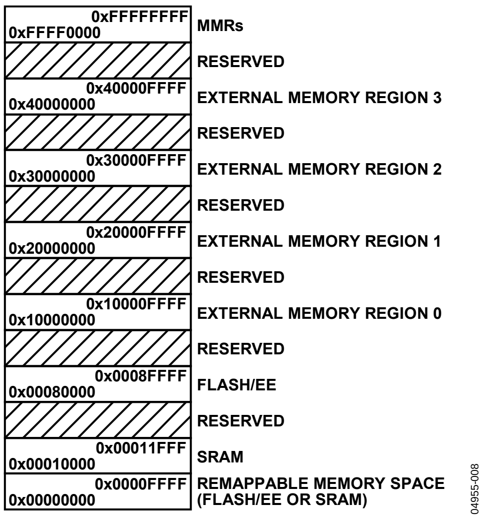


Figure 45. Physical Memory Map

Note that by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE Memory section.

MEMORY ACCESS

The ARM7 core sees memory as a linear array of a 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 45.

The ADuC7019/20/21/22/24/25/26/27/28/29 memory organizations are configured in little endian format, which means that the least significant byte is located in the lowest byte address, and the most significant byte is in the highest byte address.

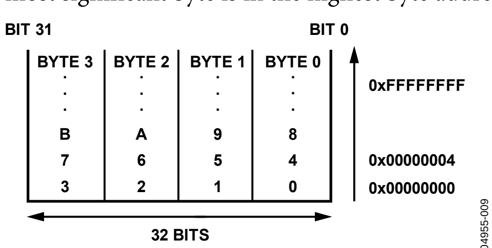


Figure 46. Little Endian Format

FLASH/EE MEMORY

The total 64 kB of Flash/EE memory is organized as 32 k × 16 bits; 31 k × 16 bits is user space and 1 k × 16 bits is reserved for the on-chip kernel. The page size of this Flash/EE memory is 512 bytes.

Sixty-two kilobytes of Flash/EE memory are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, which means that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. It is therefore recommended to use thumb mode when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in thumb mode and 20.89 MHz in full ARM mode. More details about Flash/EE access time are outlined in the Execution Time from SRAM and Flash/EE section.

SRAM

Eight kilobytes of SRAM are available to the user, organized as 2 k × 32 bits, that is, two words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array. More details about SRAM access time are outlined in the Execution Time from SRAM and Flash/EE section.

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 47 are unoccupied or reserved locations and should not be accessed by user software. Table 16 shows the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules and the advanced peripheral bus (APB) used for lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7019/20/21/22/24/25/26/27/28/29 are on the APB except the Flash/EE memory, the GPIOs (see Table 78), and the PWM.

ADC CIRCUIT OVERVIEW

The analog-to-digital converter (ADC) incorporates a fast, multichannel, 12-bit ADC. It can operate from 2.7 V to 3.6 V supplies and is capable of providing a throughput of up to 1 MSPS when the clock source is 41.78 MHz. This block provides the user with a multichannel multiplexer, a differential track-and-hold, an on-chip reference, and an ADC.

The ADC consists of a 12-bit successive approximation converter based around two capacitor DACs. Depending on the input signal configuration, the ADC can operate in one of three modes.

- Fully differential mode, for small and balanced signals
- Single-ended mode, for any single-ended signals
- Pseudo differential mode, for any single-ended signals, taking advantage of the common-mode rejection offered by the pseudo differential input

The converter accepts an analog input range of 0 V to V_{REF} when operating in single-ended or pseudo differential mode. In fully differential mode, the input signal must be balanced around a common-mode voltage (V_{CM}) in the 0 V to AV_{DD} range with a maximum amplitude of 2 V_{REF} (see Figure 48).

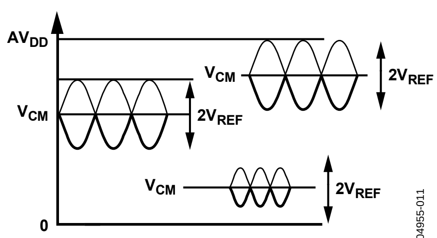


Figure 48. Examples of Balanced Signals in Fully Differential Mode

A high precision, low drift, factory calibrated, 2.5 V reference is provided on-chip. An external reference can also be connected as described in the Band Gap Reference section.

Single or continuous conversion modes can be initiated in the software. An external $\overline{\text{CONV}_{\text{START}}}$ pin, an output generated from the on-chip PLA, or a Timer0 or Timer1 overflow can also be used to generate a repetitive trigger for ADC conversions.

A voltage output from an on-chip band gap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexer, effectively an additional ADC channel input. This facilitates an internal temperature sensor channel that measures die temperature to an accuracy of ±3°C.

TRANSFER FUNCTION

Pseudo Differential and Single-Ended Modes

In pseudo differential or single-ended mode, the input range is 0 V to V_{REF}. The output coding is straight binary in pseudo differential and single-ended modes with

1 LSB = *FS*/4096, or
2.5 V/4096 = 0.61 mV, or
610 µV when V_{REF} = 2.5 V

The ideal code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, … , FS – 3/2 LSB). The ideal input/output transfer characteristic is shown in Figure 49.

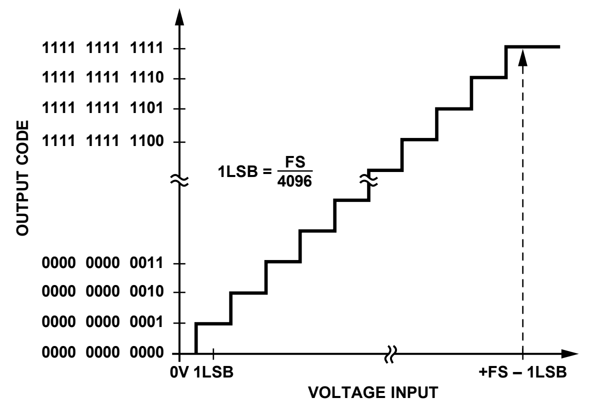


Figure 49. ADC Transfer Function in Pseudo Differential or Single-Ended Mode

Fully Differential Mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} input voltage pins (that is, $V_{IN+} - V_{IN-}$). The maximum amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ p-p (that is, 2 × V_{REF}). This is regardless of the common mode (CM). The common mode is the average of the two signals, for example, $(V_{IN+} + V_{IN-})/2$, and is, therefore, the voltage that the two inputs are centered on. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally, and its range varies with V_{REF} (see the Driving the Analog Inputs section).

The output coding is twos complement in fully differential mode with 1 LSB = 2 V_{REF}/4096 or 2 × 2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V. The output result is ±11 bits, but this is shifted by 1 to the right. This allows the result in ADCDAT to be declared as a signed integer when writing C code. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, … , FS – 3/2 LSB). The ideal input/output transfer characteristic is shown in Figure 50.

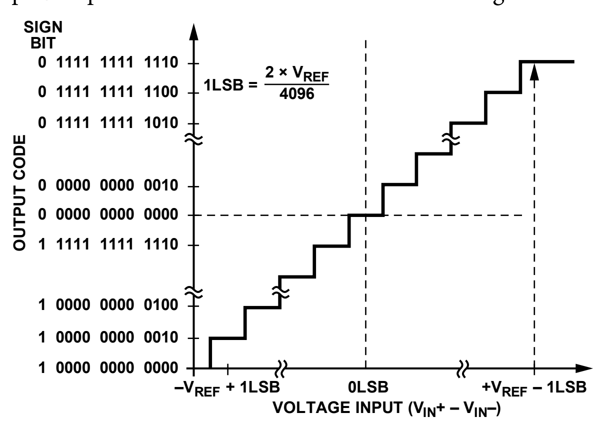


Figure 50. ADC Transfer Function in Differential Mode

Pseudo Differential Mode

In pseudo differential mode, Channel− is linked to the V_{IN-} pin of the ADuC7019/20/21/22/24/25/26/27/28/29. SW2 switches between A (Channel−) and B (V_{REF}). The V_{IN-} pin must be connected to ground or a low voltage. The input signal on V_{IN+} can then vary from V_{IN-} to V_{REF} + V_{IN-}. Note that V_{IN-} must be chosen so that V_{REF} + V_{IN-} does not exceed AV_{DD}.

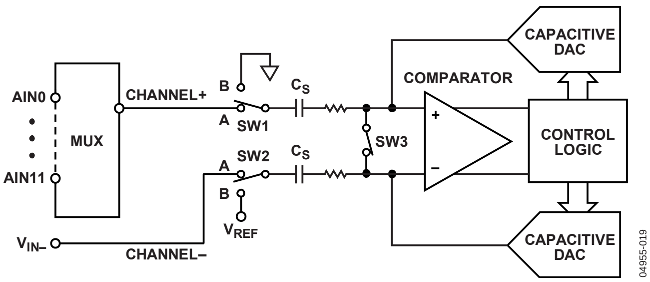


Figure 56. ADC in Pseudo Differential Mode

Single-Ended Mode

In single-ended mode, SW2 is always connected internally to ground. The V_{IN-} pin can be floating. The input signal range on V_{IN+} is 0 V to V_{REF}.

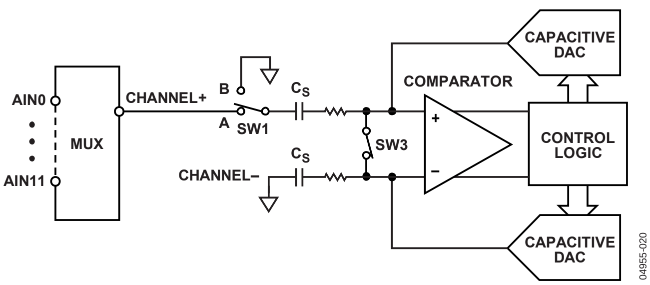


Figure 57. ADC in Single-Ended Mode

Analog Input Structure

Figure 58 shows the equivalent circuit of the analog input structure of the ADC. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV; exceeding 300 mV causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The C1 capacitors in Figure 58 are typically 4 pF and can be primarily attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC's sampling capacitors and typically have a capacitance of 16 pF.

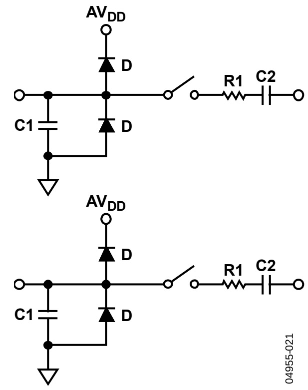


Figure 58. Equivalent Analog Input Circuit Conversion Phase: Switches Open, Track Phase: Switches Closed

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application. Figure 59 and Figure 60 give an example of an ADC front end.

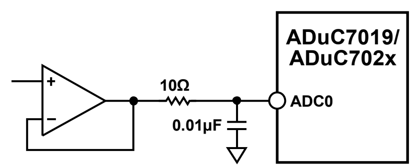


Figure 59. Buffering Single-Ended/Pseudo Differential Input

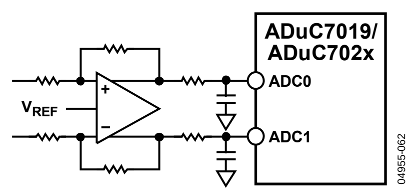


Figure 60. Buffering Differential Inputs

When no amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and the performance degrades.

DRIVING THE ANALOG INPUTS

Internal or external references can be used for the ADC. In the differential mode of operation, there are restrictions on the common-mode input signal (V_{CM}), which is dependent upon the reference value and supply voltage used to ensure that the signal remains within the supply rails. Table 28 gives some calculated V_{CM} minimum and V_{CM} maximum values.

EXECUTION TIME FROM SRAM AND FLASH/EE

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle; the access time of the SRAM is 2 ns, and a clock cycle is 22 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE): one cycle to execute the instruction, and two cycles to get the 32-bit data from Flash/EE. A control flow instruction (a branch instruction, for example) takes one cycle to fetch but also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 22 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD Bit = 0). Also, some dead times are needed before accessing data for any value of the CD bit.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline. A data-processing instruction involving only the core register does not require any extra clock cycles. However, if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data, and two cycles are needed to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 43.

Table 43. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD[1]	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N[2]	2 × N[2]	N[1]
STR[1]	2/1	1	2 × 20 ns	1
STRH	2/1	1	20 ns	1
STRM/POP	2/1	N[1]	2 × N × 20 ns[1]	N[1]

[1] The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles + 40 ns.
[2] N is the amount of data to load or store in the multiple load/store instruction (1 < N ≤ 16).

RESET AND REMAP

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020, as shown in Figure 62.

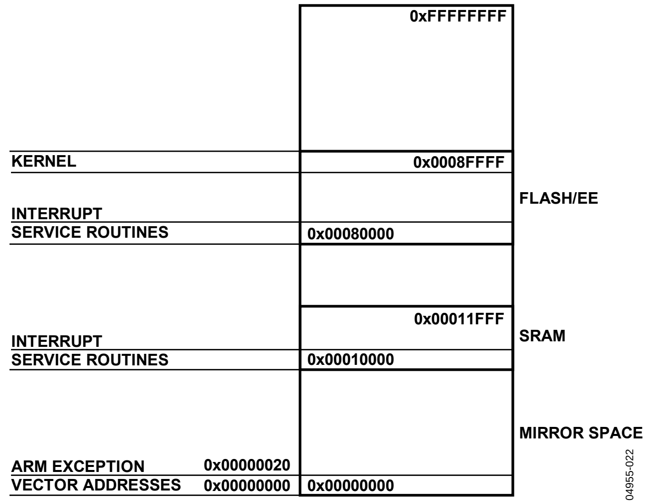


Figure 62. Remap for Exception Execution

By default, and after any reset, the Flash/EE is mirrored at the bottom of the memory array. The remap function allows the programmer to mirror the SRAM at the bottom of the memory array, which facilitates execution of exception routines from SRAM instead of from Flash/EE. This means exceptions are executed twice as fast, being executed in 32-bit ARM mode with 32-bit wide SRAM instead of 16-bit wide Flash/EE memory.

Remap Operation

When a reset occurs on the ADuC7019/20/21/22/24/25/26/27/28/29, execution automatically starts in the factory-programmed, internal configuration code. This kernel is hidden and cannot be accessed by user code. If the part is in normal mode (the BM pin is high), it executes the power-on configuration routine of the kernel and then jumps to the reset vector address, 0x00000000, to execute the user's reset exception routine.

Because the Flash/EE is mirrored at the bottom of the memory array at reset, the reset interrupt routine must always be written in Flash/EE.

The remap is done from Flash/EE by setting Bit 0 of the REMAP register. Caution must be taken to execute this command from Flash/EE, above Address 0x00080020, and not from the bottom of the array because this is replaced by the SRAM.

This operation is reversible. The Flash/EE can be remapped at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. Caution must again be taken to execute the remap function from outside the mirrored area. Any type of reset remaps the Flash/EE memory at the bottom of the array.

Both switching edges are moved by an equal amount ($PWMDAT1 \times t_{CORE}$) to preserve the symmetrical output patterns.

Also shown are the PWMSYNC pulse and Bit 0 of the PWMSTA register, which indicates whether operation is in the first or second half cycle of the PWM period.

The resulting on times of the PWM signals over the full PWM period (two half periods) produced by the timing unit can be written as follows:

On the high side

$$t_{0HH} = PWMDAT0 + 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

$$t_{0HL} = PWMDAT0 - 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (d)

$$d_{0H} = t_{0HH}/t_S = ½ + (PWMCH0 - PWMDAT1)/PWMDAT0$$

and on the low side

$$t_{0LH} = PWMDAT0 - 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

$$t_{0LL} = PWMDAT0 + 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (d)

$$d_{0L} = t_{0LH}/t_S = ½ - (PWMCH0 + PWMDAT1)/PWMDAT0$$

The minimum permissible t_{0H} and t_{0L} values are zero, corresponding to a 0% duty cycle. In a similar fashion, the maximum value is t_S, corresponding to a 100% duty cycle.

Figure 70 shows the output signals from the timing unit for operation in double update mode. It illustrates a general case where the switching frequency, dead time, and duty cycle are all changed in the second half of the PWM period. The same value for any or all of these quantities can be used in both halves of the PWM cycle. However, there is no guarantee that symmetrical PWM signals are produced by the timing unit in double update mode. Figure 70 also shows that the dead time insertions into the PWM signals are done in the same way as in single update mode.

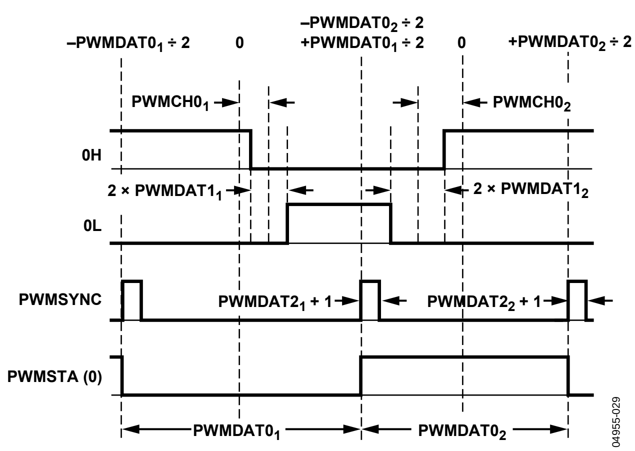


Figure 70. Typical PWM Outputs of the 3-Phase Timing Unit (Double Update Mode)

In general, the on times of the PWM signals in double update mode can be defined as follows:

On the high side

$$t_{0HH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

$$t_{0HL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (d) are

$$d_{0H} = t_{0HH}/t_S = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

On the low side

$$t_{0LH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

$$t_{0LL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (d) are

$$d_{0L} = t_{0LH}/t_S = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

For the completely general case in double update mode (see Figure 70), the switching period is given by

$$t_S = (PWMDAT0_1 + PWMDAT0_2) \times t_{CORE}$$

Again, the values of t_{0H} and t_{0L} are constrained to lie between zero and t_S.

PWM signals similar to those illustrated in Figure 69 and Figure 70 can be produced on the 1H, 1L, 2H, and 2L outputs by programming the PWMCH1 and PWMCH2 registers in a manner identical to that described for PWMCH0. The PWM controller does not produce any PWM outputs until all of the PWMDAT0, PWMCH0, PWMCH1, and PWMCH2 registers have been written to at least once. When these registers are written, internal counting of the timers in the 3-phase timing unit is enabled.

Writing to the PWMDAT0 register starts the internal timing of the main PWM timer. Provided that the PWMDAT0 register is written to prior to the PWMCH0, PWMCH1, and PWMCH2 registers in the initialization, the first PWMSYNC pulse and interrupt (if enabled) appear $1.5 \times t_{CORE} \times PWMDAT0$ seconds after the initial write to the PWMDAT0 register in single update mode. In double update mode, the first PWMSYNC pulse appears after $PWMDAT0 \times t_{CORE}$ seconds.

The GDCLK value can range from 0 to 255, corresponding to a programmable chopping frequency rate of 40.8 kHz to 10.44 MHz for a 41.78 MHz core frequency. The gate drive features must be programmed before operation of the PWM controller and are typically not changed during normal operation of the PWM controller. Following a reset, all bits of the PWMCFG register are cleared so that high frequency chopping is disabled, by default.

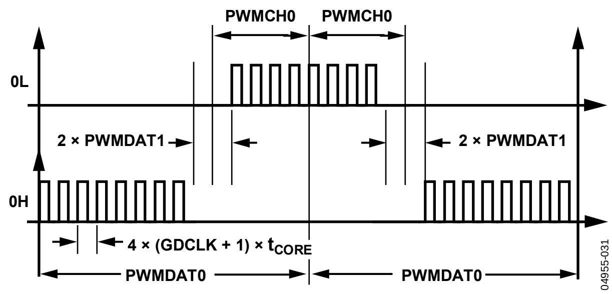


Figure 72. Typical PWM Signals with High Frequency Gate Chopping Enabled on Both High-Side and Low-Side Switches

PWM Shutdown

In the event of external fault conditions, it is essential that the PWM system be instantaneously shut down in a safe fashion. A low level on the PWM_{TRIP} pin provides an instantaneous, asynchronous (independent of the MicroConverter core clock) shutdown of the PWM controller. All six PWM outputs are placed in the off state, that is, in low state. In addition, the PWMSYNC pulse is disabled. The PWM_{TRIP} pin has an internal pull-down resistor to disable the PWM if the pin becomes disconnected. The state of the PWM_{TRIP} pin can be read from Bit 3 of the PWMSTA register.

If a PWM shutdown command occurs, a PWMTRIP interrupt is generated, and internal timing of the 3-phase timing unit of the PWM controller is stopped. Following a PWM shutdown, the PWM can be reenabled (in a PWMTRIP interrupt service routine, for example) only by writing to all of the PWMDAT0, PWMCH0, PWMCH1, and PWMCH2 registers. Provided that the external fault is cleared and the PWMTRIP is returned to a high level, the internal timing of the 3-phase timing unit resumes, and new duty-cycle values are latched on the next PWMSYNC boundary.

Note that the PWMTRIP interrupt is available in IRQ only, and the PWMSYNC interrupt is available in FIQ only. Both interrupts share the same bit in the interrupt controller. Therefore, only one of the interrupts can be used at a time. See the Interrupt System section for further details.

PWM MMRs Interface

The PWM block is controlled via the MMRs described in this section.

Table 66. PWMCON Register

Name	Address	Default Value	Access
PWMCON	0xFFFFFC00	0x0000	R/W

PWMCON is a control register that enables the PWM and chooses the update rate.

Table 67. PWMCON MMR Bit Descriptions

Bit	Name	Description
7:5		Reserved.
4	PWM_SYNCSEL	External sync select. Set to use external sync. Cleared to use internal sync.
3	PWM_EXTSYNC	External sync select. Set to select external synchronous sync signal. Cleared for asynchronous sync signal.
2	PWMDBL	Double update mode. Set to 1 by user to enable double update mode. Cleared to 0 by the user to enable single update mode.
1	PWM_SYNC_EN	PWM synchronization enable. Set by user to enable synchronization. Cleared by user to disable synchronization.
0	PWMEN	PWM enable bit. Set to 1 by user to enable the PWM. Cleared to 0 by user to disable the PWM. Also cleared automatically with PWMTRIP (PWMSTA MMR).

Table 68. PWMSTA Register

Name	Address	Default Value	Access
PWMSTA	0xFFFFFC04	0x0000	R/W

PWMSTA reflects the status of the PWM.

Table 69. PWMSTA MMR Bit Descriptions

Bit	Name	Description
15:10		Reserved.
9	PWMSYNCINT	PWM sync interrupt bit. Writing a 1 to this bit clears this interrupt.
8	PWMTRIPINT	PWM trip interrupt bit. Writing a 1 to this bit clears this interrupt.
3	PWMTRIP	Raw signal from the PWM_{TRIP} pin.
2:1		Reserved.
0	PWMPHASE	PWM phase bit. Set to 1 by the MicroConverter when the timer is counting down (first half). Cleared to 0 by the MicroConverter when the timer is counting up (second half).

Table 83. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

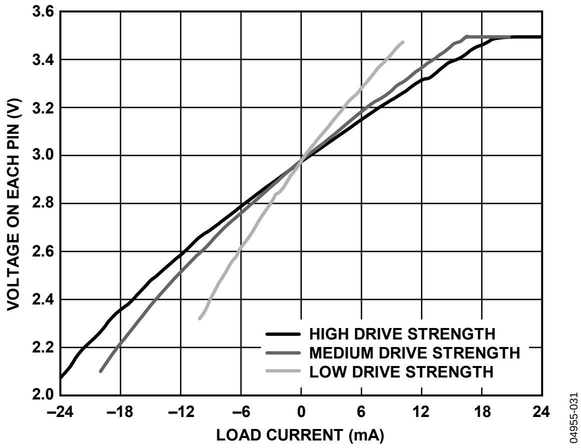


Figure 73. Programmable Strength for High Level (Typical Values)

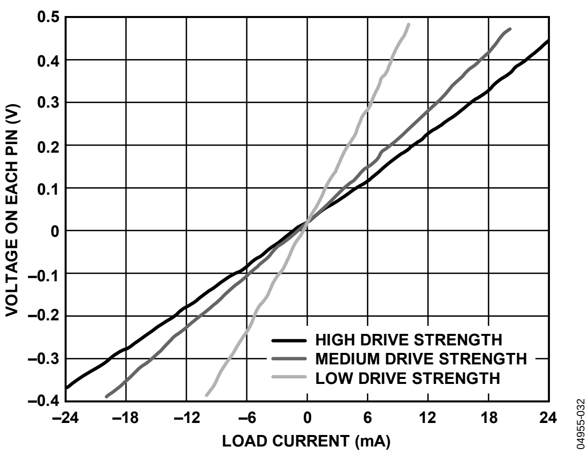


Figure 74. Programmable Strength for Low Level (Typical Values)

The drive strength bits can be written to one time only after reset. More writing to related bits has no effect on changing drive strength. The GPIO drive strength and pull-up disable is not always adjustable for the GPIO port. Some control bits cannot be changed (see Table 84).

Table 84. GPxPAR Control Bits Access Descriptions

Bit	GP0PAR	GP1PAR
31	Reserved	Reserved
30 to 29	R/W	R/W
28	R/W	R/W
27	Reserved	Reserved
26 to 25	R/W	R/W
24	R/W	R/W
23	Reserved	Reserved
22 to 21	R/W	R (b00)
20	R/W	R/W
19	Reserved	Reserved
18 to 17	R (b00)	R (b00)
16	R/W	R/W
15	Reserved	Reserved
14 to 13	R (b00)	R (b00)
12	R/W	R/W
11	Reserved	Reserved
10 to 9	R (b00)	R (b00)
8	R/W	R/W
7	Reserved	Reserved
6 to 5	R (b00)	R (b00)
4	R/W	R/W
3	Reserved	Reserved
2 to 1	R (b00)	R (b00)
0	R/W	R/W

SPI Registers

The following MMR registers are used to control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

Table 119. SPISTA Register

Name	Address	Default Value	Access
SPISTA	0xFFFF0A00	0x00	R

SPISTA is an 8-bit read-only status register. Only Bit 1 or Bit 4 of this register generates an interrupt. Bit 6 of the SPICON register determines which bit generates the interrupt.

Table 120. SPISTA MMR Bit Descriptions

Bit	Description
7:6	Reserved.
5	SPIRX data register overflow status bit. Set if SPIRX is overflowing. Cleared by reading the SPIRX register.
4	SPIRX data register IRQ. Set automatically if Bit 3 or Bit 5 is set. Cleared by reading the SPIRX register.
3	SPIRX data register full status bit. Set automatically if a valid data is present in the SPIRX register. Cleared by reading the SPIRX register.
2	SPITX data register underflow status bit. Set automatically if SPITX is underflowing. Cleared by writing in the SPITX register.
1	SPITX data register IRQ. Set automatically if Bit 0 is clear or Bit 2 is set. Cleared by writing in the SPITX register or if finished transmission disabling the SPI.
0	SPITX data register empty status bit. Set by writing to SPITX to send data. This bit is set during transmission of data. Cleared when SPITX is empty.

Table 121. SPIRX Register

Name	Address	Default Value	Access
SPIRX	0xFFFF0A04	0x00	R

SPIRX is an 8-bit, read-only receive register.

Table 122. SPITX Register

Name	Address	Default Value	Access
SPITX	0xFFFF0A08	0x00	W

SPITX is an 8-bit, write-only transmit register.

Table 123. SPIDIV Register

Name	Address	Default Value	Access
SPIDIV	0xFFFF0A0C	0x1B	R/W

SPIDIV is an 8-bit, serial clock divider register.

Table 124. SPICON Register

Name	Address	Default Value	Access
SPICON	0xFFFF0A10	0x0000	R/W

SPICON is a 16-bit control register.

Table 125. SPICON MMR Bit Descriptions

Bit	Description	Function
15:13	Reserved	N/A
12	Continuous transfer enable	Set by user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the TX register. $\overline{CS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until TX is empty. Cleared by user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period.
11	Loop back enable	Set by user to connect MISO to MOSI and test software. Cleared by user to be in normal mode.
10	Slave MISO output enable	Set this bit to disable the output driver on the MISO pin. The MISO pin becomes open drain when this bit is set. Clear this bit for MISO to operate as normal.
9	Clip select output enable	Set by user in master mode to disable the chip select output. cleared by user to enable the chip select output. P1.7 should be configured as $\overline{CS}$ before SPICON is configured as a master when the chip select output enabled is also selected.
8	SPIRX overflow overwrite enable	Set by user, the valid data in the RX register is overwritten by the new serial byte received. Cleared by user, the new serial byte received is discarded.
7	SPITX underflow mode	Set by user to transmit 0. Cleared by user to transmit the previous data.
6	Transfer and interrupt mode	Set by user to initiate transfer with a write to the SPITX register. Interrupt occurs only when TX is empty. Cleared by user to initiate transfer with a read of the SPIRX register. Interrupt occurs only when RX is full.
5	LSB first transfer enable bit	Set by user, the LSB is transmitted first. Cleared by user, the MSB is transmitted first.
4	Reserved	
3	Serial clock polarity mode bit	Set by user, the serial clock idles high. Cleared by user, the serial clock idles low.
2	Serial clock phase mode bit	Set by user, the serial clock pulses at the beginning of each serial bit transfer. Cleared by user, the serial clock pulses at the end of each serial bit transfer.
1	Master mode enable bit	Set by user to enable master mode. Cleared by user to enable slave mode.
0	SPI enable bit	Set by user to enable the SPI. Cleared by user to disable the SPI.

Table 129. I2C0SSTA MMR Bit Descriptions

Bit	Value	Description
31:15		Reserved. These bits should be written as 0.
14		Start decode bit. Set by hardware if the device receives a valid start plus matching address. Cleared by an I²C stop condition or an I²C general call reset.
13		Repeated start decode bit. Set by hardware if the device receives a valid repeated start and matching address. Cleared by an I²C stop condition, a read of the I2CSSTA register, or an I²C general call reset.
12:11		ID decode bits.
	00	Received Address Matched ID Register 0.
	01	Received Address Matched ID Register 1.
	10	Received Address Matched ID Register 2.
	11	Received Address Matched ID Register 3.
10		Stop after start and matching address interrupt. Set by hardware if the slave device receives an I²C stop condition after a previous I²C start condition and matching address. Cleared by a read of the I2C0SSTA register.
9:8		General call ID.
	00	No general call.
	01	General call reset and program address.
	10	General call program address.
	11	General call matching alternative ID.
7		General call interrupt. Set if the slave device receives a general call of any type. Cleared by setting Bit 8 of the I2CxCFG register. If it is a general call reset, all registers are at their default values. If it is a hardware general call, the Rx FIFO holds the second byte of the general call. This is similar to the I2C0ALT register (unless it is a general call to reprogram the device address). For more details, see the I²C bus specification, Version 2.1, January 2000.
6		Slave busy. Set automatically if the slave is busy. Cleared automatically.
5		No ACK. Set if master asking for data and no data is available. Cleared automatically by reading the I2C0SSTA register.
4		Slave receive FIFO overflow. Set automatically if the slave receive FIFO is overflowing. Cleared automatically by reading the I2C0SSTA register.
3		Slave receive IRQ. Set after receiving data. Cleared automatically by reading the I2C0SRX register or flushing the FIFO.
2		Slave transmit IRQ. Set at the end of a transmission. Cleared automatically by writing to the I2C0STX register.
1		Slave transmit FIFO underflow. Set automatically if the slave transmit FIFO is underflowing. Cleared automatically by writing to the I2C0SSTA register.
0		Slave transmit FIFO not full. Set automatically if the slave transmit FIFO is not full. Cleared automatically by writing twice to the I2C0STX register.

Table 130. I2CxSRX Registers

Name	Address	Default Value	Access
I2C0SRX	0xFFFF0808	0x00	R
I2C1SRX	0xFFFF0908	0x00	R

I2CxSRX are receive registers for the slave channel.

Table 131. I2CxSTX Registers

Name	Address	Default Value	Access
I2C0STX	0xFFFF080C	0x00	W
I2C1STX	0xFFFF090C	0x00	W

I2CxSTX are transmit registers for the slave channel.

Table 132. I2CxMRX Registers

Name	Address	Default Value	Access
I2C0MRX	0xFFFF0810	0x00	R
I2C1MRX	0xFFFF0910	0x00	R

I2CxMRX are receive registers for the master channel.

Table 133. I2CxMTX Registers

Name	Address	Default Value	Access
I2C0MTX	0xFFFF0814	0x00	W
I2C1MTX	0xFFFF0914	0x00	W

I2CxMTX are transmit registers for the master channel.

Table 134. I2CxCNT Registers

Name	Address	Default Value	Access
I2C0CNT	0xFFFF0818	0x00	R/W
I2C1CNT	0xFFFF0918	0x00	R/W

I2CxCNT are 3-bit, master receive, data count registers. If a master read transfer sequence is initiated, the I2CxCNT registers denote the number of bytes (−1) to be read from the slave device. By default, this counter is 0, which corresponds to the one byte expected.

Table 135. I2CxADR Registers

Name	Address	Default Value	Access
I2C0ADR	0xFFFF081C	0x00	R/W
I2C1ADR	0xFFFF091C	0x00	R/W

I2CxADR are master address byte registers. The I2CxADR value is the device address that the master wants to communicate with. It automatically transmits at the start of a master transfer sequence if there is no valid data in the I2CxMTX register when the master enable bit is set.

Table 136. I2CxBYTE Registers

Name	Address	Default Value	Access
I2C0BYTE	0xFFFF0824	0x00	R/W
I2C1BYTE	0xFFFF0924	0x00	R/W

I2CxBYTE are broadcast byte registers. Data written to these registers does not go through the TxFIFO. This data is transmitted at the start of a transfer sequence before the address. After the byte is transmitted and acknowledged, the I²C expects another byte written in I2CxBYTE or an address written to the address register.

PROGRAMMABLE LOGIC ARRAY (PLA)

Every ADuC7019/20/21/22/24/25/26/27/28/29 integrates a fully programmable logic array (PLA) that consists of two independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving each part a total of 16 PLA elements.

Each PLA element contains a two-input lookup table that can be configured to generate any logic output function based on two inputs and a flip-flop. This is represented in Figure 76.

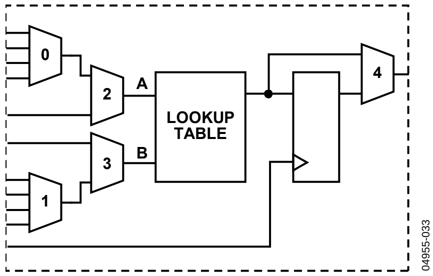


Figure 76. PLA Element

In total, 30 GPIO pins are available on each ADuC7019/20/21/22/24/25/26/27/28/29 for the PLA. These include 16 input pins and 14 output pins, which msut be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins.

The PLA is configured via a set of user MMRs. The output(s) of the PLA can be routed to the internal interrupt system, to the $\overline{\text{CONV}_{\text{START}}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The two blocks can be interconnected as follows:

- Output of Element 15 (Block 1) can be fed back to Input 0 of Mux 0 of Element 0 (Block 0).
- Output of Element 7 (Block 0) can be fed back to the Input 0 of Mux 0 of Element 8 (Block 1).

Table 145. Element Input/Output

PLA Block 0			PLA Block 1		
Element	Input	Output	Element	Input	Output
0	P1.0	P1.7	8	P3.0	P4.0
1	P1.1	P0.4	9	P3.1	P4.1
2	P1.2	P0.5	10	P3.2	P4.2
3	P1.3	P0.6	11	P3.3	P4.3
4	P1.4	P0.7	12	P3.4	P4.4
5	P1.5	P2.0	13	P3.5	P4.5
6	P1.6	P2.1	14	P3.6	P4.6
7	P0.0	P2.2	15	P3.7	P4.7

PLA MMRs Interface

The PLA peripheral interface consists of the 22 MMRs described in this section.

Table 146. PLAELMx Registers

Name	Address	Default Value	Access
PLAELM0	0xFFFF0B00	0x0000	R/W
PLAELM1	0xFFFF0B04	0x0000	R/W
PLAELM2	0xFFFF0B08	0x0000	R/W
PLAELM3	0xFFFF0B0C	0x0000	R/W
PLAELM4	0xFFFF0B10	0x0000	R/W
PLAELM5	0xFFFF0B14	0x0000	R/W
PLAELM6	0xFFFF0B18	0x0000	R/W
PLAELM7	0xFFFF0B1C	0x0000	R/W
PLAELM8	0xFFFF0B20	0x0000	R/W
PLAELM9	0xFFFF0B24	0x0000	R/W
PLAELM10	0xFFFF0B28	0x0000	R/W
PLAELM11	0xFFFF0B2C	0x0000	R/W
PLAELM12	0xFFFF0B30	0x0000	R/W
PLAELM13	0xFFFF0B34	0x0000	R/W
PLAELM14	0xFFFF0B38	0x0000	R/W
PLAELM15	0xFFFF0B3C	0x0000	R/W

PLAELMx are Element 0 to Element 15 control registers. They configure the input and output mux of each element, select the function in the lookup table, and bypass/use the flip-flop. See Table 147 and Table 152.

Table 147. PLAELMx MMR Bit Descriptions

Bit	Value	Description
31:11		Reserved.
10:9		Mux 0 control (see Table 152).
8:7		Mux 1 control (see Table 152).
6		Mux 2 control. Set by user to select the output of Mux 0. Cleared by user to select the bit value from PLADIN.
5		Mux 3 control. Set by user to select the input pin of the particular element. Cleared by user to select the output of Mux 1.
4:1		Lookup table control.
	0000	0.
	0001	NOR.
	0010	B AND NOT A.
	0011	NOT A.
	0100	A AND NOT B.
	0101	NOT B.
	0110	EXOR.
	0111	NAND.
	1000	AND.
	1001	EXNOR.
	1010	B.
	1011	NOT A OR B.
	1100	A.
	1101	A OR NOT B.
	1110	OR.
	1111	1.
0		Mux 4 control. Set by user to bypass the flip-flop. Cleared by user to select the flip-flop (cleared by default).

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the core clock frequency, or an external GPIO (P1.0 or P0.6). The maximum frequency of the clock input is 44 Mhz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 78.

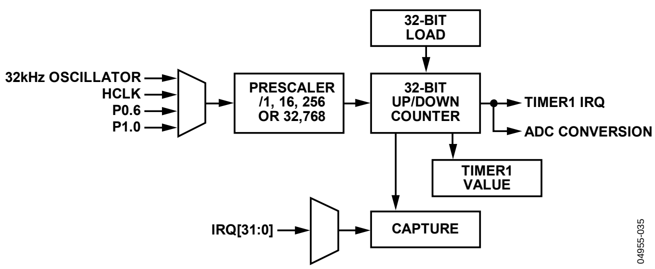


Figure 78. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

Table 177. T1LD Register

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000000	R/W

T1LD is a 32-bit load register.

Table 178. T1VAL Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0xFFFFFFFF	R

T1VAL is a 32-bit read-only register that represents the current state of the counter.

Table 179. T1CON Register

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

T1CON is the configuration MMR described in Table 180.

Table 186. T2CON MMR Bit Descriptions

Bit	Value	Description
31:11		Reserved.
10:9		Clock source.
	00	External crystal.
	01	External crystal.
	10	Internal oscillator.
	11	Core clock (41 MHz/2^{CD}).
8		Count up. Set by user for Timer2 to count up. Cleared by user for Timer2 to count down by default.
7		Timer2 enable bit. Set by user to enable Timer2. Cleared by user to disable Timer2 by default.
6		Timer2 mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode. Default mode.
5:4		Format.
	00	Binary.
	01	Reserved.
	10	Hr: min: sec: Hundredths (23 hours to 0 hour).
	11	Hr: min: sec: Hundredths (255 hours to 0 hour).
3:0		Prescale.
	0000	Source Clock/1 by default.
	0100	Source Clock/16.
	1000	Source Clock/256 expected for Format 2 and Format 3.
	1111	Source Clock/32,768.

Table 187. T2CLRI Register

Name	Address	Default Value	Access
T2CLRI	0xFFFF034C	0xFF	W

T2CLRI is an 8-bit register. Writing any value to this register clears the Timer2 interrupt.

Timer3 (Watchdog Timer)

Timer3 has two modes of operation: normal mode and watchdog mode. The watchdog timer is used to recover from an illegal software state. Once enabled, it requires periodic servicing to prevent it from forcing a processor reset.

Normal Mode

Timer3 in normal mode is identical to Timer0, except for the clock source and the count-up functionality. The clock source is 32 kHz from the PLL and can be scaled by a factor of 1, 16, or 256 (see Figure 80).

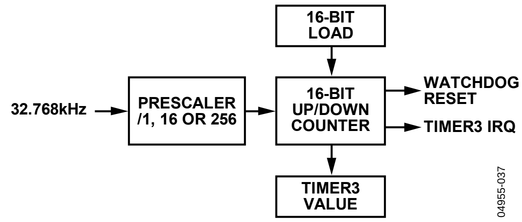


Figure 80. Timer3 Block Diagram

Watchdog Mode

Watchdog mode is entered by setting Bit 5 in the T3CON MMR. Timer3 decreases from the value present in the T3LD register to 0. T3LD is used as the timeout. The maximum timeout can be 512 sec, using the prescaler/256, and full scale in T3LD. Timer3 is clocked by the internal 32 kHz crystal when operating in watchdog mode. Note that to enter watchdog mode successfully, Bit 5 in the T3CON MMR must be set after writing to the T3LD MMR.

If the timer reaches 0, a reset or an interrupt occurs, depending on Bit 1 in the T3CON register. To avoid reset or interrupt, any value must be written to T3CLRI before the expiration period. This reloads the counter with T3LD and begins a new timeout period.

When watchdog mode is entered, T3LD and T3CON are write-protected. These two registers cannot be modified until a reset clears the watchdog enable bit, which causes Timer3 to exit watchdog mode.

The Timer3 interface consists of four MMRs: T3LD, T3VAL, T3CON, and T3CLRI.

Table 188. T3LD Register

Name	Address	Default Value	Access
T3LD	0xFFFF0360	0x0000	R/W

T3LD is a 16-bit register load register.

Table 189. T3VAL Register

Name	Address	Default Value	Access
T3VAL	0xFFFF0364	0xFFFF	R

T3VAL is a 16-bit read-only register that represents the current state of the counter.

Table 190. T3CON Register

Name	Address	Default Value	Access
T3CON	0xFFFF0368	0x0000	R/W

T3CON is the configuration MMR described in Table 191.