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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12 x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7026bstz62i

Table 6. SPI Master Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

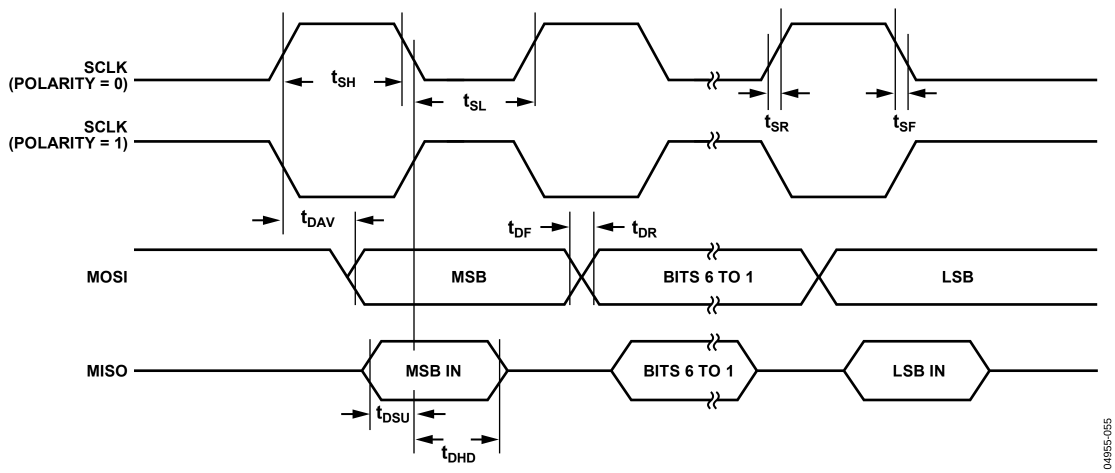

Figure 15. SPI Master Mode Timing (Phase Mode = 1)

Table 8. SPI Slave Mode Timing (Phsae Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.
[2] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

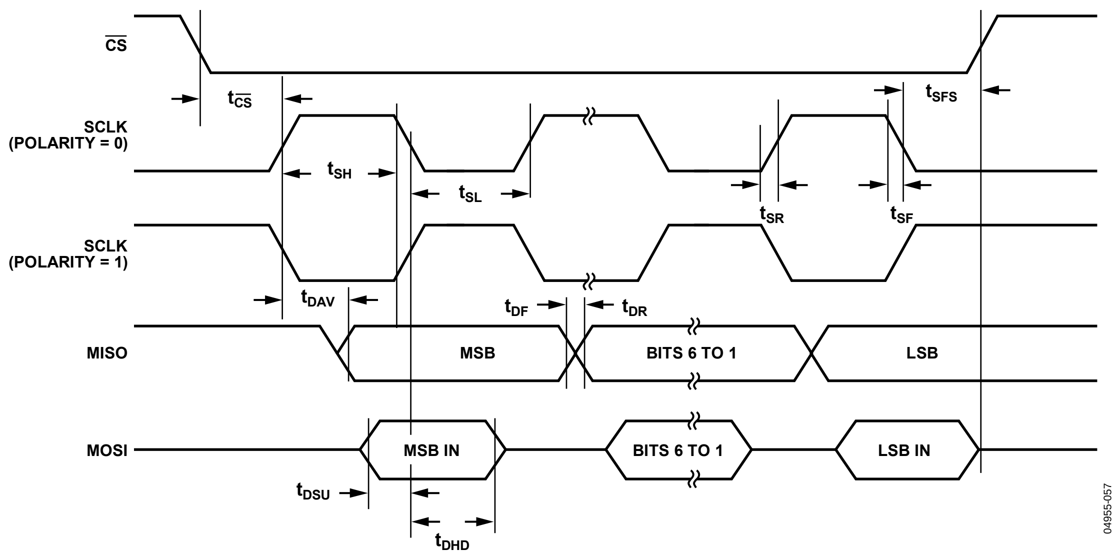

Figure 17. SPI Slave Mode Timing (Phase Mode = 1)

Table 11. Pin Function Descriptions (ADuC7019/ADuC7020/ADuC7021/ADuC7022)

Pin No.				
7019/7020	7021	7022	Mnemonic	Description
38	37	36	ADC0	Single-Ended or Differential Analog Input 0.
39	38	37	ADC1	Single-Ended or Differential Analog Input 1.
40	39	38	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
1	40	39	ADC3/CMP1	Single-Ended or Differential Analog Input 3 (Buffered Input on ADuC7019)/ Comparator Negative Input.
2	1	40	ADC4	Single-Ended or Differential Analog Input 4.
–	2	1	ADC5	Single-Ended or Differential Analog Input 5.
–	3	2	ADC6	Single-Ended or Differential Analog Input 6.
–	4	3	ADC7	Single-Ended or Differential Analog Input 7.
–	–	4	ADC8	Single-Ended or Differential Analog Input 8.
–	–	5	ADC9	Single-Ended or Differential Analog Input 9.
3	5	6	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
4	6	–	DAC0/ADC12	DAC0 Voltage Output/Single-Ended or Differential Analog Input 12.
5	7	–	DAC1/ADC13	DAC1 Voltage Output/Single-Ended or Differential Analog Input 13.
6	–	–	DAC2/ADC14	DAC2 Voltage Output/Single-Ended or Differential Analog Input 14.
7	–	–	DAC3/ADC15	DAC3 Voltage Output on ADuC7020. On the ADuC7019, a 10 nF capacitor must be connected between this pin and AGND/Single-Ended or Differential Analog Input 15 (see Figure 53).
8	8	7	TMS	Test Mode Select, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases, an external pull-up resistor (~100K) is also required to ensure that the part does not enter an erroneous state.
9	9	8	TDI	Test Data In, JTAG Test Port Input. Debug and download access.
10	10	9	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot Mode (BM). The ADuC7019/20/21/22 enter serial download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
11	11	10	P0.6/T1/MRST/PLAO[3]	Multifunction Pin. Driven low after reset. General-Purpose Output Port 0.6/ Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
12	12	11	TCK	Test Clock, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases an external pull-up resistor (~100K) is also required to ensure that the part does not enter an erroneous state.
13	13	12	TDO	Test Data Out, JTAG Test Port Output. Debug and download access.
14	14	13	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
15	15	14	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
16	16	15	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
17	17	16	DGND	Ground for Core Logic.
18	18	17	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/Test Reset, JTAG Test Port Input/ ADC_{BUSY} Signal Output.
19	19	18	$\overline{RST}$	Reset Input, Active Low.
20	20	19	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
21	21	20	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

Pin No.				
7019/7020	7021	7022	Mnemonic	Description
22	22	21	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/ Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
23	23	22	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/ Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/ Programmable Logic Array Output Element 4.
24	24	23	XCLKO	Output from the Crystal Oscillator Inverter.
25	25	24	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
26	26	25	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
27	27	26	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
28	28	27	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
29	29	28	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
30	30	29	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
31	31	30	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
32	32	31	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
33	33	32	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/ Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0.
34	–	–	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
35	34	33	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 μF capacitor when using the internal reference.
36	35	34	AGND	Analog Ground. Ground reference point for the analog circuitry.
37	36	35	AV_{DD}	3.3 V Analog Power.
0	0	0	EP	Exposed Pad. The pin configuration for the ADuC7019/ADuC7020/ ADuC7021/ADuC7022 has an exposed pad that must be soldered for mechanical purposes and left unconnected.

ADuC7024/ADuC7025

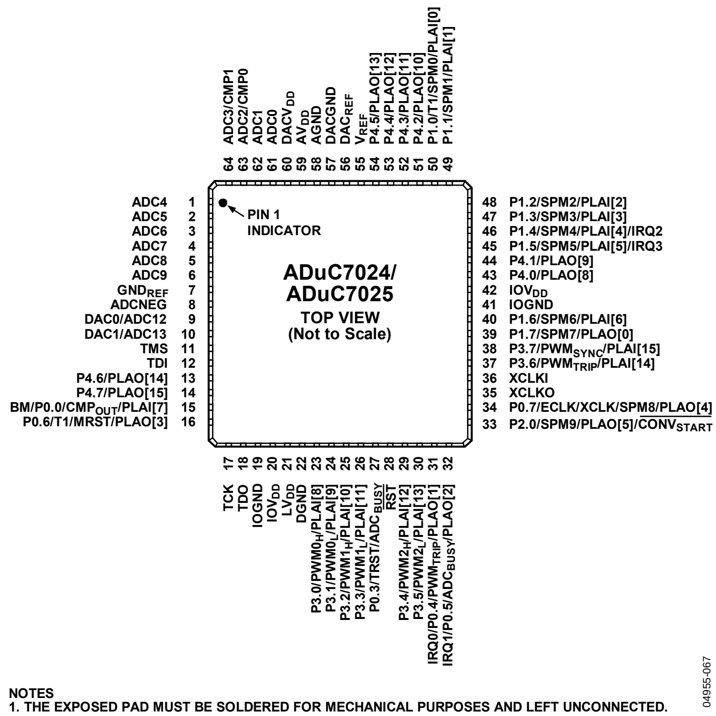

Figure 23. 64-Lead LFCSP_VQ Pin Configuration (ADuC7024/ADuC7025)

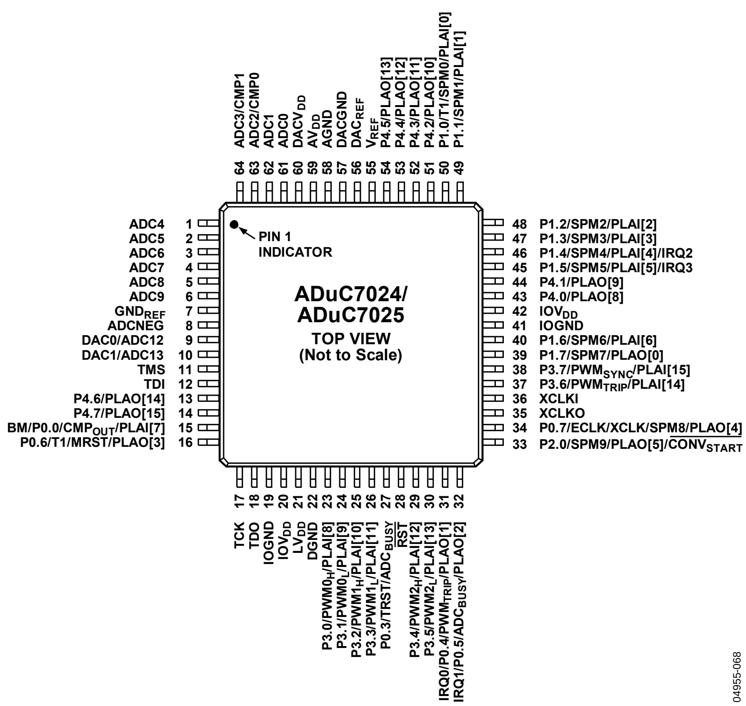

Figure 24. 64-Lead LQFP Pin Configuration (ADuC7024/ADuC7025)

ADUC7028

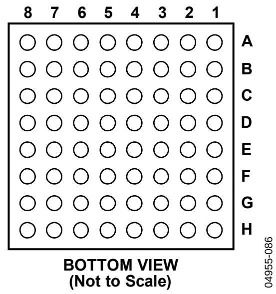

Figure 26. 64-Ball CSP_BGA Pin Configuration (ADuC7028)

Table 14. Pin Function Descriptions (ADuC7028)

Pin No.	Mnemonic	Description
A1	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
A2	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
A3	AV_{DD}	3.3 V Analog Power.
A4	AGND	Analog Ground. Ground reference point for the analog circuitry.
A5	DACGND	Ground for the DAC. Typically connected to AGND.
A6	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
A7	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
A8	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
B1	ADC4	Single-Ended or Differential Analog Input 4.
B2	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
B3	ADC1	Single-Ended or Differential Analog Input 1.
B4	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
B5	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
B6	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0.
B7	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
B8	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
C1	ADC6	Single-Ended or Differential Analog Input 6.
C2	ADC5	Single-Ended or Differential Analog Input 5.
C3	ADC0	Single-Ended or Differential Analog Input 0.
C4	P4.5/PLAO[13]	General-Purpose Input and Output Port 4.5/Programmable Logic Array Output Element 13.
C5	P4.3/PLAO[11]	General-Purpose Input and Output Port 4.3/Programmable Logic Array Output Element 11.
C6	P4.0/PLAO[8]	General-Purpose Input and Output Port 4.0/Programmable Logic Array Output Element 8.
C7	P4.1/PLAO[9]	General-Purpose Input and Output Port 4.1/Programmable Logic Array Output Element 9.
C8	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
D1	ADCNEG	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
D2	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
D3	ADC7	Single-Ended or Differential Analog Input 7.
D4	P4.4/PLAO[12]	General-Purpose Input and Output Port 4.4/Programmable Logic Array Output Element 12.
D5	P3.6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
D6	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.

Pin No.	Mnemonic	Description
E1	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
E2	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7029 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
E3	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E4	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E5	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
E7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F1	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F2	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
F3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
F4	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
F6	$\overline{RST}$	Reset Input, Active Low.
F7	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
G1	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
G2	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G3	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 μF capacitor to DGND only.
G4	DGND	Ground for Core Logic.
G5	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
G6	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
G7	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

More information relative to the programmer's model and the ARM7TDMI core architecture can be found in the following materials from ARM:

- DDI0029G, *ARM7TDMI Technical Reference Manual*
- DDI-0100, *ARM Architecture Reference Manual*

INTERRUPT LATENCY

The worst-case latency for a fast interrupt request (FIQ) consists of the following:

- The longest time the request can take to pass through the synchronizer
- The time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers including the PC
- The time for the data abort entry
- The time for FIQ entry

At the end of this time, the ARM7TDMI executes the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 μs in a system using a continuous 41.78 MHz processor clock.

The maximum interrupt request (IRQ) latency calculation is similar but must allow for the fact that FIQ has higher priority and may delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used. Some compilers have an option to compile without using this command. Another option is to run the part in thumb mode where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is a total of five cycles, which consist of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

Note that the ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, for example, when executing interrupt service routines.

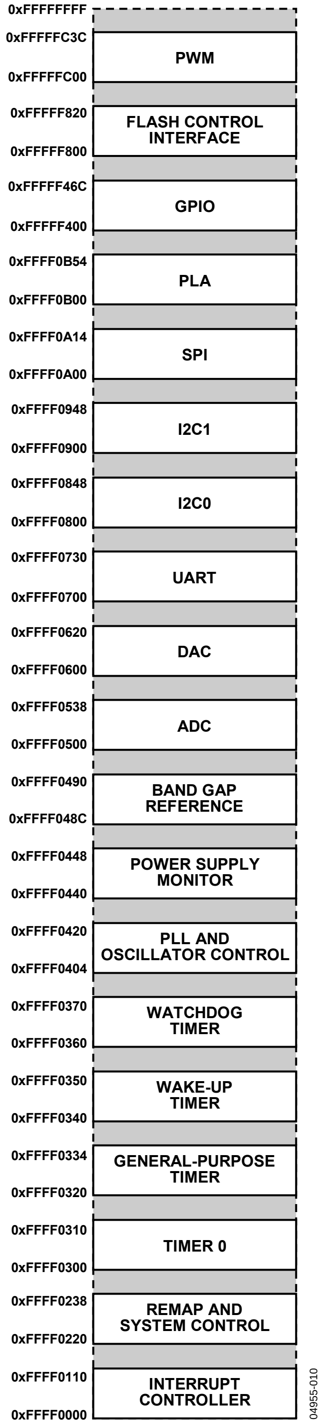

Figure 47. Memory Mapped Registers

Table 16. Complete MMR List

Address	Name	Byte	Access Type	Default Value	Page
IRQ Address Base = 0xFFFF0000					
0x0000	IRQSTA	4	R	0x00000000	83
0x0004	IRQSIG[1]	4	R	0x00XXX000	83
0x0008	IRQEN	4	R/W	0x00000000	83
0x000C	IRQCLR	4	W	0x00000000	83
0x0010	SWICFG	4	W	0x00000000	84
0x0100	FIQSTA	4	R	0x00000000	84
0x0104	FIQSIG[1]	4	R	0x00XXX000	84
0x0108	FIQEN	4	R/W	0x00000000	84
0x010C	FIQCLR	4	W	0x00000000	84

[1] Depends on the level on the external interrupt pins (P0.4, P0.5, P1.4, and P1.5).

System Control Address Base = 0xFFFF0200					
0x0220	REMAP	1	R/W	0xXX[1]	55
0x0230	RSTSTA	1	R/W	0x01	55
0x0234	RSTCLR	1	W	0x00	55

[1] Depends on the model.

Timer Address Base = 0xFFFF0300					
0x0300	T0LD	2	R/W	0x0000	85
0x0304	T0VAL	2	R	0xFFFF	85
0x0308	T0CON	2	R/W	0x0000	85
0x030C	T0CLRI	1	W	0xFF	85
0x0320	T1LD	4	R/W	0x00000000	86
0x0324	T1VAL	4	R	0xFFFFFFFF	86
0x0328	T1CON	2	R/W	0x0000	86
0x032C	T1CLRI	1	W	0xFF	87
0x0330	T1CAP	4	R/W	0x00000000	87
0x0340	T2LD	4	R/W	0x00000000	87
0x0344	T2VAL	4	R	0xFFFFFFFF	87
0x0348	T2CON	2	R/W	0x0000	87
0x034C	T2CLRI	1	W	0xFF	88
0x0360	T3LD	2	R/W	0x0000	88
0x0364	T3VAL	2	R	0xFFFF	88
0x0368	T3CON	2	R/W	0x0000	88
0x036C	T3CLRI	1	W	0x00	89

PLL Base Address = 0xFFFF0400					
0x0404	POWKEY1	2	W	0x0000	60
0x0408	POWCON	2	R/W	0x0003	60
0x040C	POWKEY2	2	W	0x0000	60
0x0410	PLLKEY1	2	W	0x0000	60
0x0414	PLLCON	1	R/W	0x21	60
0x0418	PLLKEY2	2	W	0x0000	60

PSM Address Base = 0xFFFF0440					
0x0440	PSMCON	2	R/W	0x0008	57
0x0444	CMPCON	2	R/W	0x0000	58

Address	Name	Byte	Access Type	Default Value	Page
Reference Address Base = 0xFFFF0480					
0x048C	REFCON	1	R/W	0x00	50
ADC Address Base = 0xFFFF0500					
0x0500	ADCCON	2	R/W	0x0600	46
0x0504	ADCCP	1	R/W	0x00	47
0x0508	ADCCN	1	R/W	0x01	47
0x050C	ADCSTA	1	R	0x00	48
0x0510	ADCDAT	4	R	0x00000000	48
0x0514	ADCRST	1	R/W	0x00	48
0x0530	ADCGN	2	R/W	0x0200	48
0x0534	ADCOF	2	R/W	0x0200	48
DAC Address Base = 0xFFFF0600					
0x0600	DAC0CON	1	R/W	0x00	56
0x0604	DAC0DAT	4	R/W	0x00000000	56
0x0608	DAC1CON	1	R/W	0x00	56
0x060C	DAC1DAT	4	R/W	0x00000000	56
0x0610	DAC2CON	1	R/W	0x00	56
0x0614	DAC2DAT	4	R/W	0x00000000	56
0x0618	DAC3CON	1	R/W	0x00	56
0x061C	DAC3DAT	4	R/W	0x00000000	56
UART Base Address = 0xFFFF0700					
0x0700	COMTX	1	R/W	0x00	71
	COMRX	1	R	0x00	71
	COMDIV0	1	R/W	0x00	71
0x0704	COMIEN0	1	R/W	0x00	71
	COMDIV1	1	R/W	0x00	72
0x0708	COMIID0	1	R	0x01	72
0x070C	COMCON0	1	R/W	0x00	72
0x0710	COMCON1	1	R/W	0x00	72
0x0714	COMSTA0	1	R	0x60	72
0x0718	COMSTA1	1	R	0x00	73
0x071C	COMSCR	1	R/W	0x00	73
0x0720	COMIEN1	1	R/W	0x04	73
0x0724	COMIID1	1	R	0x01	73
0x0728	COMADR	1	R/W	0xAA	74
0x072C	COMDIV2	2	R/W	0x0000	73

Address	Name	Byte	Access Type	Default Value	Page
I2C0 Base Address = 0xFFFF0800					
0x0800	I2C0MSTA	1	R/W	0x00	76
0x0804	I2C0SSTA	1	R	0x01	76
0x0808	I2C0SRX	1	R	0x00	77
0x080C	I2C0STX	1	W	0x00	77
0x0810	I2C0MRX	1	R	0x00	77
0x0814	I2C0MTX	1	W	0x00	77
0x0818	I2C0CNT	1	R/W	0x00	77
0x081C	I2C0ADR	1	R/W	0x00	77
0x0824	I2C0BYTE	1	R/W	0x00	77
0x0828	I2C0ALT	1	R/W	0x00	78
0x082C	I2C0CFG	1	R/W	0x00	78
0x0830	I2C0DIV	2	R/W	0x1F1F	79
0x0838	I2C0ID0	1	R/W	0x00	79
0x083C	I2C0ID1	1	R/W	0x00	79
0x0840	I2C0ID2	1	R/W	0x00	79
0x0844	I2C0ID3	1	R/W	0x00	79
0x0848	I2C0CCNT	1	R/W	0x01	79
0x084C	I2C0FSTA	2	R/W	0x0000	79
I2C1 Base Address = 0xFFFF0900					
0x0900	I2C1MSTA	1	R/W	0x00	76
0x0904	I2C1SSTA	1	R	0x01	76
0x0908	I2C1SRX	1	R	0x00	77
0x090C	I2C1STX	1	W	0x00	77
0x0910	I2C1MRX	1	R	0x00	77
0x0914	I2C1MTX	1	W	0x00	77
0x0918	I2C1CNT	1	R/W	0x00	77
0x091C	I2C1ADR	1	R/W	0x00	77
0x0924	I2C1BYTE	1	R/W	0x00	77
0x0928	I2C1ALT	1	R/W	0x00	78
0x092C	I2C1CFG	1	R/W	0x00	78
0x0930	I2C1DIV	2	R/W	0x1F1F	79
0x0938	I2C1ID0	1	R/W	0x00	79
0x093C	I2C1ID1	1	R/W	0x00	79
0x0940	I2C1ID2	1	R/W	0x00	79
0x0944	I2C1ID3	1	R/W	0x00	79
0x0948	I2C1CCNT	1	R/W	0x01	79
0x094C	I2C1FSTA	2	R/W	0x0000	79
SPI Base Address = 0xFFFF0A00					
0x0A00	SPISTA	1	R	0x00	75
0x0A04	SPIRX	1	R	0x00	75
0x0A08	SPITX	1	W	0x00	75
0x0A0C	SPIDIV	1	R/W	0x1B	75
0x0A10	SPICON	2	R/W	0x0000	75

Table 28. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads 4094 to 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7019/20/21/22/24/25/26/27/28/29 provide voltage output from on-chip band gap references proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The following is an example routine showing how to use the internal temperature sensor:

```
int main(void)
{
float a = 0;
      short b;
      ADCCON = 0x20;    // power-on the ADC
      delay(2000);
      ADCCP = 0x10;  // Select Temperature
Sensor as an // input to the ADC
      REFCON = 0x01; // connect internal 2.5V
reference // to Vref pin
      ADCCON = 0xE4; // continuous conversion
      while(1)
      {
              while (!ADCSTA){};
      // wait for end of conversion
              b = (ADCDAT >> 16);
      // To calculate temperature in °C, use
the formula:
              a = 0x525 - b;
      // ((Temperature = 0x525 - Sensor
Voltage) / 1.3)
              a /= 1.3;
              b = floor(a);
              printf("Temperature: %d
oC\n",b);
      }
      return 0;
}
```

BAND GAP REFERENCE

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides an on-chip band gap reference of 2.5 V, which can be used for the ADC and DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (V_{REF}) and used as a reference for other circuits in the system. An external buffer is required because of the low drive capability of the V_{REF} output. A programmable option also allows an external reference input on the V_{REF} pin. Note that it is not possible to disable the internal reference. Therefore, the external reference source must be capable of overdriving the internal reference source.

Table 29. REFCON Register

Name	Address	Default Value	Access
REFCON	0xFFFF048C	0x00	R/W

The band gap reference interface consists of an 8-bit MMR REFCON, described in Table 30.

Table 30. REFCON MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Internal reference output enable. Set by user to connect the internal 2.5 V reference to the V_{REF} pin. The reference can be used for an external component but must be buffered. Cleared by user to disconnect the reference from the V_{REF} pin.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;

  while ((T2VAL == t2val_old) || (T2VAL >
3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x01;
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

In noisy environments, noise can couple to the external crystal pins, and PLL may lose lock momentarily. A PLL interrupt is provided in the interrupt controller. The core clock is immediately halted, and this interrupt is only serviced when the lock is restored.

In case of crystal loss, the watchdog timer should be used. During initialization, a test on the RSTSTA register can determine if the reset came from the watchdog timer.

External Clock Selection

To switch to an external clock on P0.7, configure P0.7 in Mode 1. The external clock can be up to 44 MHz, providing the tolerance is 1%.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;

  while ((T2VAL == t2val_old) || (T2VAL
> 3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x03; //Select external clock
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

Power Control System

A choice of operating modes is available on the ADuC7019/20/21/22/24/25/26/27/28/29. Table 57 describes what part is powered on in the different modes and indicates the power-up time.

Table 58 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The ADC is turned off. Note that these values also include current consumption of the regulator and other parts on the test board where these values are measured.

Table 57. Operating Modes[1]

Mode	Core	Peripherals	PLL	XTAL/T2/T3	IRQ0 to IRQ3	Start-Up/Power-On Time
Active	X	X	X	X	X	130 ms at CD = 0
Pause		X	X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Nap			X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Sleep				X	X	1.58 ms
Stop					X	1.7 ms

[1] X indicates that the part is powered on.

Table 58. Typical Current Consumption at 25°C in Milliamperes

PC[2:0]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
000	Active	33.1	21.2	13.8	10	8.1	7.2	6.7	6.45
001	Pause	22.7	13.3	8.5	6.1	4.9	4.3	4	3.85
010	Nap	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8
011	Sleep	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
100	Stop	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

The PWMDAT1 register is a 10-bit register with a maximum value of 0x3FF (= 1023), which corresponds to a maximum programmed dead time of

$$t_{D(max)} = 1023 \times 2 \times t_{CORE} = 1023 \times 2 \times 24 \times 10^{-9} = 48.97\ \mu s$$

for a core clock of 41.78 MHz.

The dead time can be programmed to be zero by writing 0 to the PWMDAT1 register.

PWM Operating Mode (PWMCON and PWMSTA MMRs)

As discussed in the 3-Phase PWM section, the PWM controller of the ADuC7019/20/21/22/24/25/26/27/28/29 can operate in two distinct modes: single update mode and double update mode. The operating mode of the PWM controller is determined by the state of Bit 2 of the PWMCON register. If this bit is cleared, the PWM operates in the single update mode. Setting Bit 2 places the PWM in the double update mode. The default operating mode is single update mode.

In single update mode, a single PWMSYNC pulse is produced in each PWM period. The rising edge of this signal marks the start of a new PWM cycle and is used to latch new values from the PWM configuration registers (PWMDAT0 and PWMDAT1) and the PWM duty cycle registers (PWMCH0, PWMCH1, and PWMCH2) into the 3-phase timing unit. In addition, the PWMEN register is latched into the output control unit on the rising edge of the PWMSYNC pulse. In effect, this means that the characteristics and resulting duty cycles of the PWM signals can be updated only once per PWM period at the start of each cycle. The result is symmetrical PWM patterns about the midpoint of the switching period.

In double update mode, there is an additional PWMSYNC pulse produced at the midpoint of each PWM period. The rising edge of this new PWMSYNC pulse is again used to latch new values of the PWM configuration registers, duty cycle registers, and the PWMEN register. As a result, it is possible to alter both the characteristics (switching frequency and dead time) as well as the output duty cycles at the midpoint of each PWM cycle. Consequently, it is also possible to produce PWM switching patterns that are no longer symmetrical about the midpoint of the period (asymmetrical PWM patterns). In double update mode, it could be necessary to know whether operation at any point in time is in either the first half or the second half of the PWM cycle. This information is provided by Bit 0 of the PWMSTA register, which is cleared during operation in the first half of each PWM period (between the rising edge of the original PWMSYNC pulse and the rising edge of the new PWMSYNC pulse introduced in double update mode). Bit 0 of the PWMSTA register is set during operation in the second half of each PWM period. This status bit allows the user to make a determination of the particular half cycle during implementation of the PWMSYNC interrupt service routine, if required.

The advantage of double update mode is that lower harmonic voltages can be produced by the PWM process, and faster control bandwidths are possible. However, for a given PWM switching frequency, the PWMSYNC pulses occur at twice the rate in the double update mode. Because new duty cycle values must be computed in each PWMSYNC interrupt service routine, there is a larger computational burden on the ARM core in double update mode.

PWM Duty Cycles (PWMCH0, PWMCH1, and PWMCH2 MMRs)

The duty cycles of the six PWM output signals on Pin $PWM0_H$ to Pin $PWM2_L$ are controlled by the three 16-bit read/write duty cycle registers, PWMCH0, PWMCH1, and PWMCH2. The duty cycle registers are programmed in integer counts of the fundamental time unit, t_{CORE}. They define the desired on time of the high-side PWM signal produced by the 3-phase timing unit over half the PWM period. The switching signals produced by the 3-phase timing unit are also adjusted to incorporate the programmed dead time value in the PWMDAT1 register. The 3-phase timing unit produces active high signals so that a high level corresponds to a command to turn on the associated power device.

Figure 69 shows a typical pair of PWM outputs (in this case, 0H and 0L) from the timing unit in single update mode. All illustrated time values indicate the integer value in the associated register and can be converted to time by simply multiplying by the fundamental time increment, t_{CORE}. Note that the switching patterns are perfectly symmetrical about the midpoint of the switching period in this mode because the same values of PWMCH0, PWMDAT0, and PWMDAT1 are used to define the signals in both half cycles of the period.

Figure 69 also demonstrates how the programmed duty cycles are adjusted to incorporate the desired dead time into the resulting pair of PWM signals. The dead time is incorporated by moving the switching instants of both PWM signals (0H and 0L) away from the instant set by the PWMCH0 register.

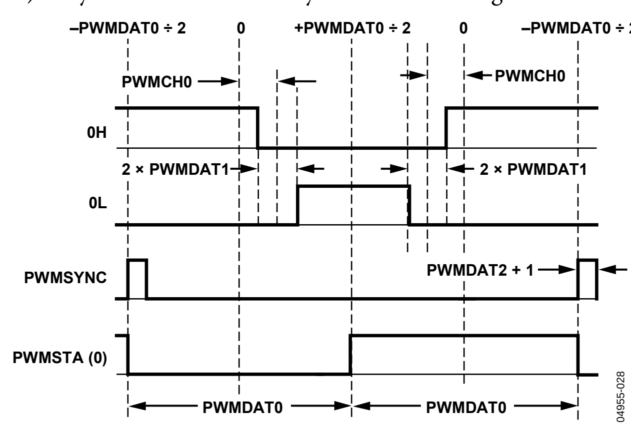

Figure 69. Typical PWM Outputs of the 3-Phase Timing Unit (Single Update Mode)

Table 83. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

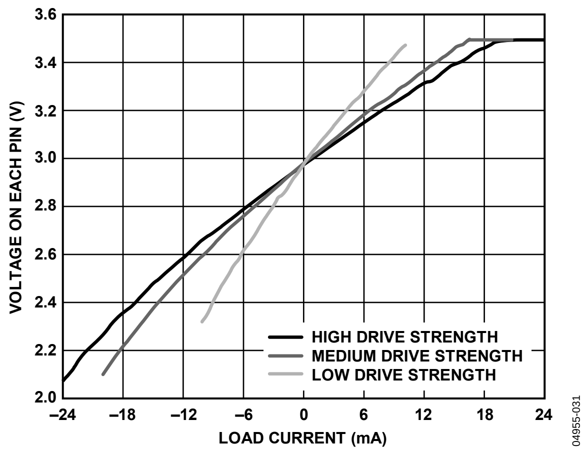

Figure 73. Programmable Strength for High Level (Typical Values)

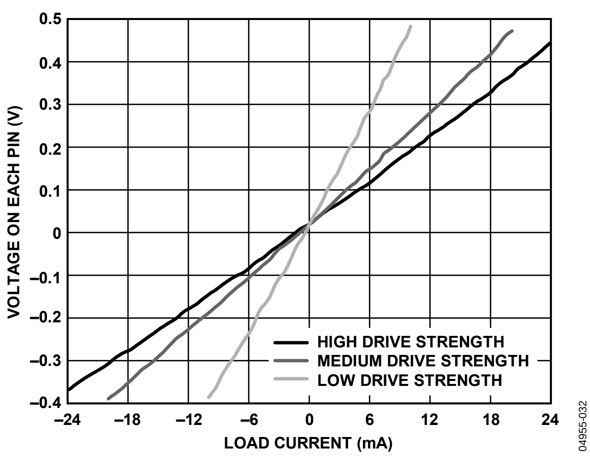

Figure 74. Programmable Strength for Low Level (Typical Values)

The drive strength bits can be written to one time only after reset. More writing to related bits has no effect on changing drive strength. The GPIO drive strength and pull-up disable is not always adjustable for the GPIO port. Some control bits cannot be changed (see Table 84).

Table 84. GPxPAR Control Bits Access Descriptions

Bit	GP0PAR	GP1PAR
31	Reserved	Reserved
30 to 29	R/W	R/W
28	R/W	R/W
27	Reserved	Reserved
26 to 25	R/W	R/W
24	R/W	R/W
23	Reserved	Reserved
22 to 21	R/W	R (b00)
20	R/W	R/W
19	Reserved	Reserved
18 to 17	R (b00)	R (b00)
16	R/W	R/W
15	Reserved	Reserved
14 to 13	R (b00)	R (b00)
12	R/W	R/W
11	Reserved	Reserved
10 to 9	R (b00)	R (b00)
8	R/W	R/W
7	Reserved	Reserved
6 to 5	R (b00)	R (b00)
4	R/W	R/W
3	Reserved	Reserved
2 to 1	R (b00)	R (b00)
0	R/W	R/W

The serial communication adopts an asynchronous protocol, which supports various word lengths, stop bits, and parity generation options selectable in the configuration register.

Baud Rate Generation

There are two ways of generating the UART baud rate, normal 450 UART baud rate generation and the fractional divider.

Normal 450 UART Baud Rate Generation

The baud rate is a divided version of the core clock using the values in the COMDIV0 and COMDIV1 MMRs (16-bit value, DL).

$$\text{Baud Rate} = \frac{41.78\,\text{MHz}}{2^{CD} \text{ - } 16 \times 2 \times \text{DL}}$$

Table 93 gives some common baud rate values.

Table 93. Baud Rate Using the Normal Baud Rate Generator

Baud Rate	CD	DL	Actual Baud Rate	% Error
9600	0	0x88	9600	0
19,200	0	0x44	19,200	0
115,200	0	0x0B	118,691	3
9600	3	0x11	9600	0
19,200	3	0x08	20,400	6.25
115,200	3	0x01	163,200	41.67

Fractional Divider

The fractional divider, combined with the normal baud rate generator, produces a wider range of more accurate baud rates.

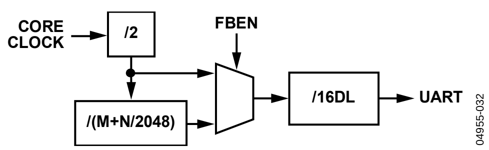

Figure 75. Baud Rate Generation Options

Calculation of the baud rate using fractional divider is as follows:

$$Baud\ \ Rate = \frac{41.78\,\text{MHz}}{2^{CD} \times 16 \times DL \times 2 \times \left(M + \frac{N}{2048}\right)}$$

$$\text{M} + \frac{\text{N}}{2048} = \frac{41.78\,\text{MHz}}{\text{Baud Rate} \times\ 2^{CD} \times 16 \times \text{DL} \times 2}$$

For example, generation of 19,200 baud with CD bits = 3 (Table 93 gives DL = 0x08) is

$$M + \frac{N}{2048} = \frac{41.78\,\text{MHz}}{19200\ \times 2^{3} \times 16 \times 8 \times 2}$$

$$M + \frac{N}{2048} = 1.06$$

where:
$M = 1$
$N = 0.06 \times 2048 = 128$

$$\text{Baud Rate} = \frac{41.78\,\text{MHz}}{2^{3} \times 16 \times 8 \times 2 \times \frac{128}{2048}}$$

where:
Baud Rate = 19,200 bps

Error = 0%, compared to 6.25% with the normal baud rate generator.

UART Register Definitions

The UART interface consists of 12 registers: COMTX, COMRX, COMDIV0, COMIEN0, COMDIV1, COMIID0, COMCON0, COMCON1, COMSTA0, COMSTA1, COMSCR, and COMDIV2.

Table 94. COMTX Register

Name	Address	Default Value	Access
COMTX	0xFFFF0700	0x00	R/W

COMTX is an 8-bit transmit register.

Table 95. COMRX Register

Name	Address	Default Value	Access
COMRX	0xFFFF0700	0x00	R

COMRX is an 8-bit receive register.

Table 96. COMDIV0 Register

Name	Address	Default Value	Access
COMDIV0	0xFFFF0700	0x00	R/W

COMDIV0 is a low byte divisor latch. COMTX, COMRX, and COMDIV0 share the same address location. COMTX and COMRX can be accessed when Bit 7 in the COMCON0 register is cleared. COMDIV0 can be accessed when Bit 7 of COMCON0 is set.

Table 97. COMIEN0 Register

Name	Address	Default Value	Access
COMIEN0	0xFFFF0704	0x00	R/W

COMIEN0 is the interrupt enable register.

Table 98. COMIEN0 MMR Bit Descriptions

Bit	Name	Description
7:4	N/A	Reserved.
3	EDSSI	Modem status interrupt enable bit. Set by user to enable generation of an interrupt if any of COMSTA1[3:1] is set. Cleared by user.
2	ELSI	Rx status interrupt enable bit. Set by user to enable generation of an interrupt if any of COMSTA0[4:1] is set. Cleared by user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by user to enable interrupt when buffer is empty during a transmission. Cleared by user.
0	ERBFI	Enable receive buffer full interrupt. Set by user to enable interrupt when buffer is full during a reception. Cleared by user.

Table 108. COMSTA1 Register

Name	Address	Default Value	Access
COMSTA1	0xFFFF0718	0x00	R

COMSTA1 is a modem status register.

Table 109. COMSTA1 MMR Bit Descriptions

Bit	Name	Description
7	DCD	Data carrier detect.
6	RI	Ring indicator.
5	DSR	Data set ready.
4	CTS	Clear to send.
3	DDCD	Delta DCD. Set automatically if DCD changed state since last COMSTA1 read. Cleared automatically by reading COMSTA1.
2	TERI	Trailing edge RI. Set if RI changed from 0 to 1 since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
1	DDSR	Delta DSR. Set automatically if DSR changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.

Table 110. COMSCR Register

Name	Address	Default Value	Access
COMSCR	0xFFFF071C	0x00	R/W

COMSCR is an 8-bit scratch register used for temporary storage. It is also used in network addressable UART mode.

Table 111. COMDIV2 Register

Name	Address	Default Value	Access
COMDIV2	0xFFFF072C	0x0000	R/W

COMDIV2 is a 16-bit fractional baud divide register.

Table 112. COMDIV2 MMR Bit Descriptions

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by user to enable the fractional baud rate generator. Cleared by user to generate baud rate using the standard 450 UART baud rate generator.
14:13		Reserved.
12:11	FBM[1:0]	M if FBM = 0, M = 4 (see the Fractional Divider section).
10:0	FBN[10:0]	N (see the Fractional Divider section).

Network Addressable UART Mode

This mode connects the MicroConverter to a 256-node serial network, either as a hardware single master or via software in a multimaster network. Bit 7 (ENAM) of the COMIEN1 register must be set to enable UART in network addressable mode (see Table 114). Note that there is no parity check in this mode.

Network Addressable UART Register Definitions

Four additional registers, COMIEN0, COMIEN1, COMIID1, and COMADR are used in network addressable UART mode only.

In network address mode, the least significant bit of the COMIEN1 register is the transmitted network address control bit. If set to 1, the device is transmitting an address. If cleared to 0, the device is transmitting data. For example, the following master-based code transmits the slave's address followed by the data:

```
  COMIEN1  = 0xE7;       //Setting ENAM,
E9BT, E9BR, ETD, NABP
  COMTX = 0xA0;  // Slave address is 0xA0
  while(!(0x020==(COMSTA0 & 0x020))){} //
wait for adr tx to finish.
  COMIEN1  = 0xE6;       //  Clear NAB bit
to indicate Data is coming
   COMTX = 0x55; // Tx data to slave: 0x55
```

Table 113. COMIEN1 Register

Name	Address	Default Value	Access
COMIEN1	0xFFFF0720	0x04	R/W

COMIEN1 is an 8-bit network enable register.

Table 114. COMIEN1 MMR Bit Descriptions

Bit	Name	Description
7	ENAM	Network address mode enable bit. Set by user to enable network address mode. Cleared by user to disable network address mode.
6	E9BT	9-bit transmit enable bit. Set by user to enable 9-bit transmit. ENAM must be set. Cleared by user to disable 9-bit transmit.
5	E9BR	9-bit receive enable bit. Set by user to enable 9-bit receive. ENAM must be set. Cleared by user to disable 9-bit receive.
4	ENI	Network interrupt enable bit.
3	E9BD	Word length. Set for 9-bit data. E9BT has to be cleared. Cleared for 8-bit data.
2	ETD	Transmitter pin driver enable bit. Set by user to enable SOUT pin as an output in slave mode or multimaster mode. Cleared by user; SOUT is three-state.
1	NABP	Network address bit. Interrupt polarity bit.
0	NAB	Network address bit (if NABP = 1). Set by user to transmit the slave address. Cleared by user to transmit data.

Table 115. COMIID1 Register

Name	Address	Default Value	Access
COMIID1	0xFFFF0724	0x01	R

COMIID1 is an 8-bit network interrupt register. Bit 7 to Bit 4 are reserved (see Table 116).

I²C-COMPATIBLE INTERFACES

The ADuC7019/20/21/22/24/25/26/27/28/29 support two licensed I²C interfaces. The I²C interfaces are both implemented as a hard-ware master and a full slave interface. Because the two I²C inter-faces are identical, this data sheet describes only I2C0 in detail. Note that the two masters and one of the slaves have individual interrupts (see the Interrupt System section).

Note that when configured as an I²C master device, the ADuC7019/20/21/22/24/25/26/27/28/29 cannot generate a repeated start condition.

The two GPIO pins used for data transfer, SDAx and SCLx, are configured in a wired-AND format that allows arbitration in a multimaster system. These pins require external pull-up resistors. Typical pull-up values are 10 kΩ.

The I²C bus peripheral address in the I²C bus system is pro-grammed by the user. This ID can be modified any time a transfer is not in progress. The user can configure the interface to respond to four slave addresses.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the slave device address and the direction of the data transfer during the initial address transfer. If the master does not lose arbitration and the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition and the bus becomes idle.

The I²C peripheral can be configured only as a master or slave at any given time. The same I²C channel cannot simultaneously support master and slave modes.

Serial Clock Generation

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (400 kHz) or standard mode (100 kHz).

The bit rate is defined in the I2C0DIV MMR as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{(2 + DIVH) + (2 + DIVL)}$$

where:
f_{UCLK} = clock before the clock divider.
$DIVH$ = the high period of the clock.
$DIVL$ = the low period of the clock.

Thus, for 100 kHz operation,

$$DIVH = DIVL = 0xCF$$

and for 400 kHz,

$$DIVH = 0x28, DIVL = 0x3C$$

The I2CxDIV registers correspond to DIVH:DIVL.

Slave Addresses

The registers I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3 contain the device IDs. The device compares the four I2C0IDx registers to the address byte. To be correctly addressed, the seven MSBs of either ID register must be identical to that of the seven MSBs of the first received address byte. The LSB of the ID registers (the transfer direction bit) is ignored in the process of address recognition.

I²C Registers

The I²C peripheral interface consists of 18 MMRs, which are discussed in this section.

Table 126. I2CxMSTA Registers

Name	Address	Default Value	Access
I2C0MSTA	0xFFFF0800	0x00	R/W
I2C1MSTA	0xFFFF0900	0x00	R/W

I2CxMSTA are status registers for the master channel.

Table 127. I2C0MSTA MMR Bit Descriptions

Bit	Access Type	Description
7	R/W	Master transmit FIFO flush. Set by user to flush the master Tx FIFO. Cleared automatically after the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
6	R	Master busy. Set automatically if the master is busy. Cleared automatically.
5	R	Arbitration loss. Set in multimaster mode if another master has the bus. Cleared when the bus becomes available.
4	R	No ACK. Set automatically if there is no acknowledge of the address by the slave device. Cleared automatically by reading the I2C0MSTA register.
3	R	Master receive IRQ. Set after receiving data. Cleared automatically by reading the I2C0MRX register.
2	R	Master transmit IRQ. Set at the end of a transmission. Cleared automatically by writing to the I2C0MTX register.
1	R	Master transmit FIFO underflow. Set automatically if the master transmit FIFO is underflowing. Cleared automatically by writing to the I2C0MTX register.
0	R	Master TX FIFO not full. Set automatically if the slave transmit FIFO is not full. Cleared automati-cally by writing twice to the I2C0STX register.

Table 128. I2CxSSTA Registers

Name	Address	Default Value	Access
I2C0SSTA	0xFFFF0804	0x01	R
I2C1SSTA	0xFFFF0904	0x01	R

I2CxSSTA are status registers for the slave channel.

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the core clock frequency, or an external GPIO (P1.0 or P0.6). The maximum frequency of the clock input is 44 Mhz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 78.

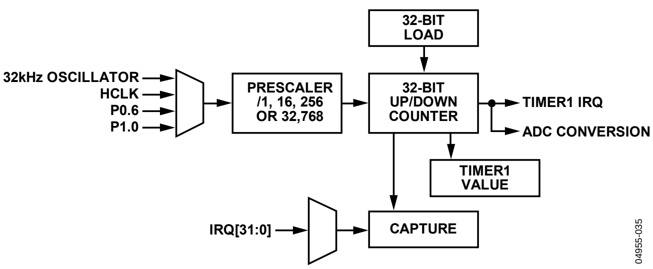

Figure 78. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

Table 177. T1LD Register

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000000	R/W

T1LD is a 32-bit load register.

Table 178. T1VAL Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0xFFFFFFFF	R

T1VAL is a 32-bit read-only register that represents the current state of the counter.

Table 179. T1CON Register

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

T1CON is the configuration MMR described in Table 180.

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7019/20/21/22/24/25/26/27/28/29 operational power supply voltage range is 2.7 V to 3.6 V. Separate analog and digital power supply pins (AV_{DD} and IOV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system IOV_{DD} line. In this mode, the part can also operate with split supplies; that is, it can use different voltage levels for each supply. For example, the system can be designed to operate with an IOV_{DD} voltage level of 3.3 V whereas the AV_{DD} level can be at 3 V or vice versa. A typical split supply configuration is shown in Figure 87.

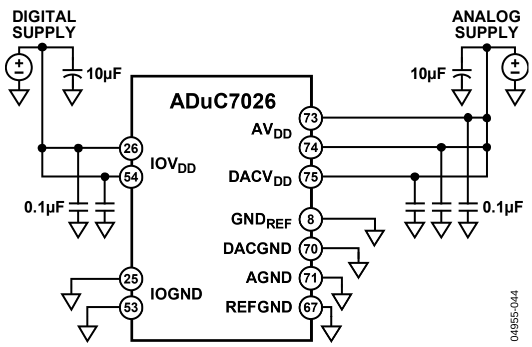

Figure 87. External Dual Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AV_{DD} by placing a small series resistor and/or ferrite bead between AV_{DD} and IOV_{DD} and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 88. With this configuration, other analog circuitry (such as op amps and voltage reference) can be powered from the AV_{DD} supply line as well.

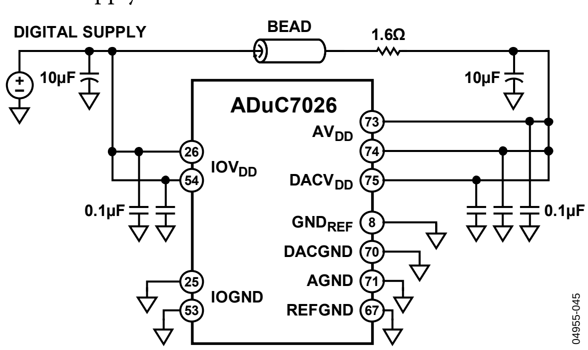

Figure 88. External Single Supply Connections

Note that in both Figure 87 and Figure 88, a large value (10 µF) reservoir capacitor sits on IOV_{DD}, and a separate 10 µF capacitor sits on AV_{DD}. In addition, local small-value (0.1 µF) capacitors are located at each AV_{DD} and IOV_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane.

Finally, note that the analog and digital ground pins on the ADuC7019/20/21/22/24/25/26/27/28/29 must be referenced to the same system ground reference point at all times.

IOV_{DD} Supply Sensitivity

The IOV_{DD} supply is sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature ensures that no flash interface timings or ARM7TDMI timings are violated.

Typically, frequency noise greater than 50 kHz and 50 mV p-p on top of the supply causes the core to stop working.

If decoupling values recommended in the Power Supplies section do not sufficiently dampen all noise sources below 50 mV on IOV_{DD}, a filter such as the one shown in Figure 89 is recommended.

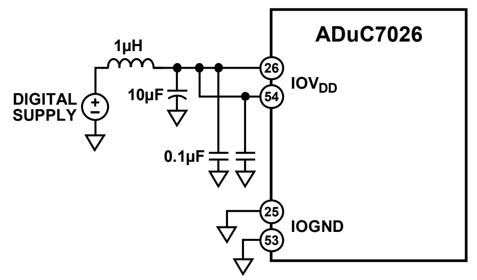

Figure 89. Recommended IOV_{DD} Supply Filter

Linear Voltage Regulator

Each ADuC7019/20/21/22/24/25/26/27/28/29 requires a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOV_{DD} for the core logic. The LV_{DD} pin is the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between LV_{DD} and DGND (as close as possible to these pins) to act as a tank of charge as shown in Figure 90.

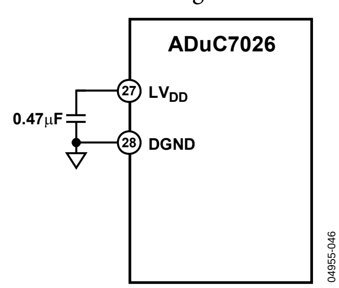

Figure 90. Voltage Regulator Connections

The LV_{DD} pin should not be used for any other chip. It is also recommended to use excellent power supply decoupling on IOV_{DD} to help improve line regulation performance of the on-chip voltage regulator.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of the ADuC7019/20/21/22/24/25/26/27/28/29-based designs to achieve optimum performance from the ADCs and DAC.

Although the parts have separate pins for analog and digital ground (AGND and IOGND), the user must not tie these to two separate ground planes unless the two ground planes are connected very close to the part. This is illustrated in the simplified example shown in Figure 91a. In systems where digital and analog ground planes are connected together somewhere else (at the system power supply, for example), the planes cannot be reconnected near the part because a ground loop results. In these cases, tie all the ADuC7019/20/21/22/24/25/26/27/28/29 AGND and IOGND pins to the analog ground plane, as illustrated in Figure 91b. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board so that digital return currents do not flow near analog circuitry (and vice versa).

The ADuC7019/20/21/22/24/25/26/27/28/29 can then be placed between the digital and analog sections, as illustrated in Figure 91c.

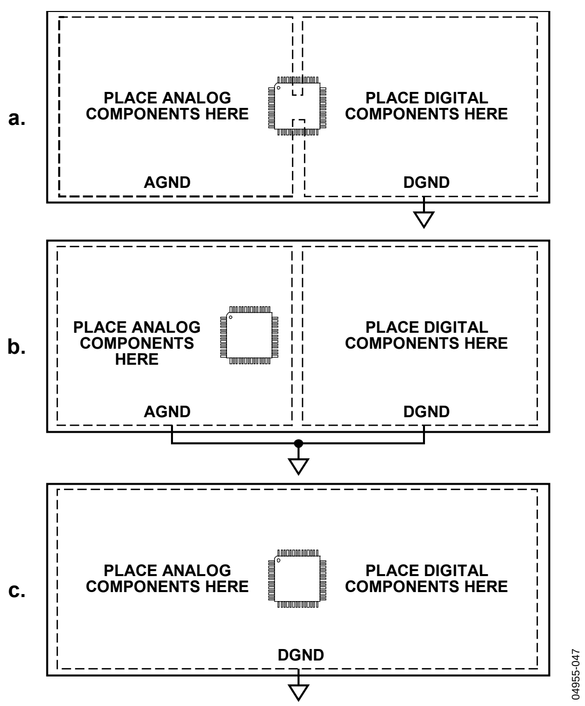

Figure 91. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, the user should pay particular attention to the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations.

For example, do not power components on the analog side (as seen in Figure 91b) with IOV_{DD} because that forces return currents from IOV_{DD} to flow through AGND. Avoid digital currents flowing under analog circuitry, which can occur if a noisy digital chip is placed on the left half of the board (shown in Figure 91c). If possible, avoid large discontinuities in the ground plane(s) such as those formed by a long trace on the same layer because they force return signals to travel a longer path. In addition, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

When connecting fast logic signals (rise/fall time < 5 ns) to any of the ADuC7019/20/21/22/24/25/26/27/28/29 digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the part's input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the part and affecting the accuracy of ADC conversions.

CLOCK OSCILLATOR

The clock source for the ADuC7019/20/21/22/24/25/26/27/28/29 can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XCLKI and XCLKO, and connect a capacitor from each pin to ground as shown in Figure 92. The crystal allows the PLL to lock correctly to give a frequency of 41.78 MHz. If no external crystal is present, the internal oscillator is used to give a typical frequency of 41.78 MHz ± 3%.

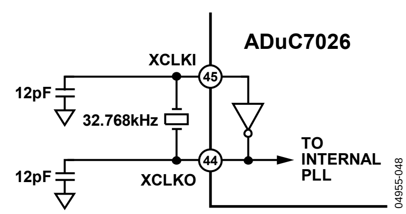

Figure 92. External Parallel Resonant Crystal Connections

To use an external source clock input instead of the PLL (see Figure 93), Bit 1 and Bit 0 of PLLCON must be modified.The external clock uses P0.7 and XCLK.

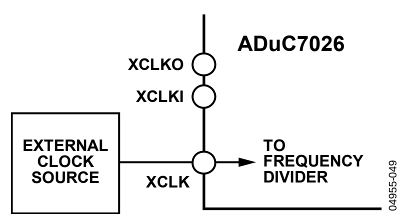

Figure 93. Connecting an External Clock Source

Using an external clock source, the ADuC7019/20/21/22/24/25/26/27/28/29-specified operational clock speed range is 50 kHz to 44 MHz ± 1%, which ensures correct operation of the analog peripherals and Flash/EE.