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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7027bstz62

REVISION HISTORY

12/15—Rev. F to Rev. G

Changed CP-40-1 to CP-40-9 ..... Universal
Updated Outline Dimensions 97
Deleted Figure 96 (CP-40-1); Renumbered Sequentially 97
Changes to Ordering Guide 101

5/13—Rev. E to Rev. F

Changes to Figure 1 1
Added Figure 2 to Figure 10; Renumbered Sequentially 4
Changes to Figure 19; Added Figure 20 21
Changes to EPAD Note in Figure 21 and Figure 22 22
Changes to EPAD Note in Table 11 23
Changes to EPAD Note in Figure 23 25
Changes to EPAD Note in Table 12 26
Changes to Table 14 31
Changes to Table 15 33
Changes to Table 82 68
Added Table 83, Figure 73, Figure 74, Following Text, and Table 84; Renumbered Sequentially 69
Changes to Bit 2 Description, Table 98 71
Changes to Table 101 72
Changes to Timer2 (Wake-Up Timer) Section 87
Changes to Figure 94 95
Updated Outline Dimensions 97
Changes to Ordering Guide 101

7/12—Rev. D to Rev. E

Changed SCLOCK to SCLK When Refering to SPI Clock, SPIMISO to MISO when Refering to SPI MISO, SPIMOSI to MOSI when Refering to SPI MOSI, and SPICSL to $\overline{CS}$ when Refering to SPI Chip Select ..... Universal
Changes to Table 4, Table 5, and Figure 5 11
Changes to Endnote 1 in Table 6 and Figure 6 12
Changes to Table 7 and Figure 7 13
Changes to Table 8 and Figure 8 14
Changes to Table 9 and Figure 9 15
Changed EPAD Note in Figure 12 and Table 11 18
Changed EPAD Note in Figure 13 and Table 12 21
Changes to Bit 6 in Table 18 43
Changes to Example Source Code (External Crystal Selection) Section and Example Source Code (External Clock Selection) Section 55
Changes to Serial Peripheral Interface Section 69
Changes to SPICON[10] and SPICON[9] Descriptions in Table 123 70
Changes to Timer Interval Down Equation and Added Timer Interval Up Equation 79
Added Hour:Minute:Second:1/128 Format Section 80
Changes to Table 189 84
Removed CP-40-10 Package 92
Changes to Ordering Guide 96

5/11—Rev. C to Rev. D

Changes to Table 4 11
Changes to Table 105 67
Updated Outline Dimensions 91
Changes to Ordering Guide 94

12/09—Rev. B to Rev. C

Added ADuC7029 Part ..... Universal
Added Table Numbers and Renumbered Tables ..... Universal
Changes to Figure Numbers ..... Universal
Changes to Table 1 6
Changes to Figure 3 9
Changes to Table 3 and Figure 4 10
Changes to Table 10 16
Changes to Figure 55 53
Changes to Serial Peripheral Interface Section 69
Changes to Table 137 73
Changes to Figure 71 and Figure 72 85
Changes to Figure 73 and Figure 74 86
Updated Outline Dimensions 91
Changes to Ordering Guide 94

3/07—Rev. A to Rev. B

Added ADuC7028 Part ..... Universal
Updated Format ..... Universal
Changes to Figure 2 5
Changes to Table 1 6
Changes to ADuC7026/ADuC7027 Section 23
Changes to Figure 21 28
Changes to Figure 32 Caption 30
Changes to Table 14 35
Changes to ADC Circuit Overview Section 38
Changes to Programming Section 44
Changes to Flash/EE Control Interface Section 45
Changes to Table 24 47
Changes to RSTCLR Register Section 48
Changes to Figure 52 49
Changes to Figure 53 50
Changes to Comparator Section 50
Changes to Oscillator and PLL—Power Control Section 51
Changes to Digital Peripherals Section 54
Changes to Interrupt System Section 75
Changes to Timers Section 76
Changes to External Memory Interfacing Section 80
Added IOV_{DD} Supply Sensitivity Section 84
Changes to Ordering Guide 90

1/06—Rev. 0 to Rev. A

Changes to Table 1 6
Added the Flash/EE Memory Reliability Section 43
Changes to Table 30 52
Changes to Serial Peripheral Interface 66
Changes to Ordering Guide 90

10/05—Revision 0: Initial Version

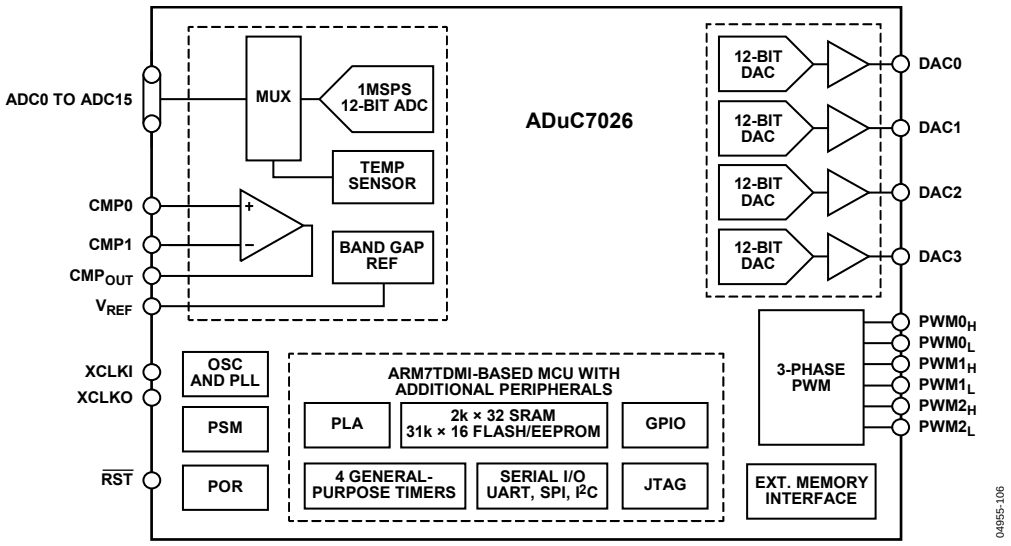


Figure 7.

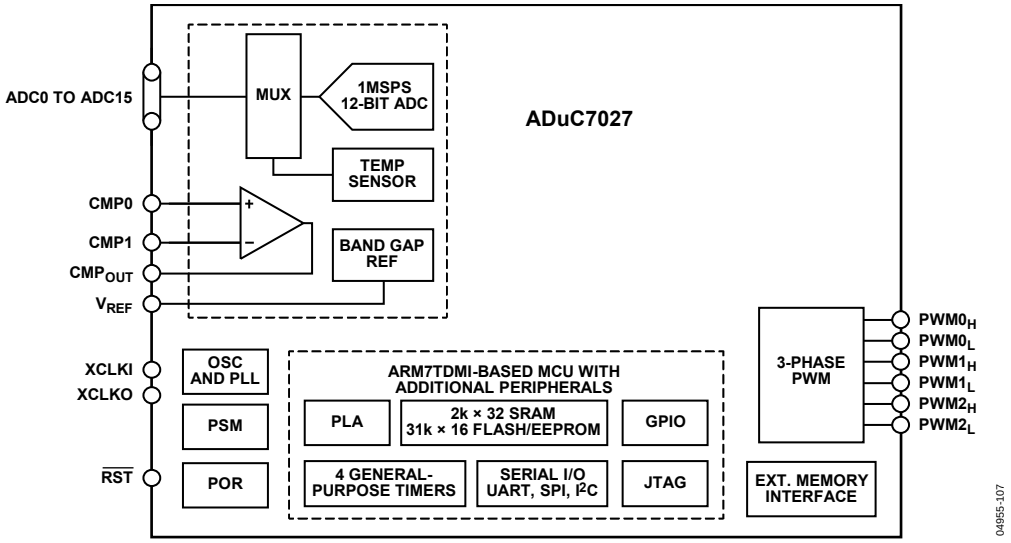


Figure 8.

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2	±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise (PHSN)		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			V_{CM}[6] ± V_{REF}/2	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±5	mV	T_A = 25°C
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		70		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					R_L = 5 kΩ, C_L = 100 pF
DC Accuracy[7]					
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range_0		0 to DAC_{REF}		V	DAC_{REF} range: DACGND to $DACV_{DD}$
Output Voltage Range_1		0 to 2.5		V	
Output Voltage Range_2		0 to $DACV_{DD}$		V	
Output Impedance		2		Ω	

ABSOLUTE MAXIMUM RATINGS

AGND = REFGND = DACGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
40-Lead LFCSP	26°C/W
49-Ball CSP_BGA	80°C/W
64-Lead LFCSP	24°C/W
64-Ball CSP_BGA	75°C/W
64-Lead LQFP	47°C/W
80-Lead LQFP	38°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

ADuC7019/ADuC7020/ADuC7021/ADuC7022

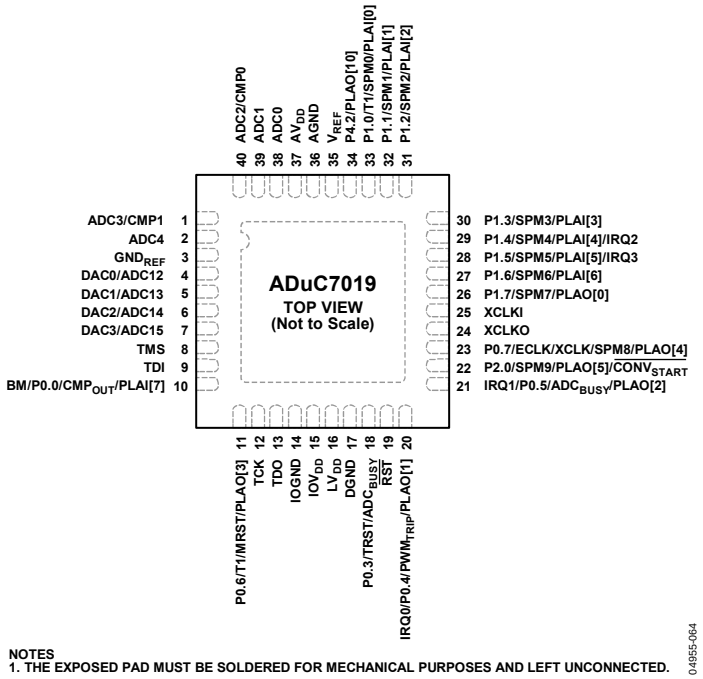


Figure 19. 40-Lead LFCSP_WQ Pin Configuration (ADuC7019)

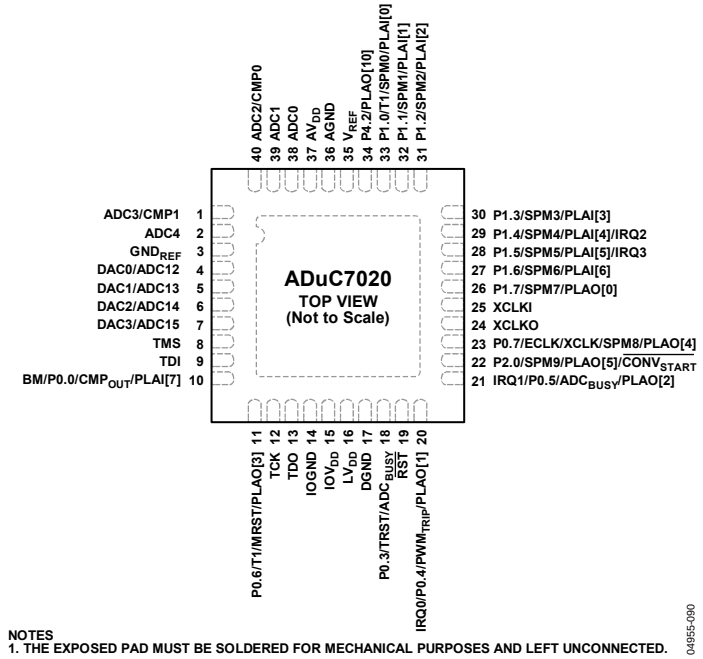
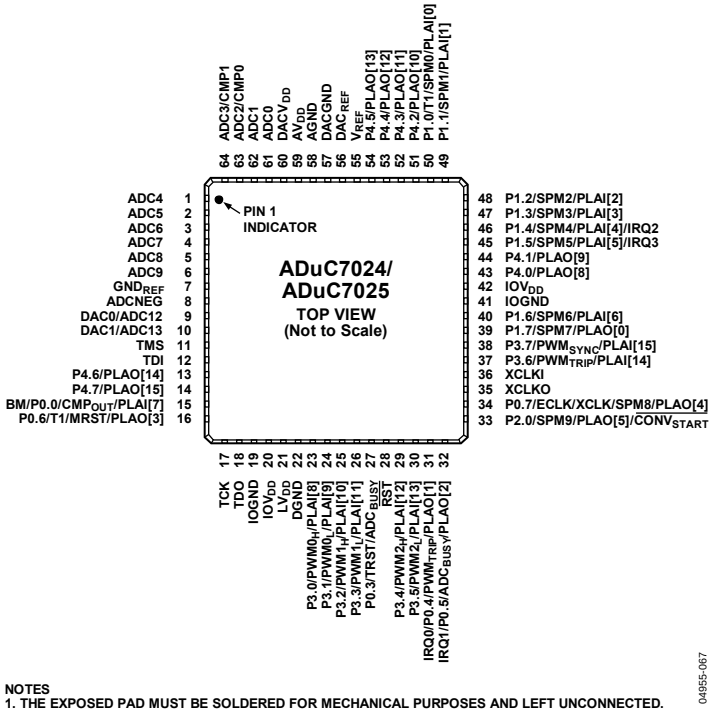


Figure 20. 40-Lead LFCSP_WQ Pin Configuration (ADuC7020)

ADuC7024/ADuC7025



NOTES
1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

Figure 23. 64-Lead LFCSP_VQ Pin Configuration (ADuC7024/ADuC7025)

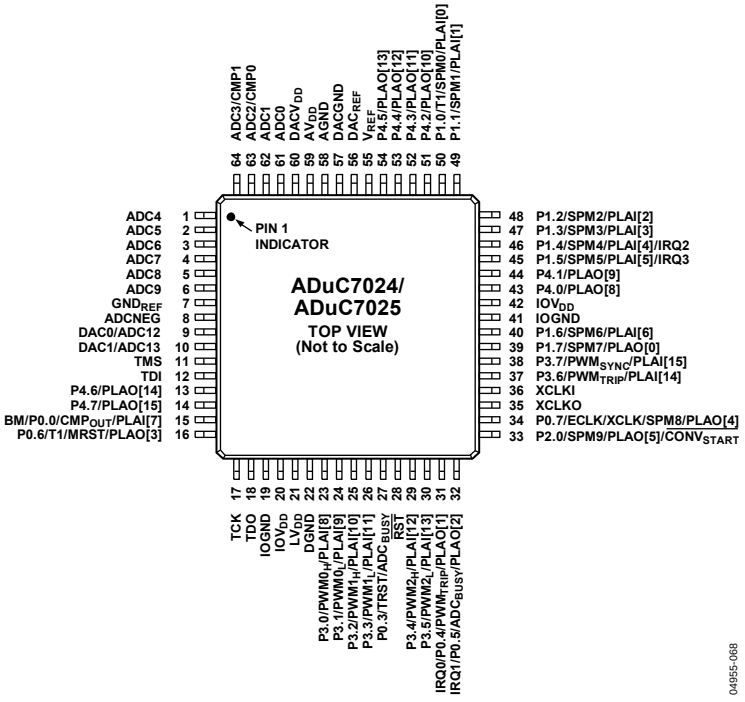


Figure 24. 64-Lead LQFP Pin Configuration (ADuC7024/ADuC7025)

ADUC7029

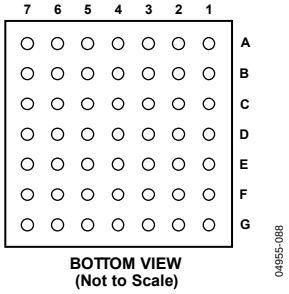


Figure 27. 49-Ball CSP_BGA Pin Configuration (ADuC7029)

Table 15. Pin Function Descriptions (ADuC7029)

Pin No.	Mnemonic	Description
A1	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
A2	ADC1	Single-Ended or Differential Analog Input 1.
A3	ADC0	Single-Ended or Differential Analog Input 0.
A4	AV_{DD}	3.3 V Analog Power.
A5	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
A6	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
A7	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
B1	ADC6	Single-Ended or Differential Analog Input 6.
B2	ADC5	Single-Ended or Differential Analog Input 5.
B3	ADC4	Single-Ended or Differential Analog Input 4.
B4	AGND	Analog Ground. Ground reference point for the analog circuitry.
B5	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
B6	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
B7	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
C1	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
C2	AGND	Analog Ground. Ground reference point for the analog circuitry.
C3	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
C4	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
C5	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
C6	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
C7	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
D1	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
D2	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
D3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
D4	$P3.3/PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
D5	$P3.4/PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
D6	$P3.6/PWM_{TRIP}$/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
D7	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.

TYPICAL PERFORMANCE CHARACTERISTICS

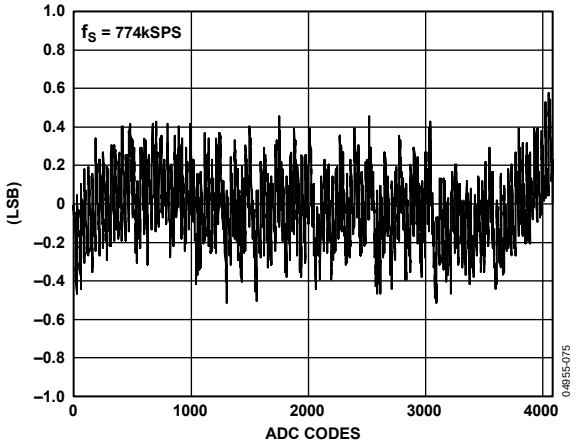


Figure 28. Typical INL Error, f_S = 774 kSPS

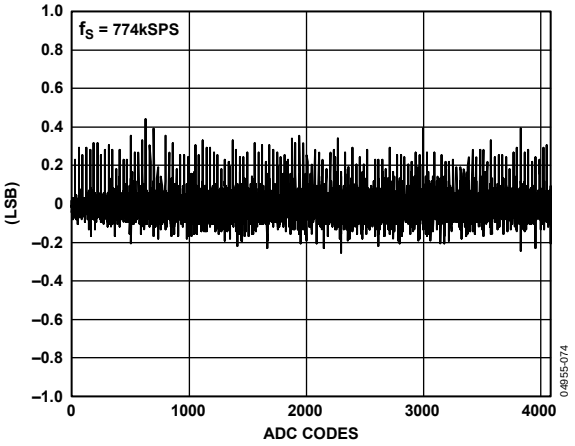


Figure 31. Typical DNL Error, f_S = 774 kSPS

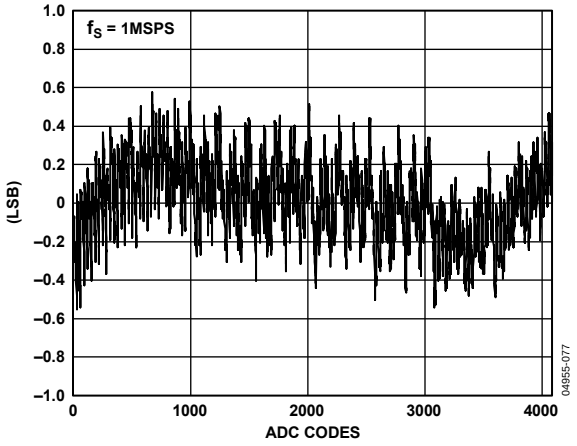


Figure 29. Typical INL Error, f_S = 1 MSPS

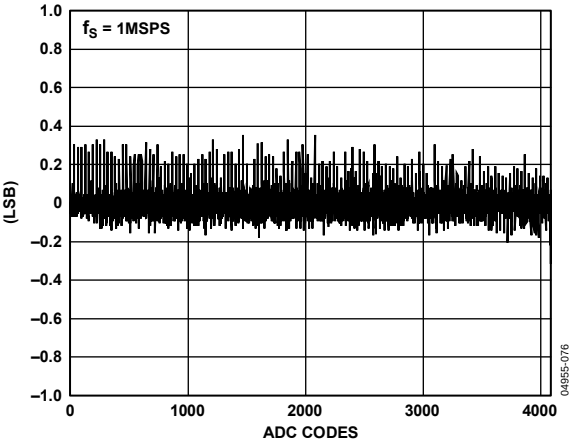


Figure 32. Typical DNL Error, f_S = 1 MSPS

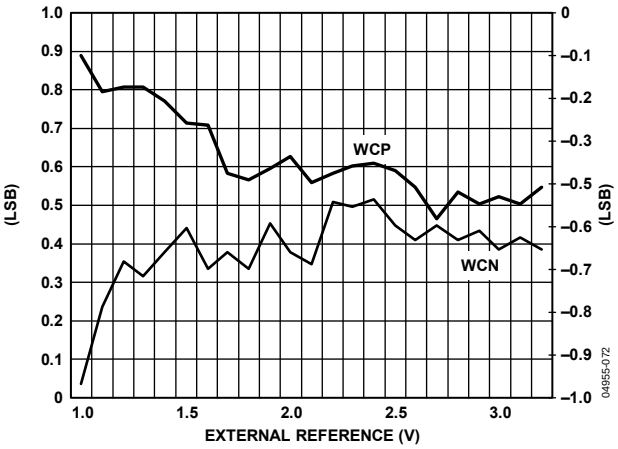


Figure 30. Typical Worst-Case (Positive (WCP) and Negative (WCN)) INL Error vs. V_{REF}, f_S = 774 kSPS

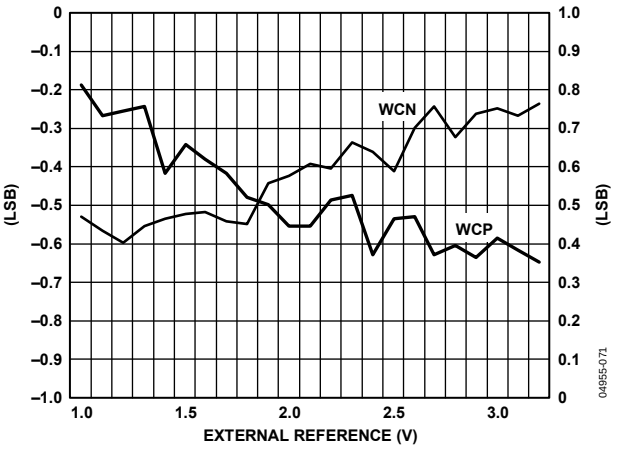


Figure 33. Typical Worst-Case (Positive (WCP)and Negative (WCN)) DNL Error vs. V_{REF}, f_S = 774 kSPS

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity (INL)
The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, +½ LSB.

Gain Error
The deviation of the last code transition from the ideal AIN voltage (full scale − 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio (SINAD)
The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy
Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time
The amount of time it takes the output to settle to within a 1 LSB level for a full-scale input change.

Address	Name	Byte	Access Type	Default Value	Page
Reference Address Base = 0xFFFF0480					
0x048C	REFCON	1	R/W	0x00	50
ADC Address Base = 0xFFFF0500					
0x0500	ADCCON	2	R/W	0x0600	46
0x0504	ADCCP	1	R/W	0x00	47
0x0508	ADCCN	1	R/W	0x01	47
0x050C	ADCSTA	1	R	0x00	48
0x0510	ADCDAT	4	R	0x00000000	48
0x0514	ADCRST	1	R/W	0x00	48
0x0530	ADCGN	2	R/W	0x0200	48
0x0534	ADCOF	2	R/W	0x0200	48
DAC Address Base = 0xFFFF0600					
0x0600	DAC0CON	1	R/W	0x00	56
0x0604	DAC0DAT	4	R/W	0x00000000	56
0x0608	DAC1CON	1	R/W	0x00	56
0x060C	DAC1DAT	4	R/W	0x00000000	56
0x0610	DAC2CON	1	R/W	0x00	56
0x0614	DAC2DAT	4	R/W	0x00000000	56
0x0618	DAC3CON	1	R/W	0x00	56
0x061C	DAC3DAT	4	R/W	0x00000000	56
UART Base Address = 0xFFFF0700					
0x0700	COMTX	1	R/W	0x00	71
	COMRX	1	R	0x00	71
	COMDIV0	1	R/W	0x00	71
0x0704	COMIEN0	1	R/W	0x00	71
	COMDIV1	1	R/W	0x00	72
0x0708	COMIID0	1	R	0x01	72
0x070C	COMCON0	1	R/W	0x00	72
0x0710	COMCON1	1	R/W	0x00	72
0x0714	COMSTA0	1	R	0x60	72
0x0718	COMSTA1	1	R	0x00	73
0x071C	COMSCR	1	R/W	0x00	73
0x0720	COMIEN1	1	R/W	0x04	73
0x0724	COMIID1	1	R	0x01	73
0x0728	COMADR	1	R/W	0xAA	74
0x072C	COMDIV2	2	R/W	0x0000	73

Address	Name	Byte	Access Type	Default Value	Page
I2C0 Base Address = 0xFFFF0800					
0x0800	I2C0MSTA	1	R/W	0x00	76
0x0804	I2C0SSTA	1	R	0x01	76
0x0808	I2C0SRX	1	R	0x00	77
0x080C	I2C0STX	1	W	0x00	77
0x0810	I2C0MRX	1	R	0x00	77
0x0814	I2C0MTX	1	W	0x00	77
0x0818	I2C0CNT	1	R/W	0x00	77
0x081C	I2C0ADR	1	R/W	0x00	77
0x0824	I2C0BYTE	1	R/W	0x00	77
0x0828	I2C0ALT	1	R/W	0x00	78
0x082C	I2C0CFG	1	R/W	0x00	78
0x0830	I2C0DIV	2	R/W	0x1F1F	79
0x0838	I2C0ID0	1	R/W	0x00	79
0x083C	I2C0ID1	1	R/W	0x00	79
0x0840	I2C0ID2	1	R/W	0x00	79
0x0844	I2C0ID3	1	R/W	0x00	79
0x0848	I2C0CCNT	1	R/W	0x01	79
0x084C	I2C0FSTA	2	R/W	0x0000	79
I2C1 Base Address = 0xFFFF0900					
0x0900	I2C1MSTA	1	R/W	0x00	76
0x0904	I2C1SSTA	1	R	0x01	76
0x0908	I2C1SRX	1	R	0x00	77
0x090C	I2C1STX	1	W	0x00	77
0x0910	I2C1MRX	1	R	0x00	77
0x0914	I2C1MTX	1	W	0x00	77
0x0918	I2C1CNT	1	R/W	0x00	77
0x091C	I2C1ADR	1	R/W	0x00	77
0x0924	I2C1BYTE	1	R/W	0x00	77
0x0928	I2C1ALT	1	R/W	0x00	78
0x092C	I2C1CFG	1	R/W	0x00	78
0x0930	I2C1DIV	2	R/W	0x1F1F	79
0x0938	I2C1ID0	1	R/W	0x00	79
0x093C	I2C1ID1	1	R/W	0x00	79
0x0940	I2C1ID2	1	R/W	0x00	79
0x0944	I2C1ID3	1	R/W	0x00	79
0x0948	I2C1CCNT	1	R/W	0x01	79
0x094C	I2C1FSTA	2	R/W	0x0000	79
SPI Base Address = 0xFFFF0A00					
0x0A00	SPISTA	1	R	0x00	75
0x0A04	SPIRX	1	R	0x00	75
0x0A08	SPITX	1	W	0x00	75
0x0A0C	SPIDIV	1	R/W	0x1B	75
0x0A10	SPICON	2	R/W	0x0000	75

TYPICAL OPERATION

Once configured via the ADC control and channel selection registers, the ADC converts the analog input and provides a 12-bit result in the ADC data register.

The top four bits are the sign bits. The 12-bit result is placed from Bit 16 to Bit 27, as shown in Figure 51. Again, it should be noted that, in fully differential mode, the result is represented in twos complement format. In pseudo differential and single-ended modes, the result is represented in straight binary format.

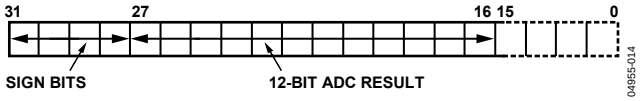


Figure 51. ADC Result Format

The same format is used in DACxDAT, simplifying the software.

Current Consumption

The ADC in standby mode, that is, powered up but not converting, typically consumes 640 μA. The internal reference adds 140 μA. During conversion, the extra current is 0.3 μA multiplied by the sampling frequency (in kilohertz (kHz)). Figure 43 shows the current consumption vs. the sampling frequency of the ADC.

Timing

Figure 52 gives details of the ADC timing. Users control the ADC clock speed and the number of acquisition clocks in the ADCCON MMR. By default, the acquisition time is eight clocks and the clock divider is 2. The number of extra clocks (such as bit trial or write) is set to 19, which gives a sampling rate of 774 kSPS. For conversion on the temperature sensor, the ADC acquisition time is automatically set to 16 clocks, and the ADC clock divider is set to 32. When using multiple channels, including the temperature sensor, the timing settings revert to the user-defined settings after reading the temperature sensor channel.

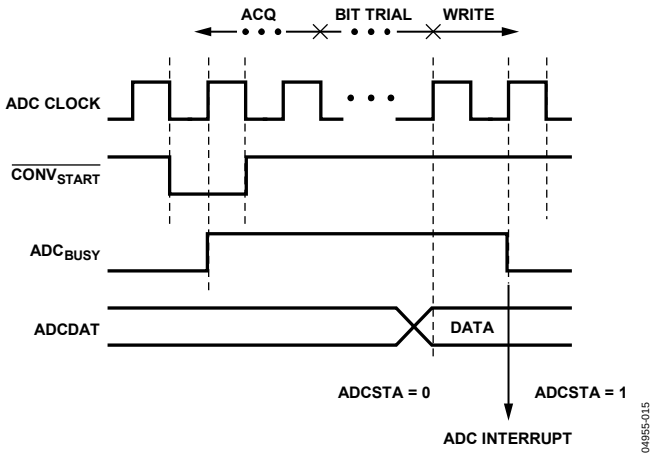


Figure 52. ADC Timing

ADuC7019

The ADuC7019 is identical to the ADuC7020 except for one buffered ADC channel, ADC3, and it has only three DACs. The output buffer of the fourth DAC is internally connected to the ADC3 channel as shown in Figure 53.

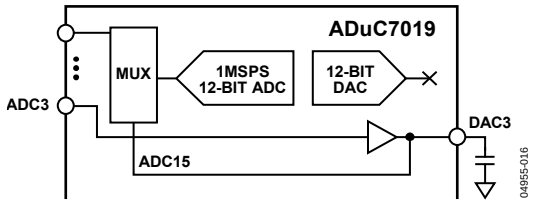


Figure 53. ADC3 Buffered Input

Note that the DAC3 output pin must be connected to a 10 nF capacitor to AGND. This channel should be used to measure dc voltages only. ADC calibration may be necessary on this channel.

MMRS INTERFACE

The ADC is controlled and configured via the eight MMRs described in this section.

Table 17. ADCCON Register

Name	Address	Default Value	Access
ADCCON	0xFFFF0500	0x0600	R/W

ADCCON is an ADC control register that allows the programmer to enable the ADC peripheral, select the mode of operation of the ADC (in single-ended mode, pseudo differential mode, or fully differential mode), and select the conversion type. This MMR is described in Table 18.

Table 28. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads 4094 to 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7019/20/21/22/24/25/26/27/28/29 provide voltage output from on-chip band gap references proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The following is an example routine showing how to use the internal temperature sensor:

```
int main(void)
{
float a = 0;
      short b;
      ADCCON = 0x20;    // power-on the ADC
      delay(2000);
      ADCCP = 0x10;  // Select Temperature
Sensor as an // input to the ADC
      REFCON = 0x01; // connect internal 2.5V
reference // to Vref pin
      ADCCON = 0xE4; // continuous conversion
      while(1)
      {
              while (!ADCSTA){};
      // wait for end of conversion
              b = (ADCDAT >> 16);
      // To calculate temperature in °C, use
the formula:
              a = 0x525 - b;
      // ((Temperature = 0x525 - Sensor
Voltage) / 1.3)
              a /= 1.3;
              b = floor(a);
              printf("Temperature: %d
oC\n",b);
      }
      return 0;
}
```

BAND GAP REFERENCE

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides an on-chip band gap reference of 2.5 V, which can be used for the ADC and DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (V_{REF}) and used as a reference for other circuits in the system. An external buffer is required because of the low drive capability of the V_{REF} output. A programmable option also allows an external reference input on the V_{REF} pin. Note that it is not possible to disable the internal reference. Therefore, the external reference source must be capable of overdriving the internal reference source.

Table 29. REFCON Register

Name	Address	Default Value	Access
REFCON	0xFFFF048C	0x00	R/W

The band gap reference interface consists of an 8-bit MMR REFCON, described in Table 30.

Table 30. REFCON MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Internal reference output enable. Set by user to connect the internal 2.5 V reference to the V_{REF} pin. The reference can be used for an external component but must be buffered. Cleared by user to disconnect the reference from the V_{REF} pin.

Both switching edges are moved by an equal amount (PWMDAT1 × t_{CORE}) to preserve the symmetrical output patterns.

Also shown are the PWMSYNC pulse and Bit 0 of the PWMSTA register, which indicates whether operation is in the first or second half cycle of the PWM period.

The resulting on times of the PWM signals over the full PWM period (two half periods) produced by the timing unit can be written as follows:

On the high side

$$t_{0HH} = PWMDAT0 + 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

$$t_{0HL} = PWMDAT0 - 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (*d*)

$$d_{0H} = t_{0HH}/t_S = ½ + (PWMCH0 - PWMDAT1)/PWMDAT0$$

and on the low side

$$t_{0LH} = PWMDAT0 - 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

$$t_{0LL} = PWMDAT0 + 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (*d*)

$$d_{OL} = t_{0LH}/t_S = ½ - (PWMCH0 + PWMDAT1)/PWMDAT0$$

The minimum permissible t_{0H} and t_{0L} values are zero, corresponding to a 0% duty cycle. In a similar fashion, the maximum value is t_S, corresponding to a 100% duty cycle.

Figure 70 shows the output signals from the timing unit for operation in double update mode. It illustrates a general case where the switching frequency, dead time, and duty cycle are all changed in the second half of the PWM period. The same value for any or all of these quantities can be used in both halves of the PWM cycle. However, there is no guarantee that symmetrical PWM signals are produced by the timing unit in double update mode. Figure 70 also shows that the dead time insertions into the PWM signals are done in the same way as in single update mode.

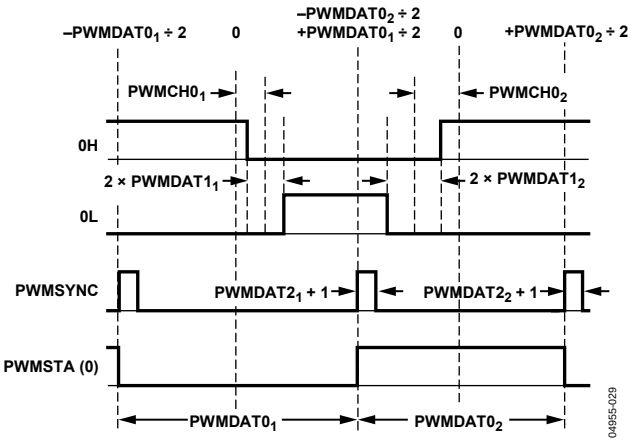


Figure 70. Typical PWM Outputs of the 3-Phase Timing Unit (Double Update Mode)

In general, the on times of the PWM signals in double update mode can be defined as follows:

On the high side

$$t_{0HH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

$$t_{0HL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (*d*) are

$$d_{0H} = t_{0HH}/t_S = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

On the low side

$$t_{0LH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

$$t_{0LL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (d) are

$$d_{0L} = t_{0LH}/t_S = (\text{PWMDAT0}_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

For the completely general case in double update mode (see Figure 70), the switching period is given by

$$t_S = (PWMDAT0_1 + PWMDAT0_2) \times t_{CORE}$$

Again, the values of t_{0H} and t_{0L} are constrained to lie between zero and t_S.

PWM signals similar to those illustrated in Figure 69 and Figure 70 can be produced on the 1H, 1L, 2H, and 2L outputs by programming the PWMCH1 and PWMCH2 registers in a manner identical to that described for PWMCH0. The PWM controller does not produce any PWM outputs until all of the PWMDAT0, PWMCH0, PWMCH1, and PWMCH2 registers have been written to at least once. When these registers are written, internal counting of the timers in the 3-phase timing unit is enabled.

Writing to the PWMDAT0 register starts the internal timing of the main PWM timer. Provided that the PWMDAT0 register is written to prior to the PWMCH0, PWMCH1, and PWMCH2 registers in the initialization, the first PWMSYNC pulse and interrupt (if enabled) appear 1.5 × t_{CORE} × PWMDAT0 seconds after the initial write to the PWMDAT0 register in single update mode. In double update mode, the first PWMSYNC pulse appears after PWMDAT0 × t_{CORE} seconds.

Table 85. GPxDAT Registers

Name	Address	Default Value[1]	Access
GP0DAT	0xFFFFF420	0x000000XX	R/W
GP1DAT	0xFFFFF430	0x000000XX	R/W
GP2DAT	0xFFFFF440	0x000000XX	R/W
GP3DAT	0xFFFFF450	0x000000XX	R/W
GP4DAT	0xFFFFF460	0x000000XX	R/W

[1] X = 0, 1, 2, or 3.

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins configured as output, and store the input value of the pins configured as input.

Table 86. GPxDAT MMR Bit Descriptions

Bit	Description
31:24	Direction of the data. Set to 1 by user to configure the GPIO pin as an output. Cleared to 0 by user to configure the GPIO pin as an input.
23:16	Port x data output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x data input (read only).

Table 87. GPxSET Registers

Name	Address	Default Value[1]	Access
GP0SET	0xFFFFF424	0x000000XX	W
GP1SET	0xFFFFF434	0x000000XX	W
GP2SET	0xFFFFF444	0x000000XX	W
GP3SET	0xFFFFF454	0x000000XX	W
GP4SET	0xFFFFF464	0x000000XX	W

[1] X = 0, 1, 2, or 3.

GPxSET are data set Port x registers.

Table 88. GPxSET MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x set bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

Table 89. GPxCLR Registers

Name	Address	Default Value[1]	Access
GP0CLR	0xFFFFF428	0x000000XX	W
GP1CLR	0xFFFFF438	0x000000XX	W
GP2CLR	0xFFFFF448	0x000000XX	W
GP3CLR	0xFFFFF458	0x000000XX	W
GP4CLR	0xFFFFF468	0x000000XX	W

[1] X = 0, 1, 2, or 3.

GPxCLR are data clear Port x registers.

Table 90. GPxCLR MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x clear bit. Set to 1 by user to clear bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

SERIAL PORT MUX

The serial port mux multiplexes the serial port peripherals (an SPI, UART, and two I^2Cs) and the programmable logic array (PLA) to a set of 10 GPIO pins. Each pin must be configured to one of its specific I/O functions as described in Table 91.

Table 91. SPM Configuration

SPMMUX	GPIO (00)	UART (01)	UART/I^2C/SPI (10)	PLA (11)
SPM0	P1.0	SIN	I2C0SCL	PLAI[0]
SPM1	P1.1	SOUT	I2C0SDA	PLAI[1]
SPM2	P1.2	RTS	I2C1SCL	PLAI[2]
SPM3	P1.3	CTS	I2C1SDA	PLAI[3]
SPM4	P1.4	RI	SCLK	PLAI[4]
SPM5	P1.5	DCD	MISO	PLAI[5]
SPM6	P1.6	DSR	MOSI	PLAI[6]
SPM7	P1.7	DTR	$\overline{CS}$	PLAO[0]
SPM8	P0.7	ECLK/XCLK	SIN	PLAO[4]
SPM9	P2.0	CONV	SOUT	PLAO[5]

Table 91 also details the mode for each of the SPMMUX pins. This configuration must be done via the GP0CON, GP1CON, and GP2CON MMRs. By default, these 10 pins are configured as GPIOs.

UART SERIAL INTERFACE

The UART peripheral is a full-duplex, universal, asynchronous receiver/transmitter. It is fully compatible with the 16,450 serial port standard. The UART performs serial-to-parallel conversions on data characters received from a peripheral device or modem, and parallel-to-serial conversions on data characters received from the CPU. The UART includes a fractional divider for baud rate generation and has a network addressable mode. The UART function is made available on the 10 pins of the ADuC7019/20/21/22/24/25/26/27/28/29 (see Table 92).

Table 92. UART Signal Description

Pin	Signal	Description
SPM0 (Mode 1)	SIN	Serial receive data.
SPM1 (Mode 1)	SOUT	Serial transmit data.
SPM2 (Mode 1)	RTS	Request to send.
SPM3 (Mode 1)	CTS	Clear to send.
SPM4 (Mode 1)	RI	Ring indicator.
SPM5 (Mode 1)	DCD	Data carrier detect.
SPM6 (Mode 1)	DSR	Data set ready.
SPM7 (Mode 1)	DTR	Data terminal ready.
SPM8 (Mode 2)	SIN	Serial receive data.
SPM9 (Mode 2)	SOUT	Serial transmit data.

Table 140. I2CxDIV Registers

Name	Address	Default Value	Access
I2C0DIV	0xFFFF0830	0x1F1F	R/W
I2C1DIV	0xFFFF0930	0x1F1F	R/W

I2CxDIV are the clock divider registers.

Table 141. I2CxIDx Registers

Name	Address	Default Value	Access
I2C0ID0	0xFFFF0838	0x00	R/W
I2C0ID1	0xFFFF083C	0x00	R/W
I2C0ID2	0xFFFF0840	0x00	R/W
I2C0ID3	0xFFFF0844	0x00	R/W
I2C1ID0	0xFFFF0938	0x00	R/W
I2C1ID1	0xFFFF093C	0x00	R/W
I2C1ID2	0xFFFF0940	0x00	R/W
I2C1ID3	0xFFFF0944	0x00	R/W

I2CxID0, I2CxID1, I2CxID2, and I2CxID3 are slave address device ID registers of I2Cx.

Table 142. I2CxCCNT Registers

Name	Address	Default Value	Access
I2C0CCNT	0xFFFF0848	0x01	R/W
I2C1CCNT	0xFFFF0948	0x01	R/W

I2CxCCNT are 8-bit start/stop generation counters. They hold off SDA low for start and stop conditions.

Table 143. I2CxFSTA Registers

Name	Address	Default Value	Access
I2C0FSTA	0xFFFF084C	0x0000	R/W
I2C1FSTA	0xFFFF094C	0x0000	R/W

I2CxFSTA are FIFO status registers.

Table 144. I2C0FSTA MMR Bit Descriptions

Bit	Access Type	Value	Description
15:10			Reserved.
9	R/W		Master transmit FIFO flush. Set by the user to flush the master Tx FIFO. Cleared automatically when the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
8	R/W		Slave transmit FIFO flush. Set by the user to flush the slave Tx FIFO. Cleared automatically after the slave Tx FIFO is flushed.
7:6	R		Master Rx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
5:4	R		Master Tx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
3:2	R		Slave Rx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
1:0	R		Slave Tx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 23 interrupt sources on the ADuC7019/20/21/22/24/25/26/27/28/29 that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals, such as ADC and UART. Four additional interrupt sources are generated from external interrupt request pins, IRQ0, IRQ1, IRQ2, and IRQ3. The ARM7TDMI CPU core only recognizes interrupts as one of two types: a normal interrupt request IRQ or a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system are managed through nine interrupt-related registers, four dedicated to IRQ, and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ register (except for Bit 23) represent the same interrupt source as described in Table 160.

Table 160. IRQ/FIQ MMRs Bit Description

Bit	Description
0	All interrupts OR'ed (FIQ only)
1	SWI
2	Timer0
3	Timer1
4	Wake-up timer (Timer2)
5	Watchdog timer (Timer3)
6	Flash control
7	ADC channel
8	PLL lock
9	I2C0 slave
10	I2C0 master
11	I2C1 master
12	SPI slave
13	SPI master
14	UART
15	External IRQ0
16	Comparator
17	PSM
18	External IRQ1
19	PLA IRQ0
20	PLA IRQ1
21	External IRQ2
22	External IRQ3
23	PWM trip (IRQ only)/PWM sync (FIQ only)

IRQ

The interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It is used to service general-purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are IRQSTA, IRQSIG, IRQEN, and IRQCLR.

Table 161. IRQSTA Register

Name	Address	Default Value	Access
IRQSTA	0xFFFF0000	0x00000000	R

IRQSTA (read-only register) provides the current-enabled IRQ source status. When set to 1, that source should generate an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically OR'ed to create the IRQ signal to the ARM7TDMI core.

Table 162. IRQSIG Register

Name	Address	Default Value	Access
IRQSIG	0xFFFF0004	0x00XXX000[1]	R

[1] X indicates an undefined value.

IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read only.

Table 163. IRQEN Register

Name	Address	Default Value	Access
IRQEN	0xFFFF0008	0x00000000	R/W

IRQEN provides the value of the current enable mask. When each bit is set to 1, the source request is enabled to create an IRQ exception. When each bit is set to 0, the source request is disabled or masked, which does not create an IRQ exception.

Note that to clear an already enabled interrupt source, the user must set the appropriate bit in the IRQCLR register. Clearing an interrupt's IRQEN bit does not disable the interrupt.

Table 164. IRQCLR Register

Name	Address	Default Value	Access
IRQCLR	0xFFFF000C	0x00000000	W

IRQCLR (write-only register) clears the IRQEN register in order to mask an interrupt source. Each bit set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, independently manipulates the enable mask without requiring an atomic read-modify-write.

In normal mode, an IRQ is generated each time the value of the counter reaches zero when counting down. It is also generated each time the counter value reaches full scale when counting up. An IRQ can be cleared by writing any value to clear the register of that particular timer (TxCLRI).

When using an asynchronous clock-to-clock timer, the interrupt in the timer block may take more time to clear than the time it takes for the code in the interrupt routine to execute. Ensure that the interrupt signal is cleared before leaving the interrupt service routine. This can be done by checking the IRQSTA MMR.

Hour:Minute:Second:1/128 Format

To use the timer in hour:minute:second:hundredths format, select the 32,768 kHz clock and prescaler of 256. The hundredths field does not represent milliseconds but 1/128 of a second (256/32,768). The bits representing the hour, minute, and second are not consecutive in the register. This arrangement applies to TxLD and TxVAL when using the hour:minute:second:hundredths format as set in TxCON[5:4]. See Table 171 for additional details.

Table 171. Hour:Minnute:Second:Hundredths Format

Bit	Value	Description
31:24	0 to 23 or 0 to 255	Hours
23:22	0	Reserved
21:16	0 to 59	Minutes
15:14	0	Reserved
13.8	0 to 59	Seconds
7	0	Reserved
6:0	0 to 127	1/128 second

Timer0 (RTOS Timer)

Timer0 is a general-purpose, 16-bit timer (count down) with a programmable prescaler (see Figure 77). The prescaler source is the core clock frequency (HCLK) and can be scaled by factors of 1, 16, or 256.

Timer0 can be used to start ADC conversions as shown in the block diagram in Figure 77.

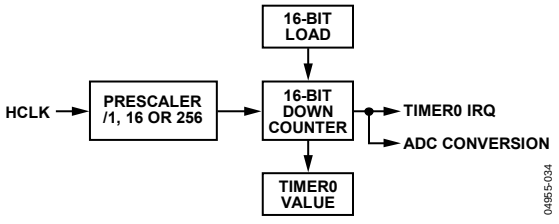


Figure 77. Timer0 Block Diagram

The Timer0 interface consists of four MMRs: T0LD, T0VAL, T0CON, and T0CLRI.

Table 172. T0LD Register

Name	Address	Default Value	Access
T0LD	0xFFFF0300	0x0000	R/W

T0LD is a 16-bit load register.

Table 173. T0VAL Register

Name	Address	Default Value	Access
T0VAL	0xFFFF0304	0xFFFF	R

T0VAL is a 16-bit read-only register representing the current state of the counter.

Table 174. T0CON Register

Name	Address	Default Value	Access
T0CON	0xFFFF0308	0x0000	R/W

T0CON is the configuration MMR described in Table 175.

Table 175. T0CON MMR Bit Descriptions

Bit	Value	Description
15:8		Reserved.
7		Timer0 enable bit. Set by user to enable Timer0. Cleared by user to disable Timer0 by default.
6		Timer0 mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode. Default mode.
5:4		Reserved.
3:2		Prescale.
	00	Core Clock/1. Default value.
	01	Core Clock/16.
	10	Core Clock/256.
	11	Undefined. Equivalent to 00.
1:0		Reserved.

Table 176. T0CLRI Register

Name	Address	Default Value	Access
T0CLRI	0xFFFF030C	0xFF	W

T0CLRI is an 8-bit register. Writing any value to this register clears the interrupt.

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the core clock frequency, or an external GPIO (P1.0 or P0.6). The maximum frequency of the clock input is 44 Mhz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 78.

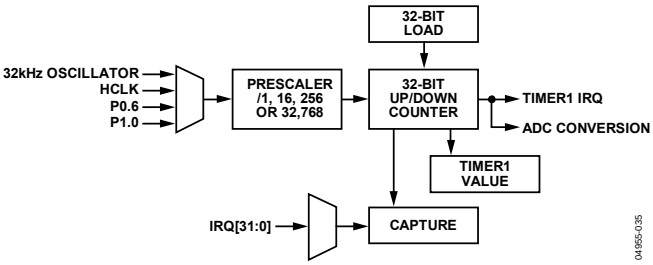


Figure 78. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

Table 177. T1LD Register

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000000	R/W

T1LD is a 32-bit load register.

Table 178. T1VAL Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0xFFFFFFFF	R

T1VAL is a 32-bit read-only register that represents the current state of the counter.

Table 179. T1CON Register

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

T1CON is the configuration MMR described in Table 180.

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7019/20/21/22/24/25/26/27/28/29 operational power supply voltage range is 2.7 V to 3.6 V. Separate analog and digital power supply pins (AV_{DD} and IOV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system IOV_{DD} line. In this mode, the part can also operate with split supplies; that is, it can use different voltage levels for each supply. For example, the system can be designed to operate with an IOV_{DD} voltage level of 3.3 V whereas the AV_{DD} level can be at 3 V or vice versa. A typical split supply configuration is shown in Figure 87.

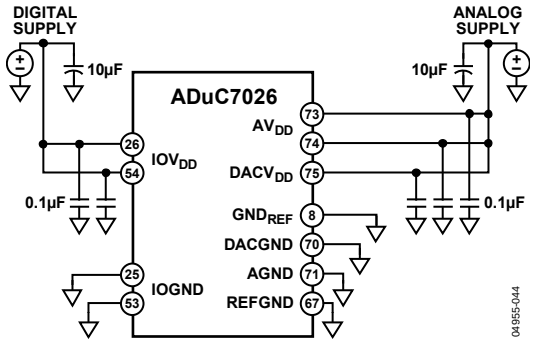


Figure 87. External Dual Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AV_{DD} by placing a small series resistor and/or ferrite bead between AV_{DD} and IOV_{DD} and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 88. With this configuration, other analog circuitry (such as op amps and voltage reference) can be powered from the AV_{DD} supply line as well.

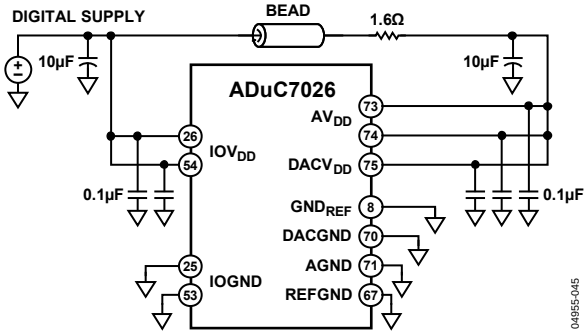


Figure 88. External Single Supply Connections

Note that in both Figure 87 and Figure 88, a large value (10 µF) reservoir capacitor sits on IOV_{DD}, and a separate 10 µF capacitor sits on AV_{DD}. In addition, local small-value (0.1 µF) capacitors are located at each AV_{DD} and IOV_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane.

Finally, note that the analog and digital ground pins on the ADuC7019/20/21/22/24/25/26/27/28/29 must be referenced to the same system ground reference point at all times.

IOV_{DD} Supply Sensitivity

The IOV_{DD} supply is sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature ensures that no flash interface timings or ARM7TDMI timings are violated.

Typically, frequency noise greater than 50 kHz and 50 mV p-p on top of the supply causes the core to stop working.

If decoupling values recommended in the Power Supplies section do not sufficiently dampen all noise sources below 50 mV on IOV_{DD}, a filter such as the one shown in Figure 89 is recommended.

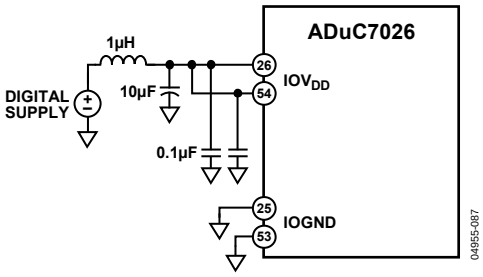


Figure 89. Recommended IOV_{DD} Supply Filter

Linear Voltage Regulator

Each ADuC7019/20/21/22/24/25/26/27/28/29 requires a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOV_{DD} for the core logic. The LV_{DD} pin is the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between LV_{DD} and DGND (as close as possible to these pins) to act as a tank of charge as shown in Figure 90.

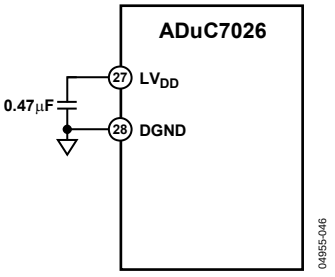


Figure 90. Voltage Regulator Connections

The LV_{DD} pin should not be used for any other chip. It is also recommended to use excellent power supply decoupling on IOV_{DD} to help improve line regulation performance of the on-chip voltage regulator.

Model[1, 2]	ADC Channels[3]	DAC Channels	FLASH/ RAM	GPIO	Down-loader	Temperature Range	Package Description	Package Option	Ordering Quantity
EVAL-ADuC7020MKZ							ADuC7020 MiniKit		
EVAL-ADuC7020QSZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7020QSPZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7024QSZ							ADuC7024 QuickStart Development System		
EVAL-ADuC7026QSZ							ADuC7026 QuickStar Development System		
EVAL-ADuC7026QSPZ							ADuC7026 QuickStart Plus Development System		
EVAL-ADuC7028QSZ							ADuC7028 QuickStart Development System		
EVAL-ADUC7029QSZ							ADuC7029 QuickStart Development System		

[1] Z = RoHS Compliant Part.
[2] Models ADuC7026 and ADuC7027 include an external memory interface.
[3] One of the ADC channels is internally buffered for ADuC7019 models.

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).