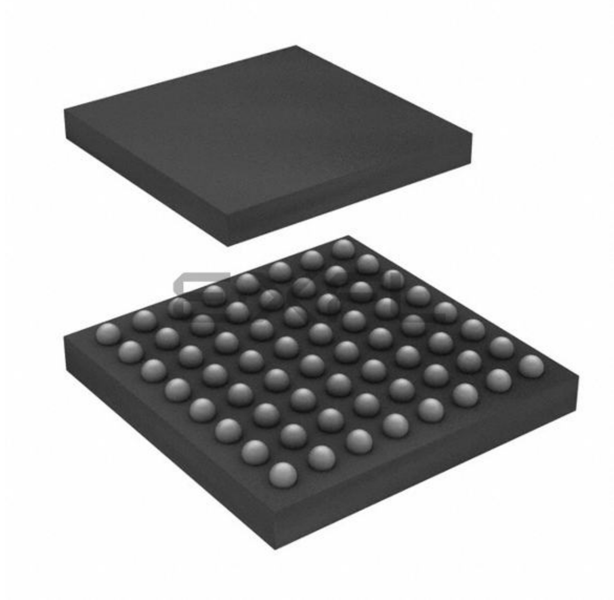

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	30
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA, CSPBGA
Supplier Device Package	64-CSPBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7028bbcz62-rl

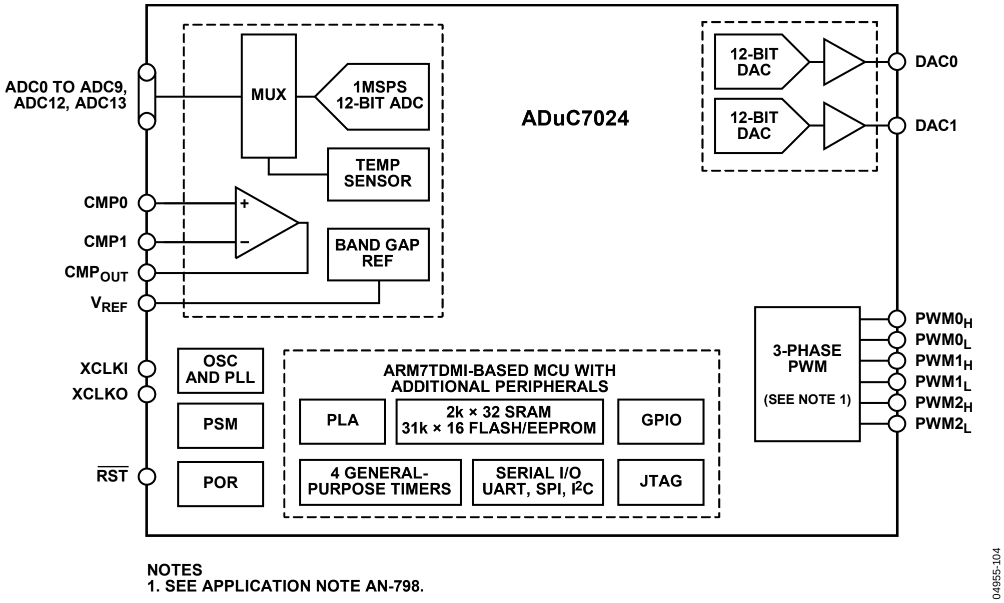

Figure 5.

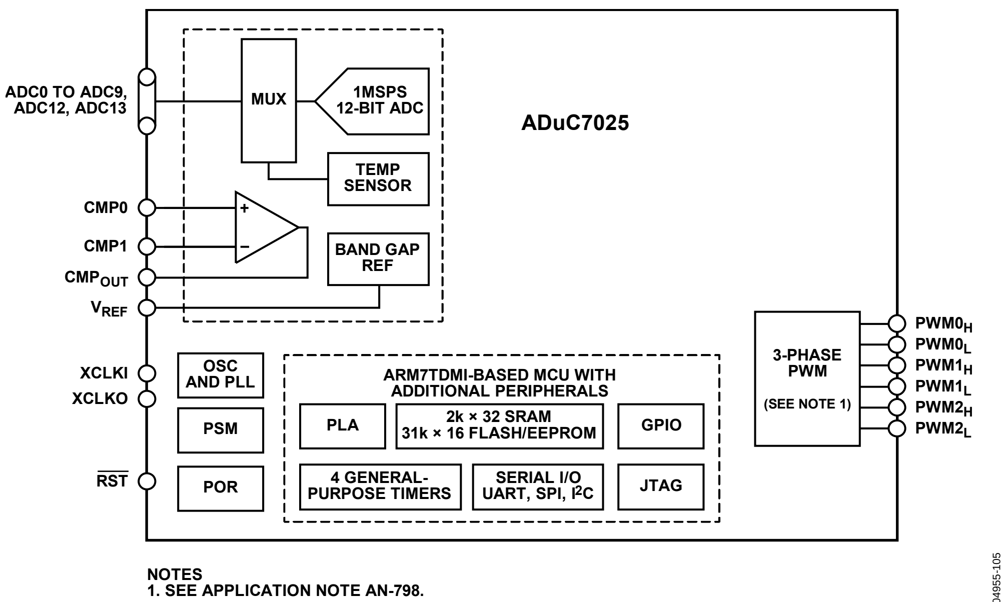

Figure 6.

Table 7. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

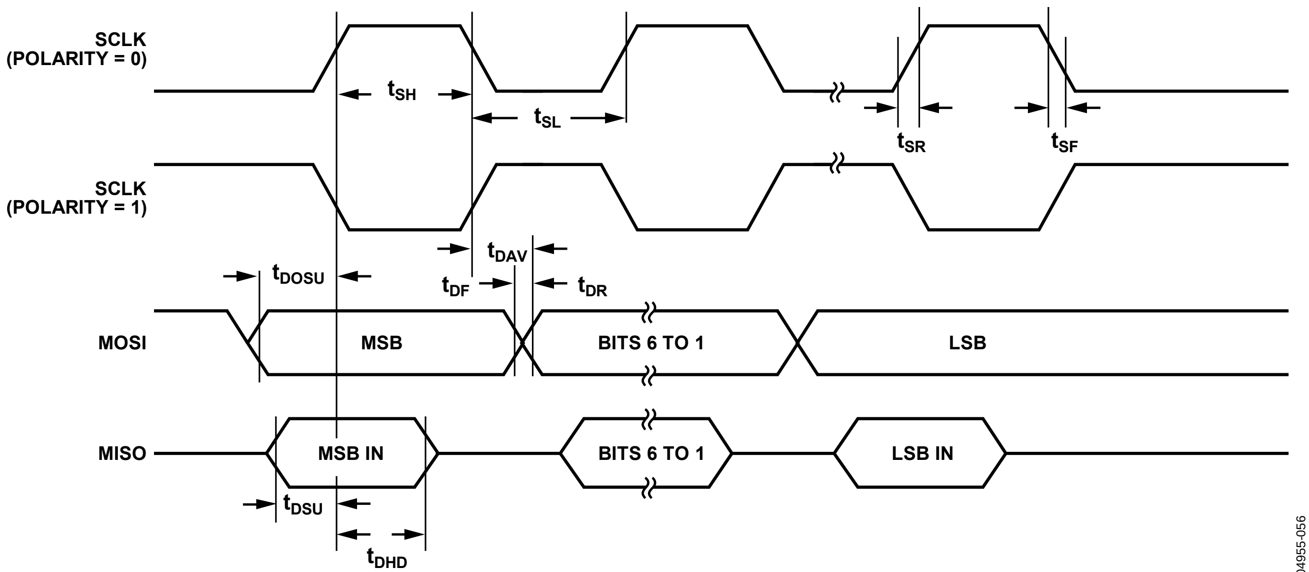

Figure 16. SPI Master Mode Timing (Phase Mode = 0)

Table 8. SPI Slave Mode Timing (Phsae Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.
[2] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

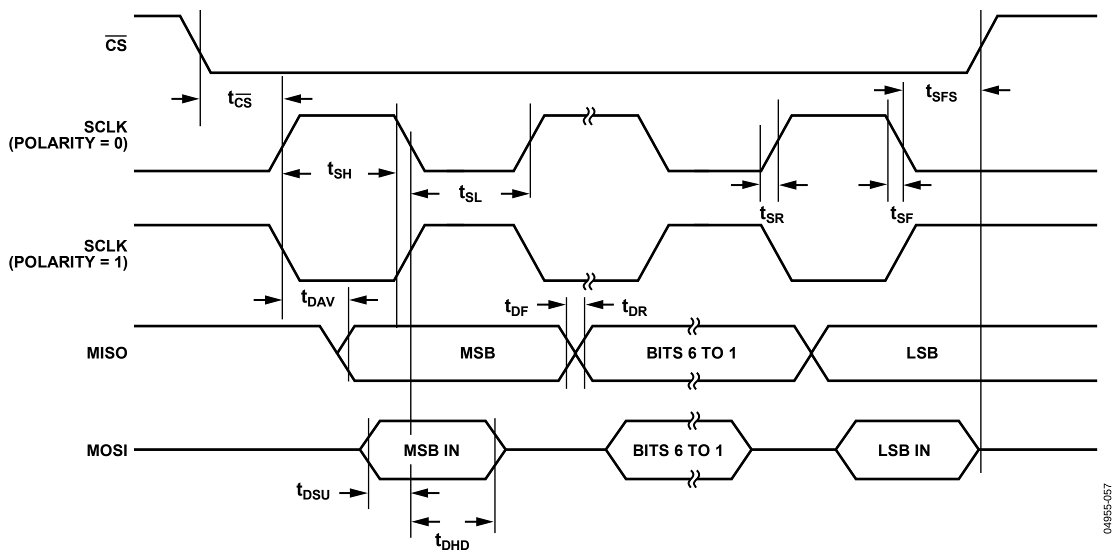

Figure 17. SPI Slave Mode Timing (Phase Mode = 1)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

ADuC7019/ADuC7020/ADuC7021/ADuC7022

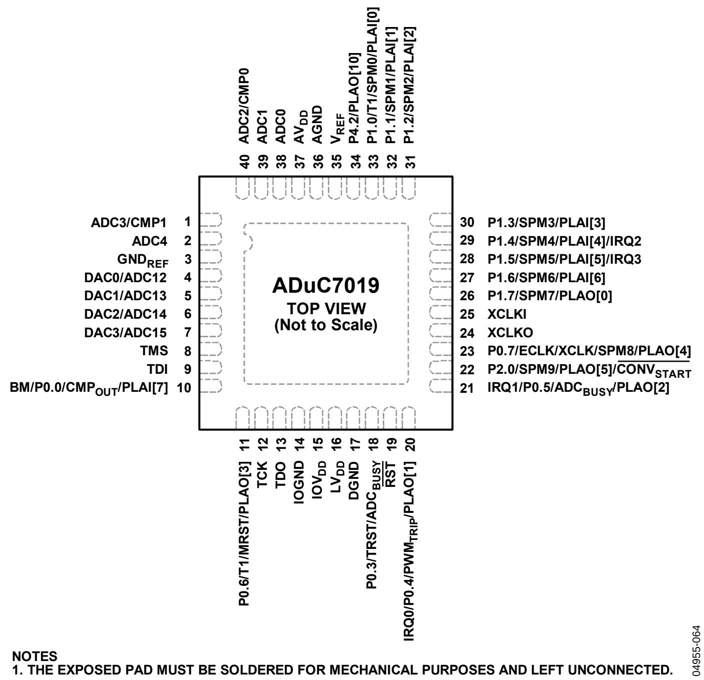

Figure 19. 40-Lead LFCSP_WQ Pin Configuration (ADuC7019)

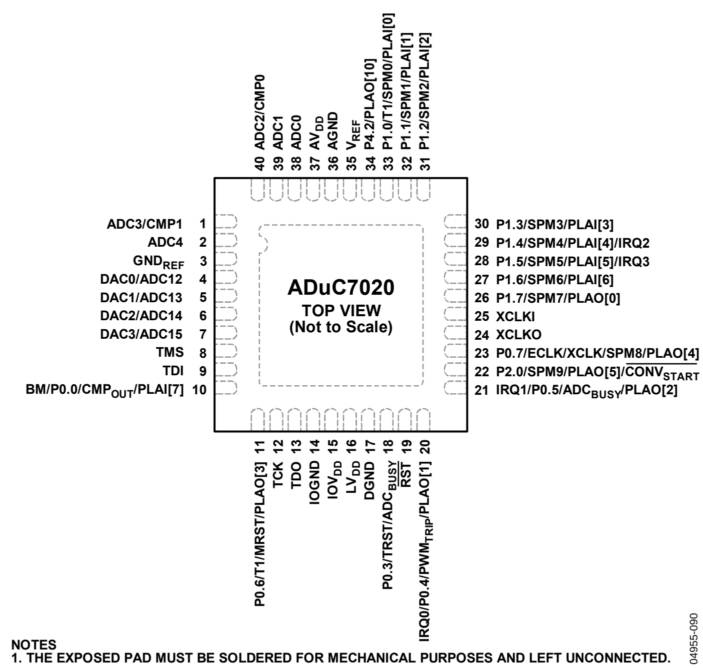

Figure 20. 40-Lead LFCSP_WQ Pin Configuration (ADuC7020)

Pin No.			Mnemonic	Description
7019/7020	7021	7022		
22	22	21	P2.0/SPM9/PLAO[5]/$\overline{\text{CONV}_{\text{START}}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/ Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
23	23	22	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/ Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/ Programmable Logic Array Output Element 4.
24	24	23	XCLKO	Output from the Crystal Oscillator Inverter.
25	25	24	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
26	26	25	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
27	27	26	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
28	28	27	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
29	29	28	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
30	30	29	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
31	31	30	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
32	32	31	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
33	33	32	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/ Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0.
34	–	–	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
35	34	33	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
36	35	34	AGND	Analog Ground. Ground reference point for the analog circuitry.
37	36	35	AV_{DD}	3.3 V Analog Power.
0	0	0	EP	Exposed Pad. The pin configuration for the ADuC7019/ADuC7020/ ADuC7021/ADuC7022 has an exposed pad that must be soldered for mechanical purposes and left unconnected.

ADuC7024/ADuC7025

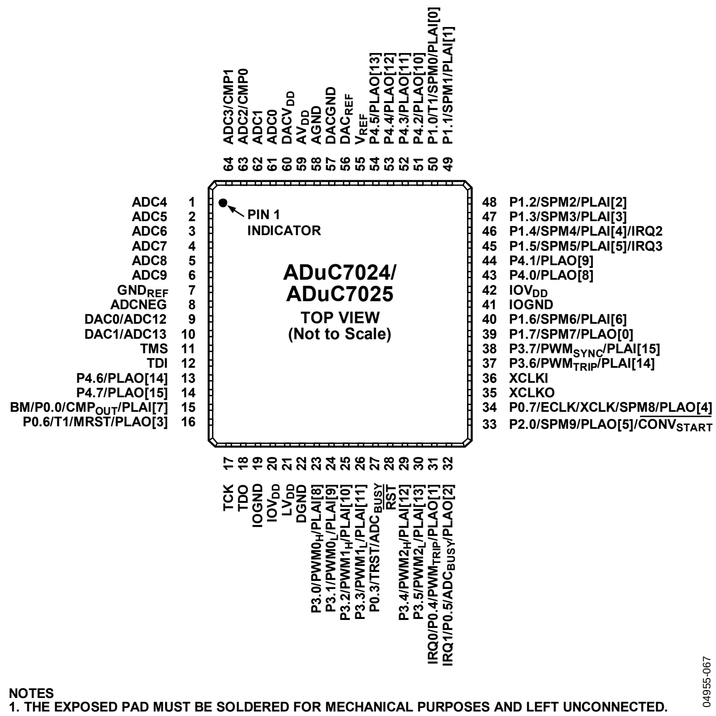

Figure 23. 64-Lead LFCSP_VQ Pin Configuration (ADuC7024/ADuC7025)

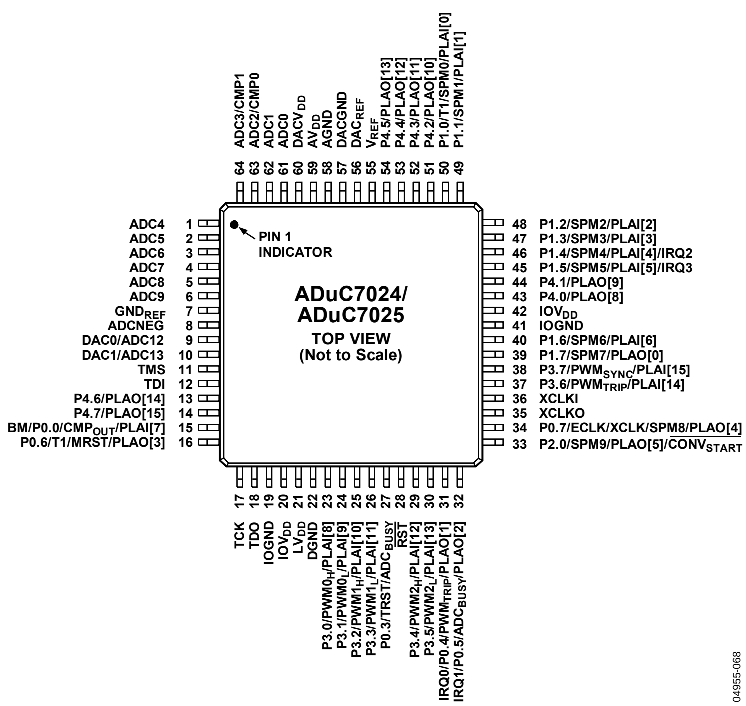

Figure 24. 64-Lead LQFP Pin Configuration (ADuC7024/ADuC7025)

Pin No.	Mnemonic	Description
D7	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
D8	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E1	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
E2	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
E4	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
E5	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
E7	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization/Programmable Logic Array Input Element 15.
E8	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
F1	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
F2	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F3	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
F4	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
F6	$\overline{RST}$	Reset Input, Active Low.
F7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F8	XCLKO	Output from the Crystal Oscillator Inverter.
G1	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7028 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
G2	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
G3	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
G4	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G5	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
G6	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
G7	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
G8	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
H1	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
H2	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
H3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
H4	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
H5	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
H6	DGND	Ground for Core Logic.
H7	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
H8	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity (INL)
The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, +½ LSB.

Gain Error
The deviation of the last code transition from the ideal AIN voltage (full scale – 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio (SINAD)
The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal to (Noise + Distortion)} = (6.02\,N + 1.76)\text{ dB}$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy
Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time
The amount of time it takes the output to settle to within a 1 LSB level for a full-scale input change.

MEMORY ORGANIZATION

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate two separate blocks of memory: 8 kB of SRAM and 64 kB of on-chip Flash/EE memory. The 62 kB of on-chip Flash/EE memory is available to the user, and the remaining 2 kB are reserved for the factory-configured boot page. These two blocks are mapped as shown in Figure 45.

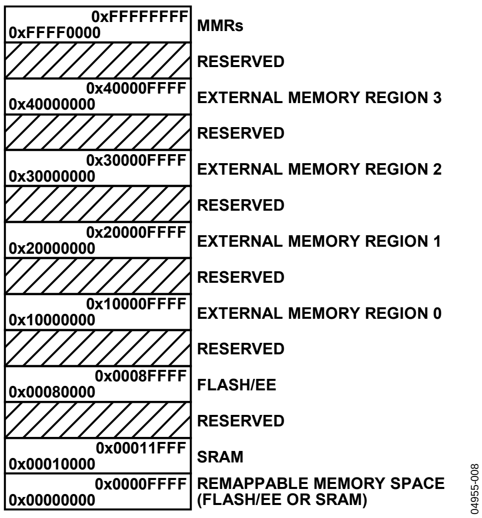

Figure 45. Physical Memory Map

Note that by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE Memory section.

MEMORY ACCESS

The ARM7 core sees memory as a linear array of a 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 45.

The ADuC7019/20/21/22/24/25/26/27/28/29 memory organizations are configured in little endian format, which means that the least significant byte is located in the lowest byte address, and the most significant byte is in the highest byte address.

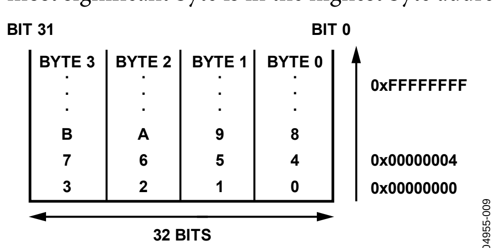

Figure 46. Little Endian Format

FLASH/EE MEMORY

The total 64 kB of Flash/EE memory is organized as 32 k × 16 bits; 31 k × 16 bits is user space and 1 k × 16 bits is reserved for the on-chip kernel. The page size of this Flash/EE memory is 512 bytes.

Sixty-two kilobytes of Flash/EE memory are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, which means that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. It is therefore recommended to use thumb mode when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in thumb mode and 20.89 MHz in full ARM mode. More details about Flash/EE access time are outlined in the Execution Time from SRAM and Flash/EE section.

SRAM

Eight kilobytes of SRAM are available to the user, organized as 2 k × 32 bits, that is, two words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array. More details about SRAM access time are outlined in the Execution Time from SRAM and Flash/EE section.

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 47 are unoccupied or reserved locations and should not be accessed by user software. Table 16 shows the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules and the advanced peripheral bus (APB) used for lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7019/20/21/22/24/25/26/27/28/29 are on the APB except the Flash/EE memory, the GPIOs (see Table 78), and the PWM.

Table 18. ADCCON MMR Bit Designations

Bit	Value	Description
15:13		Reserved.
12:10		ADC clock speed.
	000	fADC/1. This divider is provided to obtain 1 MSPS ADC with an external clock <41.78 MHz.
	001	fADC/2 (default value).
	010	fADC/4.
	011	fADC/8.
	100	fADC/16.
	101	fADC/32.
9:8		ADC acquisition time.
	00	Two clocks.
	01	Four clocks.
	10	Eight clocks (default value).
	11	16 clocks.
7		Enable start conversion. Set by the user to start any type of conversion command. Cleared by the user to disable a start conversion (clearing this bit does not stop the ADC when continuously converting).
6		Reserved.
5		ADC power control. Set by the user to place the ADC in normal mode (the ADC must be powered up for at least 5 μs before it converts correctly). Cleared by the user to place the ADC in power-down mode.
4:3		Conversion mode.
	00	Single-ended mode.
	01	Differential mode.
	10	Pseudo differential mode.
	11	Reserved.
2:0		Conversion type.
	000	Enable $\overline{CONV_{START}}$ pin as a conversion input.
	001	Enable Timer1 as a conversion input.
	010	Enable Timer0 as a conversion input.
	011	Single software conversion. Sets to 000 after conversion (note that Bit 7 of ADCCON MMR should be cleared after starting a single software conversion to avoid further conversions triggered by the $\overline{CONV_{START}}$ pin).
	100	Continuous software conversion.
	101	PLA conversion.
	Other	Reserved.

Table 19. ADCCP Register

Name	Address	Default Value	Access
ADCCP	0xFFFF0504	0x00	R/W

ADCCP is an ADC positive channel selection register. This MMR is described in Table 20.

Table 20. ADCCP[1] MMR Bit Designation

Bit	Value	Description
7:5		Reserved.
4:0		Positive channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Temperature sensor.
	10001	AGND (self-diagnostic feature).
	10010	Internal reference (self-diagnostic feature).
	10011	$AV_{DD}/2$.
	Others	Reserved.

[1] ADC and DAC channel availability depends on the part model. See Ordering Guide for details.

Table 21. ADCCN Register

Name	Address	Default Value	Access
ADCCN	0xFFFF0508	0x01	R/W

ADCCN is an ADC negative channel selection register. This MMR is described in Table 22.

Linearity degradation near ground and AV_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 64. The dotted line in Figure 64 indicates the ideal transfer function, and the solid line represents what the transfer function may look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 64 represents a transfer function in 0-to-AV_{DD} mode only. In 0-to-V_{REF} or 0-to-DAC_{REF} mode (with $V_{REF} < AV_{DD}$ or $DAC_{REF} < AV_{DD}$), the lower nonlinearity is similar. However, the upper portion of the transfer function follows the ideal line right to the end (V_{REF} in this case, not AV_{DD}), showing no signs of endpoint linearity errors.

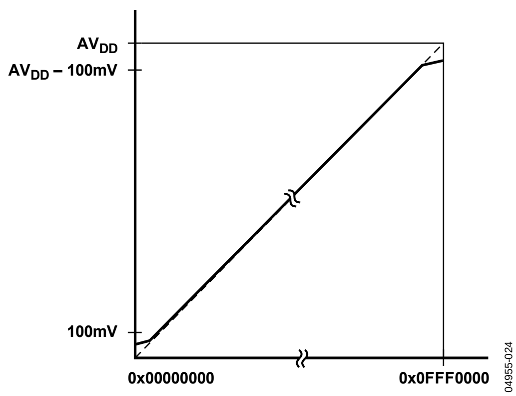

Figure 64. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities conceptually illustrated in Figure 64 get worse as a function of output loading. Most of the ADuC7019/20/21/22/24/25/26/27/28/29 data sheet specifications assume a 5 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 64 become larger. With larger current demands, this can significantly limit output voltage swing.

POWER SUPPLY MONITOR

The power supply monitor regulates the IOV_{DD} supply on the ADuC7019/20/21/22/24/25/26/27/28/29. It indicates when the IOV_{DD} supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is immediately cleared after CMP goes high.

This monitor function allows the user to save working registers to avoid possible data loss due to low supply or brown-out conditions. It also ensures that normal code execution does not resume until a safe supply level is established.

Table 53. PSMCON Register

Name	Address	Default Value	Access
PSMCON	0xFFFF0440	0x0008	R/W

Table 54. PSMCON MMR Bit Descriptions

Bit	Name	Description
3	CMP	Comparator bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates that the IOV_{DD} supply is above its selected trip point or that the PSM is in power-down mode. Read 0 indicates that the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip point selection bit. 0 = 2.79 V, 1 = 3.07 V.
1	PSMEN	Power supply monitor enable bit. Set to 1 to enable the power supply monitor circuit. Cleared to 0 to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the MicroConverter after CMP goes low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. After CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A 0 write has no effect. There is no timeout delay; PSMI can be immediately cleared after CMP goes high.

COMPARATOR

The ADuC7019/20/21/22/24/25/26/27/28/29 integrate voltage comparators. The positive input is multiplexed with ADC2, and the negative input has two options: ADC3 and DAC0. The output of the comparator can be configured to generate a system interrupt, be routed directly to the programmable logic array, start an ADC conversion, or be on an external pin, CMP_{OUT}, as shown in Figure 65.

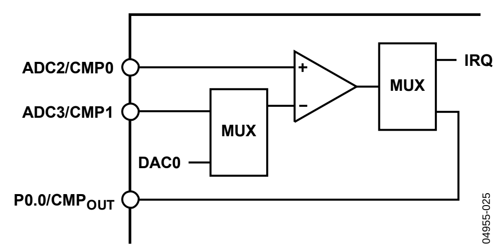

Figure 65. Comparator

Note that because the ADuC7022, ADuC7025, and ADu7027 parts do not support a DAC0 output, it is not possible to use DAC0 as a comparator input on these parts.

Hysteresis

Figure 66 shows how the input offset voltage and hysteresis terms are defined.

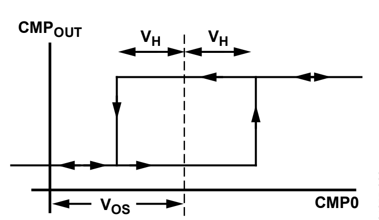

Figure 66. Comparator Hysteresis Transfer Function

DESCRIPTION OF THE PWM BLOCK

A functional block diagram of the PWM controller is shown in Figure 68. The generation of the six output PWM signals on Pin $PWM0_H$ to Pin $PWM2_L$ is controlled by the following four important blocks:

- The 3-phase PWM timing unit. The core of the PWM controller, this block generates three pairs of complemented and dead-time-adjusted, center-based PWM signals. This unit also generates the internal synchronization pulse, PWMSYNC. It also controls whether the external PWM_{SYNC} pin is used.
- The output control unit. This block can redirect the outputs of the 3-phase timing unit for each channel to either the high-side or low-side output. In addition, the output control unit allows individual enabling/disabling of each of the six PWM output signals.
- The gate drive unit. This block can generate the high frequency chopping and its subsequent mixing with the PWM signals.
- The PWM shutdown controller. This block controls the PWM shutdown via the PWM_{TRIP} pin and generates the correct reset signal for the timing unit.

The PWM controller is driven by the ADuC7019/20/21/22/24/25/26/27/28/29 core clock frequency and is capable of generating two interrupts to the ARM core. One interrupt is generated on the occurrence of a PWMSYNC pulse, and the other is generated on the occurrence of any PWM shutdown action.

3-Phase Timing Unit

PWM Switching Frequency (PWMDAT0 MMR)

The PWM switching frequency is controlled by the PWM period register, PWMDAT0. The fundamental timing unit of the PWM controller is

$$t_{CORE} = 1/f_{CORE}$$

where f_{CORE} is the core frequency of the MicroConverter.

Therefore, for a 41.78 MHz f_{CORE}, the fundamental time increment is 24 ns. The value written to the PWMDAT0 register is effectively the number of f_{CORE} clock increments in one-half a PWM period. The required PWMDAT0 value is a function of the desired PWM switching frequency (f_{PWN}) and is given by

$$PWMDAT0 = f_{CORE}/(2 \times f_{PWM})$$

Therefore, the PWM switching period, t_S, can be written as

$$t_S = 2 \times PWMDAT0 \times t_{CORE}$$

The largest value that can be written to the 16-bit PWMDAT0 MMR is 0xFFFF = 65,535, which corresponds to a minimum PWM switching frequency of

$$f_{PWM(min)} = 41.78 \times 10^6/(2 \times 65{,}535) = 318.75 \text{ Hz}$$

Note that PWMDAT0 values of 0 and 1 are not defined and should not be used.

PWM Switching Dead Time (PWMDAT1 MMR)

The second important parameter that must be set up in the initial configuration of the PWM block is the switching dead time. This is a short delay time introduced between turning off one PWM signal (0H, for example) and turning on the complementary signal (0L). This short time delay is introduced to permit the power switch to be turned off (in this case, 0H) to completely recover its blocking capability before the complementary switch is turned on. This time delay prevents a potentially destructive short-circuit condition from developing across the dc link capacitor of a typical voltage source inverter.

The dead time is controlled by the 10-bit, read/write PWMDAT1 register. There is only one dead-time register that controls the dead time inserted into all three pairs of PWM output signals. The dead time, t_D, is related to the value in the PWMDAT1 register by

$$t_D = PWMDAT1 \times 2 \times t_{CORE}$$

Therefore, a PWMDAT1 value of 0x00A (= 10), introduces a 426 ns delay between the turn-off on any PWM signal (0H, for example) and the turn-on of its complementary signal (0L). The amount of the dead time can, therefore, be programmed in increments of $2t_{CORE}$ (or 49 ns for a 41.78 MHz core clock).

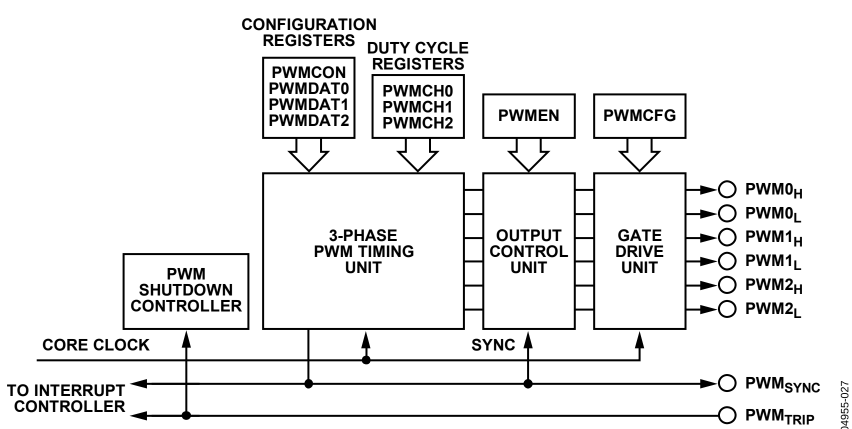

Figure 68. Overview of the PWM Controller

Both switching edges are moved by an equal amount ($PWMDAT1 \times t_{CORE}$) to preserve the symmetrical output patterns.

Also shown are the PWMSYNC pulse and Bit 0 of the PWMSTA register, which indicates whether operation is in the first or second half cycle of the PWM period.

The resulting on times of the PWM signals over the full PWM period (two half periods) produced by the timing unit can be written as follows:

On the high side

$$t_{0HH} = PWMDAT0 + 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

$$t_{0HL} = PWMDAT0 - 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (d)

$$d_{0H} = t_{0HH}/t_S = ½ + (PWMCH0 - PWMDAT1)/PWMDAT0$$

and on the low side

$$t_{0LH} = PWMDAT0 - 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

$$t_{0LL} = PWMDAT0 + 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (d)

$$d_{0L} = t_{0LH}/t_S = ½ - (PWMCH0 + PWMDAT1)/PWMDAT0$$

The minimum permissible t_{0H} and t_{0L} values are zero, corresponding to a 0% duty cycle. In a similar fashion, the maximum value is t_S, corresponding to a 100% duty cycle.

Figure 70 shows the output signals from the timing unit for operation in double update mode. It illustrates a general case where the switching frequency, dead time, and duty cycle are all changed in the second half of the PWM period. The same value for any or all of these quantities can be used in both halves of the PWM cycle. However, there is no guarantee that symmetrical PWM signals are produced by the timing unit in double update mode. Figure 70 also shows that the dead time insertions into the PWM signals are done in the same way as in single update mode.

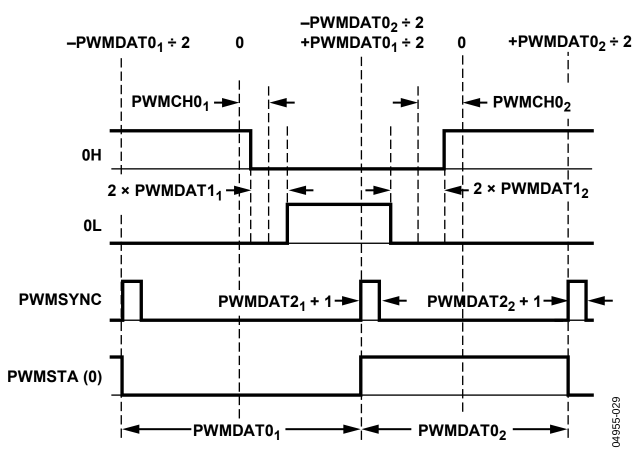

Figure 70. Typical PWM Outputs of the 3-Phase Timing Unit (Double Update Mode)

In general, the on times of the PWM signals in double update mode can be defined as follows:

On the high side

$$t_{0HH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

$$t_{0HL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (d) are

$$d_{0H} = t_{0HH}/t_S = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

On the low side

$$t_{0LH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

$$t_{0LL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (d) are

$$d_{0L} = t_{0LH}/t_S = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

For the completely general case in double update mode (see Figure 70), the switching period is given by

$$t_S = (PWMDAT0_1 + PWMDAT0_2) \times t_{CORE}$$

Again, the values of t_{0H} and t_{0L} are constrained to lie between zero and t_S.

PWM signals similar to those illustrated in Figure 69 and Figure 70 can be produced on the 1H, 1L, 2H, and 2L outputs by programming the PWMCH1 and PWMCH2 registers in a manner identical to that described for PWMCH0. The PWM controller does not produce any PWM outputs until all of the PWMDAT0, PWMCH0, PWMCH1, and PWMCH2 registers have been written to at least once. When these registers are written, internal counting of the timers in the 3-phase timing unit is enabled.

Writing to the PWMDAT0 register starts the internal timing of the main PWM timer. Provided that the PWMDAT0 register is written to prior to the PWMCH0, PWMCH1, and PWMCH2 registers in the initialization, the first PWMSYNC pulse and interrupt (if enabled) appear $1.5 \times t_{CORE} \times PWMDAT0$ seconds after the initial write to the PWMDAT0 register in single update mode. In double update mode, the first PWMSYNC pulse appears after $PWMDAT0 \times t_{CORE}$ seconds.

Table 78. GPIO Pin Function Descriptions

		Configuration			
Port	Pin	00	01	10	11
0	P0.0	GPIO	CMP	MS0	PLAI[7]
	P0.1	GPIO	$PWM2_H$	$\overline{BLE}$	
	P0.2	GPIO	$PWM2_L$	$\overline{BHE}$	
	P0.3	GPIO	TRST	A16	ADC_{BUSY}
	P0.4	GPIO/IRQ0	PWM_{TRIP}	MS1	PLAO[1]
	P0.5	GPIO/IRQ1	ADC_{BUSY}	MS2	PLAO[2]
	P0.6	GPIO/T1	MRST		PLAO[3]
	P0.7	GPIO	ECLK/XCLK[1]	SIN	PLAO[4]
1	P1.0	GPIO/T1	SIN	SCL0	PLAI[0]
	P1.1	GPIO	SOUT	SDA0	PLAI[1]
	P1.2	GPIO	RTS	SCL1	PLAI[2]
	P1.3	GPIO	CTS	SDA1	PLAI[3]
	P1.4	GPIO/IRQ2	RI	SCLK	PLAI[4]
	P1.5	GPIO/IRQ3	DCD	MISO	PLAI[5]
	P1.6	GPIO	DSR	MOSI	PLAI[6]
	P1.7	GPIO	DTR	$\overline{CS}$	PLAO[0]
2	P2.0	GPIO	$\overline{CONV_{START}}$[2]	SOUT	PLAO[5]
	P2.1	GPIO	$PWM0_H$	$\overline{WS}$	PLAO[6]
	P2.2	GPIO	$PWM0_L$	$\overline{RS}$	PLAO[7]
	P2.3	GPIO		AE	
	P2.4	GPIO	$PWM0_H$	MS0	
	P2.5	GPIO	$PWM0_L$	MS1	
	P2.6	GPIO	$PWM1_H$	MS2	
	P2.7	GPIO	$PWM1_L$	MS3	
3	P3.0	GPIO	$PWM0_H$	AD0	PLAI[8]
	P3.1	GPIO	$PWM0_L$	AD1	PLAI[9]
	P3.2	GPIO	$PWM1_H$	AD2	PLAI[10]
	P3.3	GPIO	$PWM1_L$	AD3	PLAI[11]
	P3.4	GPIO	$PWM2_H$	AD4	PLAI[12]
	P3.5	GPIO	$PWM2_L$	AD5	PLAI[13]
	P3.6	GPIO	PWM_{TRIP}	AD6	PLAI[14]
	P3.7	GPIO	PWM_{SYNC}	AD7	PLAI[15]
4	P4.0	GPIO		AD8	PLAO[8]
	P4.1	GPIO		AD9	PLAO[9]
	P4.2	GPIO		AD10	PLAO[10]
	P4.3	GPIO		AD11	PLAO[11]
	P4.4	GPIO		AD12	PLAO[12]
	P4.5	GPIO		AD13	PLAO[13]
	P4.6	GPIO		AD14	PLAO[14]
	P4.7	GPIO		AD15	PLAO[15]

[1] When configured in Mode 1, P0.7 is ECLK by default, or core clock output. To configure it as a clock input, the MDCLK bits in PLLCON must be set to 11.
[2] The $\overline{CONV_{START}}$ signal is active in all modes of P2.0.

Table 79. GPxCON Registers

Name	Address	Default Value	Access
GP0CON	0xFFFFF400	0x00000000	R/W
GP1CON	0xFFFFF404	0x00000000	R/W
GP2CON	0xFFFFF408	0x00000000	R/W
GP3CON	0xFFFFF40C	0x00000000	R/W
GP4CON	0xFFFFF410	0x00000000	R/W

GPxCON are the Port x control registers, which select the function of each pin of Port x as described in Table 80.

Table 80. GPxCON MMR Bit Descriptions

Bit	Description
31:30	Reserved.
29:28	Select function of the Px.7 pin.
27:26	Reserved.
25:24	Select function of the Px.6 pin.
23:22	Reserved.
21:20	Select function of the Px.5 pin.
19:18	Reserved.
17:16	Select function of the Px.4 pin.
15:14	Reserved.
13:12	Select function of the Px.3 pin.
11:10	Reserved.
9:8	Select function of the Px.2 pin.
7:6	Reserved.
5:4	Select function of the Px.1 pin.
3:2	Reserved.
1:0	Select function of the Px.0 pin.

Table 81. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFFF42C	0x20000000	R/W
GP1PAR	0xFFFFF43C	0x00000000	R/W

GPxPAR program the parameters for Port 0 and Port 1. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 82. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
30:29	Drive strength Px.7.
28	Pull-Up Disable Px.7.
27	Reserved.
26:25	Drive strength Px.6.
24	Pull-Up Disable Px.6.
23	Reserved.
22:21	Drive strength Px.5.
20	Pull-Up Disable Px.5.
19	Reserved.
18:17	Drive strength Px.4.
16	Pull-Up Disable Px.4.
15	Reserved.
14:13	Drive strength Px.3.
12	Pull-Up Disable Px.3.
11	Reserved.
10:9	Drive strength Px.2.
8	Pull-Up Disable Px.2.
7	Reserved.
6:5	Drive strength Px.1.
4	Pull-Up Disable Px.1.
3	Reserved.
2:1	Drive strength Px.0.
0	Pull-Up Disable Px.0.

Table 85. GPxDAT Registers

Name	Address	Default Value[1]	Access
GP0DAT	0xFFFFF420	0x000000XX	R/W
GP1DAT	0xFFFFF430	0x000000XX	R/W
GP2DAT	0xFFFFF440	0x000000XX	R/W
GP3DAT	0xFFFFF450	0x000000XX	R/W
GP4DAT	0xFFFFF460	0x000000XX	R/W

[1] X = 0, 1, 2, or 3.

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins configured as output, and store the input value of the pins configured as input.

Table 86. GPxDAT MMR Bit Descriptions

Bit	Description
31:24	Direction of the data. Set to 1 by user to configure the GPIO pin as an output. Cleared to 0 by user to configure the GPIO pin as an input.
23:16	Port x data output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x data input (read only).

Table 87. GPxSET Registers

Name	Address	Default Value[1]	Access
GP0SET	0xFFFFF424	0x000000XX	W
GP1SET	0xFFFFF434	0x000000XX	W
GP2SET	0xFFFFF444	0x000000XX	W
GP3SET	0xFFFFF454	0x000000XX	W
GP4SET	0xFFFFF464	0x000000XX	W

[1] X = 0, 1, 2, or 3.

GPxSET are data set Port x registers.

Table 88. GPxSET MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x set bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

Table 89. GPxCLR Registers

Name	Address	Default Value[1]	Access
GP0CLR	0xFFFFF428	0x000000XX	W
GP1CLR	0xFFFFF438	0x000000XX	W
GP2CLR	0xFFFFF448	0x000000XX	W
GP3CLR	0xFFFFF458	0x000000XX	W
GP4CLR	0xFFFFF468	0x000000XX	W

[1] X = 0, 1, 2, or 3.

GPxCLR are data clear Port x registers.

Table 90. GPxCLR MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x clear bit. Set to 1 by user to clear bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

SERIAL PORT MUX

The serial port mux multiplexes the serial port peripherals (an SPI, UART, and two I^2Cs) and the programmable logic array (PLA) to a set of 10 GPIO pins. Each pin must be configured to one of its specific I/O functions as described in Table 91.

Table 91. SPM Configuration

SPMMUX	GPIO (00)	UART (01)	UART/I²C/SPI (10)	PLA (11)
SPM0	P1.0	SIN	I2C0SCL	PLAI[0]
SPM1	P1.1	SOUT	I2C0SDA	PLAI[1]
SPM2	P1.2	RTS	I2C1SCL	PLAI[2]
SPM3	P1.3	CTS	I2C1SDA	PLAI[3]
SPM4	P1.4	RI	SCLK	PLAI[4]
SPM5	P1.5	DCD	MISO	PLAI[5]
SPM6	P1.6	DSR	MOSI	PLAI[6]
SPM7	P1.7	DTR	$\overline{CS}$	PLAO[0]
SPM8	P0.7	ECLK/XCLK	SIN	PLAO[4]
SPM9	P2.0	CONV	SOUT	PLAO[5]

Table 91 also details the mode for each of the SPMMUX pins. This configuration must be done via the GP0CON, GP1CON, and GP2CON MMRs. By default, these 10 pins are configured as GPIOs.

UART SERIAL INTERFACE

The UART peripheral is a full-duplex, universal, asynchronous receiver/transmitter. It is fully compatible with the 16,450 serial port standard. The UART performs serial-to-parallel conversions on data characters received from a peripheral device or modem, and parallel-to-serial conversions on data characters received from the CPU. The UART includes a fractional divider for baud rate generation and has a network addressable mode. The UART function is made available on the 10 pins of the ADuC7019/20/21/22/24/25/26/27/28/29 (see Table 92).

Table 92. UART Signal Description

Pin	Signal	Description
SPM0 (Mode 1)	SIN	Serial receive data.
SPM1 (Mode 1)	SOUT	Serial transmit data.
SPM2 (Mode 1)	RTS	Request to send.
SPM3 (Mode 1)	CTS	Clear to send.
SPM4 (Mode 1)	RI	Ring indicator.
SPM5 (Mode 1)	DCD	Data carrier detect.
SPM6 (Mode 1)	DSR	Data set ready.
SPM7 (Mode 1)	DTR	Data terminal ready.
SPM8 (Mode 2)	SIN	Serial receive data.
SPM9 (Mode 2)	SOUT	Serial transmit data.

The serial communication adopts an asynchronous protocol, which supports various word lengths, stop bits, and parity generation options selectable in the configuration register.

Baud Rate Generation

There are two ways of generating the UART baud rate, normal 450 UART baud rate generation and the fractional divider.

Normal 450 UART Baud Rate Generation

The baud rate is a divided version of the core clock using the values in the COMDIV0 and COMDIV1 MMRs (16-bit value, DL).

$$\text{Baud Rate} = \frac{41.78\,\text{MHz}}{2^{CD} - 16 \times 2 \times DL}$$

Table 93 gives some common baud rate values.

Table 93. Baud Rate Using the Normal Baud Rate Generator

Baud Rate	CD	DL	Actual Baud Rate	% Error
9600	0	0x88	9600	0
19,200	0	0x44	19,200	0
115,200	0	0x0B	118,691	3
9600	3	0x11	9600	0
19,200	3	0x08	20,400	6.25
115,200	3	0x01	163,200	41.67

Fractional Divider

The fractional divider, combined with the normal baud rate generator, produces a wider range of more accurate baud rates.

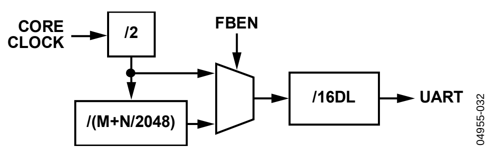

Figure 75. Baud Rate Generation Options

Calculation of the baud rate using fractional divider is as follows:

$$Baud\ \ Rate = \frac{41.78\,\text{MHz}}{2^{CD} \times 16 \times DL \times 2 \times \left(M + \frac{N}{2048}\right)}$$

$$M + \frac{N}{2048} = \frac{41.78\,\text{MHz}}{\text{Baud Rate} \times 2^{CD} \times 16 \times DL \times 2}$$

For example, generation of 19,200 baud with CD bits = 3 (Table 93 gives DL = 0x08) is

$$M + \frac{N}{2048} = \frac{41.78\,\text{MHz}}{19200 \times 2^{3} \times 16 \times 8 \times 2}$$

$$M + \frac{N}{2048} = 1.06$$

where:
$M = 1$
$N = 0.06 \times 2048 = 128$

$$\text{Baud Rate} = \frac{41.78\,\text{MHz}}{2^{3} \times 16 \times 8 \times 2 \times \frac{128}{2048}}$$

where:
Baud Rate = 19,200 bps

Error = 0%, compared to 6.25% with the normal baud rate generator.

UART Register Definitions

The UART interface consists of 12 registers: COMTX, COMRX, COMDIV0, COMIEN0, COMDIV1, COMIID0, COMCON0, COMCON1, COMSTA0, COMSTA1, COMSCR, and COMDIV2.

Table 94. COMTX Register

Name	Address	Default Value	Access
COMTX	0xFFFF0700	0x00	R/W

COMTX is an 8-bit transmit register.

Table 95. COMRX Register

Name	Address	Default Value	Access
COMRX	0xFFFF0700	0x00	R

COMRX is an 8-bit receive register.

Table 96. COMDIV0 Register

Name	Address	Default Value	Access
COMDIV0	0xFFFF0700	0x00	R/W

COMDIV0 is a low byte divisor latch. COMTX, COMRX, and COMDIV0 share the same address location. COMTX and COMRX can be accessed when Bit 7 in the COMCON0 register is cleared. COMDIV0 can be accessed when Bit 7 of COMCON0 is set.

Table 97. COMIEN0 Register

Name	Address	Default Value	Access
COMIEN0	0xFFFF0704	0x00	R/W

COMIEN0 is the interrupt enable register.

Table 98. COMIEN0 MMR Bit Descriptions

Bit	Name	Description
7:4	N/A	Reserved.
3	EDSSI	Modem status interrupt enable bit. Set by user to enable generation of an interrupt if any of COMSTA1[3:1] is set. Cleared by user.
2	ELSI	Rx status interrupt enable bit. Set by user to enable generation of an interrupt if any of COMSTA0[4:1] is set. Cleared by user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by user to enable interrupt when buffer is empty during a transmission. Cleared by user.
0	ERBFI	Enable receive buffer full interrupt. Set by user to enable interrupt when buffer is full during a reception. Cleared by user.

Table 116. COMIID1 MMR Bit Descriptions

Bit 3:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
000	1		No interrupt	
110	0	2	Matching network address	Read COMRX
101	0	3	Address transmitted, buffer empty	Write data to COMTX or read COMIID0
011	0	1	Receive line status interrupt	Read COMSTA0
010	0	2	Receive buffer full interrupt	Read COMRX
001	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
000	0	4	Modem status interrupt	Read COMSTA1

Note that to receive a network address interrupt, the slave must ensure that Bit 0 of COMIEN0 (enable receive buffer full interrupt) is set to 1.

Table 117. COMADR Register

Name	Address	Default Value	Access
COMADR	0xFFFF0728	0xAA	R/W

COMADR is an 8-bit, read/write network address register that holds the address checked for by the network addressable UART. Upon receiving this address, the device interrupts the processor and/or sets the appropriate status bit in COMIID1.

SERIAL PERIPHERAL INTERFACE

The ADuC7019/20/21/22/24/25/26/27/28/29 integrate a complete hardware serial peripheral interface (SPI) on-chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 3.48 Mb, as shown in Table 118. The SPI interface is not operational with core clock divider (CD) bits. POWCON[2:0] = 6 or 7 in master mode.

The SPI port can be configured for master or slave operation. and typically consists of four pins: MISO (P1.5), MOSI (P1.6), SCLK (P1.4), and $\overline{\text{CS}}$ (P1.7).

On the transmit side, the SPITX register (and a TX shift register outside it) loads data onto the transmit pin (in slave mode, MISO; in master mode, MOSI). The transmit status bit, Bit 0, in SPISTA indicates whether there is valid data in the SPITX register.

Similarly, the receive data path consists of the SPIRX register (and an RX shift register). SPISTA, Bit 3 indicates whether there is valid data in the SPIRX register. If valid data in the SPIRX register is overwritten or if valid data in the RX shift register is discarded, SPISTA, Bit 5 (the overflow bit) is set.

MISO (Master In, Slave Out) Pin

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In) Pin

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O) Pin

The master serial clock (SCLK) is used to synchronize the data being transmitted and received through the MOSI SCLK period. Therefore, a byte is transmitted/received after eight SCLK periods. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, the polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{2 \times (1 + SPIDIV)}$$

The maximum speed of the SPI clock is dependent on the clock divider bits and is summarized in Table 118.

Table 118. SPI Speed vs. Clock Divider Bits in Master Mode

CD Bits	0	1	2	3	4	5
SPIDIV in Hex	0x05	0x0B	0x17	0x2F	0x5F	0xBF
SPI dpeed in MHz	3.482	1.741	0.870	0.435	0.218	0.109

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10.4 Mb at CD = 0. The formula to determine the maximum speed is as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{HCLK}}{4}$$

In both master and slave modes, data is transmitted on one edge of the SCL signal and sampled on the other. Therefore, it is important that the polarity and phase be configured the same for the master and slave devices.

Chip Select ($\overline{\text{CS}}$ Input) Pin

In SPI slave mode, a transfer is initiated by the assertion of $\overline{\text{CS}}$, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{\text{CS}}$. In slave mode, $\overline{\text{CS}}$ is always an input.

SPI Registers

The following MMR registers are used to control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

Table 119. SPISTA Register

Name	Address	Default Value	Access
SPISTA	0xFFFF0A00	0x00	R

SPISTA is an 8-bit read-only status register. Only Bit 1 or Bit 4 of this register generates an interrupt. Bit 6 of the SPICON register determines which bit generates the interrupt.

Table 120. SPISTA MMR Bit Descriptions

Bit	Description
7:6	Reserved.
5	SPIRX data register overflow status bit. Set if SPIRX is overflowing. Cleared by reading the SPIRX register.
4	SPIRX data register IRQ. Set automatically if Bit 3 or Bit 5 is set. Cleared by reading the SPIRX register.
3	SPIRX data register full status bit. Set automatically if a valid data is present in the SPIRX register. Cleared by reading the SPIRX register.
2	SPITX data register underflow status bit. Set automatically if SPITX is underflowing. Cleared by writing in the SPITX register.
1	SPITX data register IRQ. Set automatically if Bit 0 is clear or Bit 2 is set. Cleared by writing in the SPITX register or if finished transmission disabling the SPI.
0	SPITX data register empty status bit. Set by writing to SPITX to send data. This bit is set during transmission of data. Cleared when SPITX is empty.

Table 121. SPIRX Register

Name	Address	Default Value	Access
SPIRX	0xFFFF0A04	0x00	R

SPIRX is an 8-bit, read-only receive register.

Table 122. SPITX Register

Name	Address	Default Value	Access
SPITX	0xFFFF0A08	0x00	W

SPITX is an 8-bit, write-only transmit register.

Table 123. SPIDIV Register

Name	Address	Default Value	Access
SPIDIV	0xFFFF0A0C	0x1B	R/W

SPIDIV is an 8-bit, serial clock divider register.

Table 124. SPICON Register

Name	Address	Default Value	Access
SPICON	0xFFFF0A10	0x0000	R/W

SPICON is a 16-bit control register.

Table 125. SPICON MMR Bit Descriptions

Bit	Description	Function
15:13	Reserved	N/A
12	Continuous transfer enable	Set by user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the TX register. $\overline{CS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until TX is empty. Cleared by user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period.
11	Loop back enable	Set by user to connect MISO to MOSI and test software. Cleared by user to be in normal mode.
10	Slave MISO output enable	Set this bit to disable the output driver on the MISO pin. The MISO pin becomes open drain when this bit is set. Clear this bit for MISO to operate as normal.
9	Clip select output enable	Set by user in master mode to disable the chip select output. cleared by user to enable the chip select output. P1.7 should be configured as $\overline{CS}$ before SPICON is configured as a master when the chip select output enabled is also selected.
8	SPIRX overflow overwrite enable	Set by user, the valid data in the RX register is overwritten by the new serial byte received. Cleared by user, the new serial byte received is discarded.
7	SPITX underflow mode	Set by user to transmit 0. Cleared by user to transmit the previous data.
6	Transfer and interrupt mode	Set by user to initiate transfer with a write to the SPITX register. Interrupt occurs only when TX is empty. Cleared by user to initiate transfer with a read of the SPIRX register. Interrupt occurs only when RX is full.
5	LSB first transfer enable bit	Set by user, the LSB is transmitted first. Cleared by user, the MSB is transmitted first.
4	Reserved	
3	Serial clock polarity mode bit	Set by user, the serial clock idles high. Cleared by user, the serial clock idles low.
2	Serial clock phase mode bit	Set by user, the serial clock pulses at the beginning of each serial bit transfer. Cleared by user, the serial clock pulses at the end of each serial bit transfer.
1	Master mode enable bit	Set by user to enable master mode. Cleared by user to enable slave mode.
0	SPI enable bit	Set by user to enable the SPI. Cleared by user to disable the SPI.

I²C-COMPATIBLE INTERFACES

The ADuC7019/20/21/22/24/25/26/27/28/29 support two licensed I²C interfaces. The I²C interfaces are both implemented as a hard-ware master and a full slave interface. Because the two I²C inter-faces are identical, this data sheet describes only I2C0 in detail. Note that the two masters and one of the slaves have individual interrupts (see the Interrupt System section).

Note that when configured as an I²C master device, the ADuC7019/20/21/22/24/25/26/27/28/29 cannot generate a repeated start condition.

The two GPIO pins used for data transfer, SDAx and SCLx, are configured in a wired-AND format that allows arbitration in a multimaster system. These pins require external pull-up resistors. Typical pull-up values are 10 kΩ.

The I²C bus peripheral address in the I²C bus system is pro-grammed by the user. This ID can be modified any time a transfer is not in progress. The user can configure the interface to respond to four slave addresses.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the slave device address and the direction of the data transfer during the initial address transfer. If the master does not lose arbitration and the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition and the bus becomes idle.

The I²C peripheral can be configured only as a master or slave at any given time. The same I²C channel cannot simultaneously support master and slave modes.

Serial Clock Generation

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (400 kHz) or standard mode (100 kHz).

The bit rate is defined in the I2C0DIV MMR as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{(2 + DIVH) + (2 + DIVL)}$$

where:
f_{UCLK} = clock before the clock divider.
$DIVH$ = the high period of the clock.
$DIVL$ = the low period of the clock.

Thus, for 100 kHz operation,

$DIVH = DIVL = 0xCF$

and for 400 kHz,

$DIVH = 0x28, DIVL = 0x3C$

The I2CxDIV registers correspond to DIVH:DIVL.

Slave Addresses

The registers I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3 contain the device IDs. The device compares the four I2C0IDx registers to the address byte. To be correctly addressed, the seven MSBs of either ID register must be identical to that of the seven MSBs of the first received address byte. The LSB of the ID registers (the transfer direction bit) is ignored in the process of address recognition.

I²C Registers

The I²C peripheral interface consists of 18 MMRs, which are discussed in this section.

Table 126. I2CxMSTA Registers

Name	Address	Default Value	Access
I2C0MSTA	0xFFFF0800	0x00	R/W
I2C1MSTA	0xFFFF0900	0x00	R/W

I2CxMSTA are status registers for the master channel.

Table 127. I2C0MSTA MMR Bit Descriptions

Bit	Access Type	Description
7	R/W	Master transmit FIFO flush. Set by user to flush the master Tx FIFO. Cleared automatically after the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
6	R	Master busy. Set automatically if the master is busy. Cleared automatically.
5	R	Arbitration loss. Set in multimaster mode if another master has the bus. Cleared when the bus becomes available.
4	R	No ACK. Set automatically if there is no acknowledge of the address by the slave device. Cleared automatically by reading the I2C0MSTA register.
3	R	Master receive IRQ. Set after receiving data. Cleared automatically by reading the I2C0MRX register.
2	R	Master transmit IRQ. Set at the end of a transmission. Cleared automatically by writing to the I2C0MTX register.
1	R	Master transmit FIFO underflow. Set automatically if the master transmit FIFO is underflowing. Cleared automatically by writing to the I2C0MTX register.
0	R	Master TX FIFO not full. Set automatically if the slave transmit FIFO is not full. Cleared automati-cally by writing twice to the I2C0STX register.

Table 128. I2CxSSTA Registers

Name	Address	Default Value	Access
I2C0SSTA	0xFFFF0804	0x01	R
I2C1SSTA	0xFFFF0904	0x01	R

I2CxSSTA are status registers for the slave channel.

Table 137. I2CxALT Registers

Name	Address	Default Value	Access
I2C0ALT	0xFFFF0828	0x00	R/W
I2C1ALT	0xFFFF0928	0x00	R/W

I2CxALT are hardware general call ID registers used in slave mode.

Table 138. I2CxCFG Registers

Name	Address	Default Value	Access
I2C0CFG	0xFFFF082C	0x00	R/W
I2C1CFG	0xFFFF092C	0x00	R/W

I2CxCFG are configuration registers.

Table 139. I2C0CFG MMR Bit Descriptions

Bit	Description
31:5	Reserved. These bits should be written by the user as 0.
14	Enable stop interrupt. Set by the user to generate an interrupt upon receiving a stop condition and after receiving a valid start condition and matching address. Cleared by the user to disable the generation of an interrupt upon receiving a stop condition.
13	Reserved.
12	Reserved.
11	Enable stretch SCL (holds SCL low). Set by the user to stretch the SCL line. Cleared by the user to disable stretching of the SCL line.
10	Reserved.
9	Slave Tx FIFO request interrupt enable. Set by the user to disable the slave Tx FIFO request interrupt. Cleared by the user to generate an interrupt request just after the negative edge of the clock for the R/W bit. This allows the user to input data into the slave Tx FIFO if it is empty. At 400 ksps and the core clock running at 41.78 MHz, the user has 45 clock cycles to take appropriate action, taking interrupt latency into account.
8	General call status bit clear. Set by the user to clear the general call status bits. Cleared automatically by hardware after the general call status bits are cleared.
7	Master serial clock enable bit. Set by user to enable generation of the serial clock in master mode. Cleared by user to disable serial clock in master mode.
6	Loopback enable bit. Set by user to internally connect the transition to the reception to test user software. Cleared by user to operate in normal mode.
5	Start backoff disable bit. Set by user in multimaster mode. If losing arbitration, the master immediately tries to retransmit. Cleared by user to enable start backoff. After losing arbitration, the master waits before trying to retransmit.
4	Hardware general call enable. When this bit and Bit 3 are set and have received a general call (Address 0x00) and a data byte, the device checks the contents of I2C0ALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a "to whom it may concern" call. The ADuC7019/20/21/22/24/25/26/27/28/29 watch for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2C0ALT register should always be written to 1, as indicated in *The I²C-Bus Specification*, January 2000, from NXP.
3	General call enable bit. This bit is set by the user to enable the slave device to acknowledge (ACK) an I²C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of slave address by hardware) as the data byte, the I²C interface resets as as indicated in *The I²C-Bus Specification,* January 2000, from NXP. This command can be used to reset an entire I²C system. The general call interrupt status bit sets on any general call. The user must take corrective action by setting up the I²C interface after a reset. If it receives a 0x04 (write programmable part of slave address by hardware) as the data byte, the general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address.
2	Reserved.
1	Master enable bit. Set by user to enable the master I²C channel. Cleared by user to disable the master I²C channel.
0	Slave enable bit. Set by user to enable the slave I²C channel. A slave transfer sequence is monitored for the device address in I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3. At 400 kSPs, the core clock should run at 41.78 MHz because the interrupt latency could be up to 45 clock cycles alone. After the I²C read bit, the user has 0.5 of an I²C clock cycle to load the Tx FIFO. AT 400 kSPS, this is 1.26 µs, the interrupt latency.