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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	22
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	49-TFBGA, CSPBGA
Supplier Device Package	49-CSPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7029bbcz62-rl

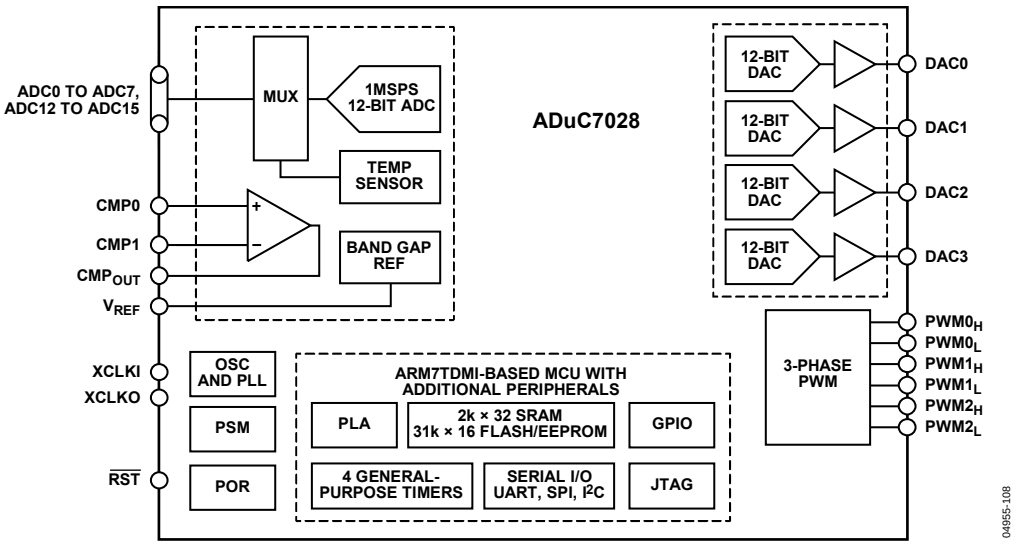

Figure 9.

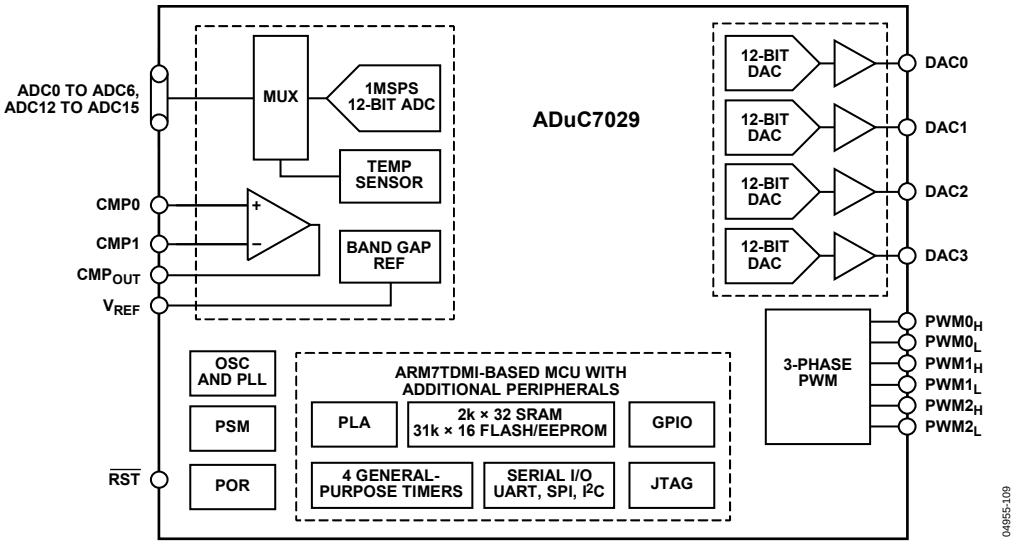

Figure 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MCU CLOCK RATE					
From 32 kHz Internal Oscillator		326		kHz	CD[12] = 7
From 32 kHz External Crystal		41.78		MHz	CD[12] = 0
Using an External Clock	0.05		44	MHz	T_A = 85°C
	0.05		41.78	MHz	T_A = 125°C
START-UP TIME					Core clock = 41.78 MHz
At Power-On		130		ms	
From Pause/Nap Mode		24		ns	CD[12] = 0
		3.06		µs	CD[12] = 7
From Sleep Mode		1.58		ms	
From Stop Mode		1.7		ms	
PROGRAMMABLE LOGIC ARRAY (PLA)					
Pin Propagation Delay		12		ns	From input pin to output pin
Element Propagation Delay		2.5		ns	
POWER REQUIREMENTS[13, 14]					
Power Supply Voltage Range					
AV_{DD} to AGND and IOV_{DD} to IOGND	2.7		3.6	V	
Analog Power Supply Currents					
AV_{DD} Current		200		µA	ADC in idle mode; all parts except ADuC7019
		400		µA	ADC in idle mode; ADuC7019 only
$DACV_{DD}$ Current[15]		3	25	µA	
Digital Power Supply Current					
IOV_{DD} Current in Normal Mode					Code executing from Flash/EE
		7	10	mA	CD[12] = 7
		11	15	mA	CD[12] = 3
		40	45	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode		25	30	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode		250	400	µA	T_A = 85°C
		600	1000	µA	T_A = 125°C
Additional Power Supply Currents					
ADC		2		mA	@ 1 MSPS
		0.7		mA	@ 62.5 kSPS
DAC		700		µA	per DAC
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			4	kV	
FCIDM Passed Up To			0.5	kV	

[1] All ADC channel specifications are guaranteed during normal MicroConverter core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 59. Based on external ADC system components; the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22m, Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] See the POWCON register.
[13] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[14] IOV_{DD} power supply current decreases typically by 2 mA during a Flash/EE erase cycle.
[15] On the ADuC7019/20/21/22, this current must be added to the AV_{DD} current.

Table 6. SPI Master Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

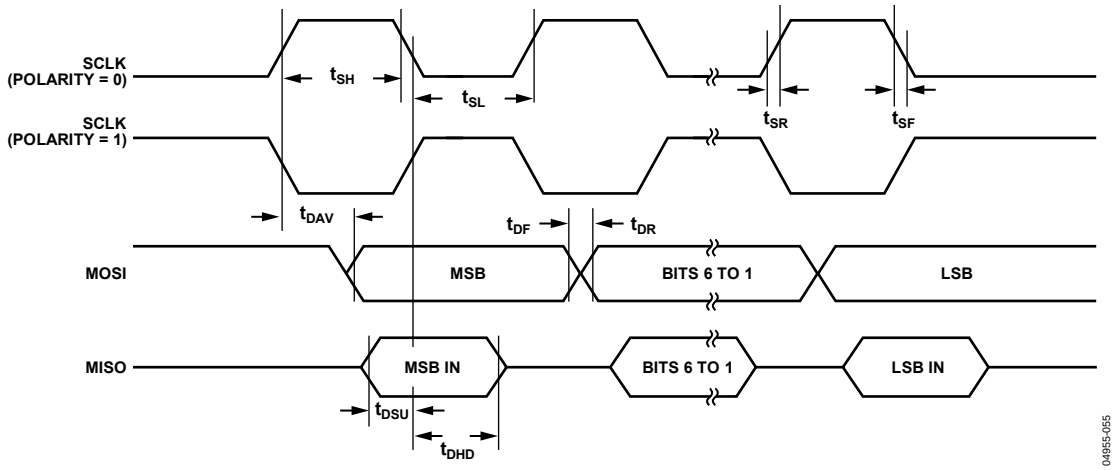

Figure 15. SPI Master Mode Timing (Phase Mode = 1)

Table 7. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

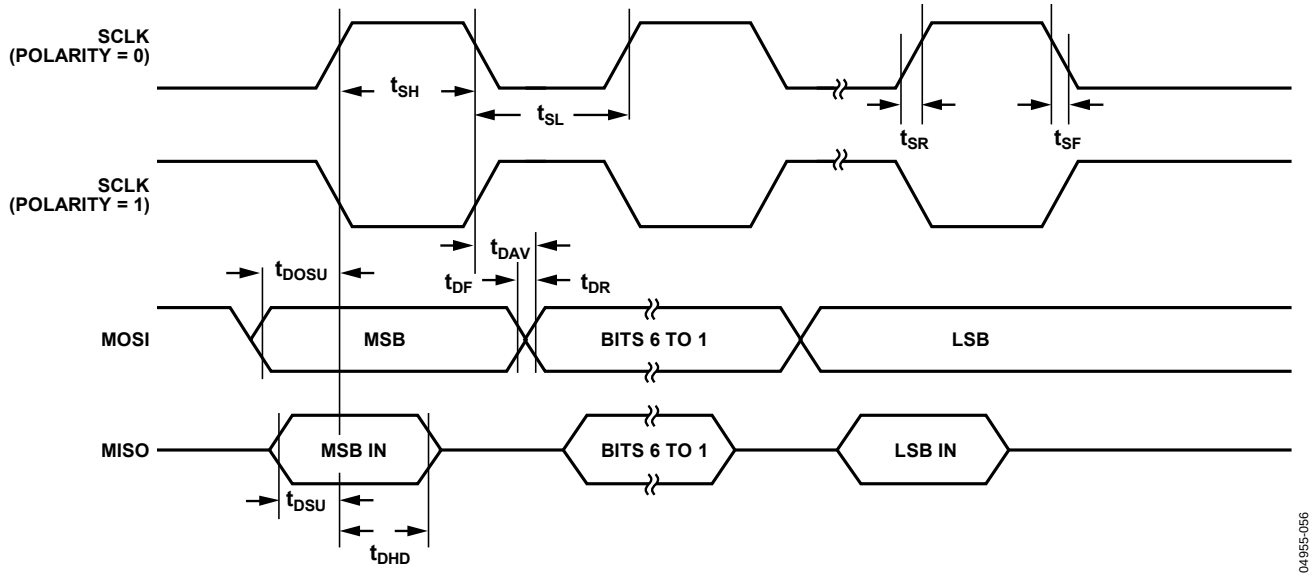

Figure 16. SPI Master Mode Timing (Phase Mode = 0)

Table 11. Pin Function Descriptions (ADuC7019/ADuC7020/ADuC7021/ADuC7022)

Pin No.				
7019/7020	7021	7022	Mnemonic	Description
38	37	36	ADC0	Single-Ended or Differential Analog Input 0.
39	38	37	ADC1	Single-Ended or Differential Analog Input 1.
40	39	38	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
1	40	39	ADC3/CMP1	Single-Ended or Differential Analog Input 3 (Buffered Input on ADuC7019)/ Comparator Negative Input.
2	1	40	ADC4	Single-Ended or Differential Analog Input 4.
–	2	1	ADC5	Single-Ended or Differential Analog Input 5.
–	3	2	ADC6	Single-Ended or Differential Analog Input 6.
–	4	3	ADC7	Single-Ended or Differential Analog Input 7.
–	–	4	ADC8	Single-Ended or Differential Analog Input 8.
–	–	5	ADC9	Single-Ended or Differential Analog Input 9.
3	5	6	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
4	6	–	DAC0/ADC12	DAC0 Voltage Output/Single-Ended or Differential Analog Input 12.
5	7	–	DAC1/ADC13	DAC1 Voltage Output/Single-Ended or Differential Analog Input 13.
6	–	–	DAC2/ADC14	DAC2 Voltage Output/Single-Ended or Differential Analog Input 14.
7	–	–	DAC3/ADC15	DAC3 Voltage Output on ADuC7020. On the ADuC7019, a 10 nF capacitor must be connected between this pin and AGND/Single-Ended or Differential Analog Input 15 (see Figure 53).
8	8	7	TMS	Test Mode Select, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases, an external pull-up resistor (~100K) is also required to ensure that the part does not enter an erroneous state.
9	9	8	TDI	Test Data In, JTAG Test Port Input. Debug and download access.
10	10	9	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot Mode (BM). The ADuC7019/20/21/22 enter serial download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
11	11	10	P0.6/T1/MRST/PLAO[3]	Multifunction Pin. Driven low after reset. General-Purpose Output Port 0.6/ Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
12	12	11	TCK	Test Clock, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases an external pull-up resistor (~100K) is also required to ensure that the part does not enter an erroneous state.
13	13	12	TDO	Test Data Out, JTAG Test Port Output. Debug and download access.
14	14	13	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
15	15	14	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
16	16	15	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
17	17	16	DGND	Ground for Core Logic.
18	18	17	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/Test Reset, JTAG Test Port Input/ ADC_{BUSY} Signal Output.
19	19	18	$\overline{RST}$	Reset Input, Active Low.
20	20	19	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
21	21	20	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

TYPICAL PERFORMANCE CHARACTERISTICS

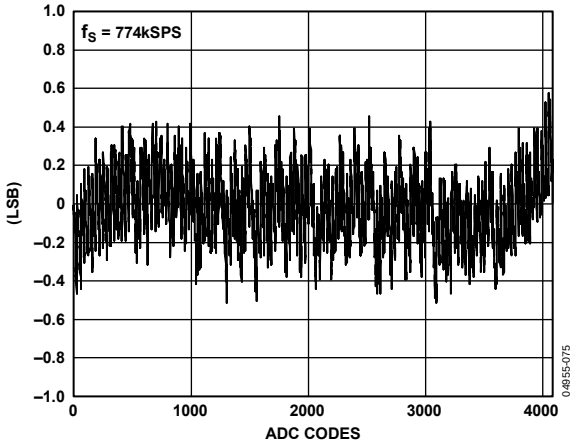

Figure 28. Typical INL Error, f_S = 774 kSPS

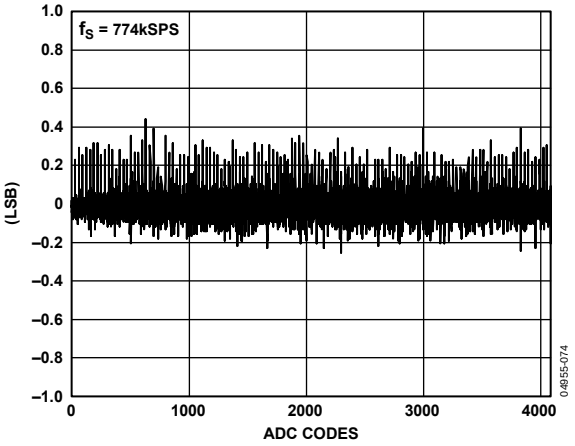

Figure 31. Typical DNL Error, f_S = 774 kSPS

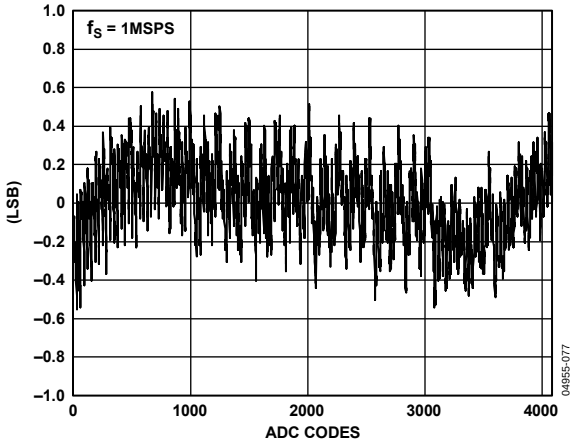

Figure 29. Typical INL Error, f_S = 1 MSPS

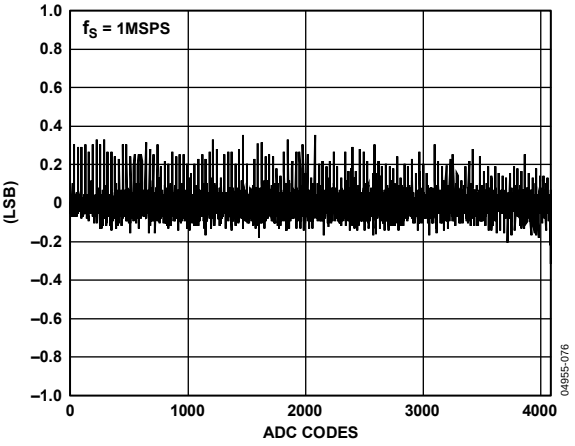

Figure 32. Typical DNL Error, f_S = 1 MSPS

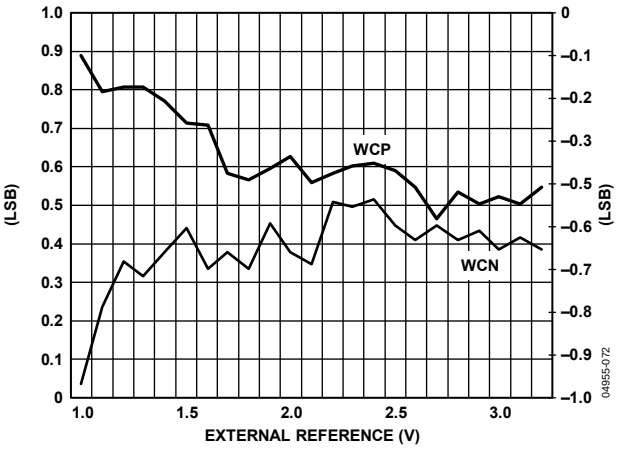

Figure 30. Typical Worst-Case (Positive (WCP) and Negative (WCN)) INL Error vs. V_{REF}, f_S = 774 kSPS

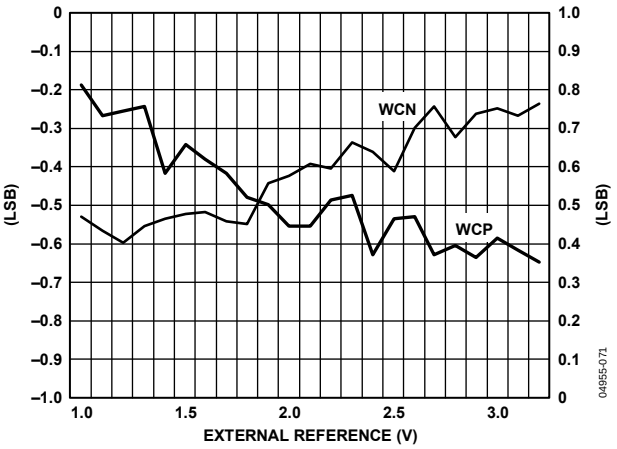

Figure 33. Typical Worst-Case (Positive (WCP)and Negative (WCN)) DNL Error vs. V_{REF}, f_S = 774 kSPS

OVERVIEW OF THE ARM7TDMI CORE

The ARM7® core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be eight bits, 16 bits, or 32 bits. The length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with four additional features.

- T support for the thumb (16-bit) instruction set.
- D support for debug.
- M support for long multiplications.
- I includes the EmbeddedICE module to support embedded system debugging.

THUMB MODE (T)

An ARM instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set that is compressed into 16 bits, called the thumb instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However, the thumb mode has two limitations.

- Thumb code typically requires more instructions for the same job. As a result, ARM code is usually best for maximizing the performance of time-critical code.
- The thumb instruction set does not include some of the instructions needed for exception handling, which automatically switches the core to ARM code for exception handling.

See the ARM7TDMI user guide for details on the core architecture, the programming model, and both the ARM and ARM thumb instruction sets.

LONG MULTIPLY (M)

The ARM7TDMI instruction set includes four extra instructions that perform 32-bit by 32-bit multiplication with a 64-bit result, and 32-bit by 32-bit multiplication-accumulation (MAC) with a 64-bit result. These results are achieved in fewer cycles than required on a standard ARM7 core.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the Flash/EE, SRAM, and memory mapped registers.

EXCEPTIONS

ARM supports five types of exceptions and a privileged processing mode for each type. The five types of exceptions are

- Normal interrupt or IRQ, which is provided to service general-purpose interrupt handling of internal and external events.
- Fast interrupt or FIQ, which is provided to service data transfers or communication channels with low latency. FIQ has priority over IRQ.
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt instruction (SWI), which can be used to make a call to an operating system.

Typically, the programmer defines interrupt as IRQ, but for higher priority interrupt, that is, faster response time, the programmer can define interrupt as FIQ.

ARM REGISTERS

ARM7TDMI has a total of 37 registers: 31 general-purpose registers and six status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general-purpose 32-bit registers (R0 to R14), the program counter (R15), and the current program status register (CPSR) are usable. The remaining registers are used for system-level programming and exception handling only.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14), as represented in Figure 44. The fast interrupt mode has more registers (R8 to R12) for fast interrupt processing. This means that interrupt processing can begin without the need to save or restore these registers and, thus, save critical time in the interrupt handling process.

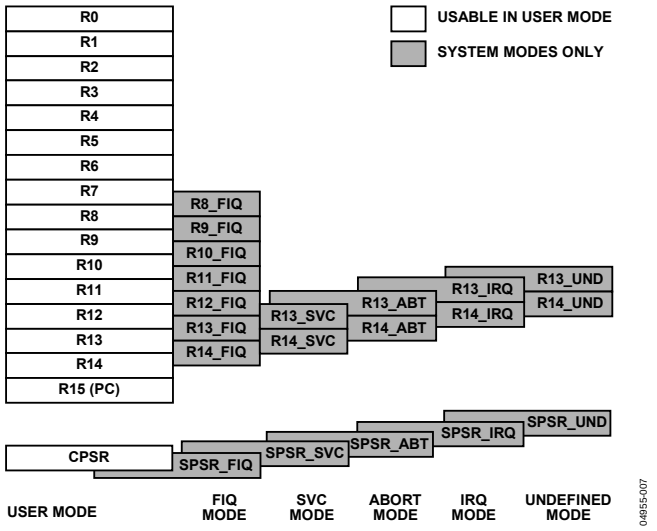

Figure 44. Register Organization

TYPICAL OPERATION

Once configured via the ADC control and channel selection registers, the ADC converts the analog input and provides a 12-bit result in the ADC data register.

The top four bits are the sign bits. The 12-bit result is placed from Bit 16 to Bit 27, as shown in Figure 51. Again, it should be noted that, in fully differential mode, the result is represented in twos complement format. In pseudo differential and single-ended modes, the result is represented in straight binary format.

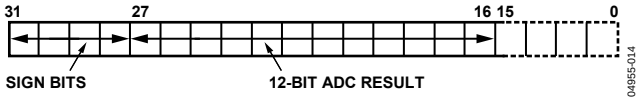

Figure 51. ADC Result Format

The same format is used in DACxDAT, simplifying the software.

Current Consumption

The ADC in standby mode, that is, powered up but not converting, typically consumes 640 μA. The internal reference adds 140 μA. During conversion, the extra current is 0.3 μA multiplied by the sampling frequency (in kilohertz (kHz)). Figure 43 shows the current consumption vs. the sampling frequency of the ADC.

Timing

Figure 52 gives details of the ADC timing. Users control the ADC clock speed and the number of acquisition clocks in the ADCCON MMR. By default, the acquisition time is eight clocks and the clock divider is 2. The number of extra clocks (such as bit trial or write) is set to 19, which gives a sampling rate of 774 kSPS. For conversion on the temperature sensor, the ADC acquisition time is automatically set to 16 clocks, and the ADC clock divider is set to 32. When using multiple channels, including the temperature sensor, the timing settings revert to the user-defined settings after reading the temperature sensor channel.

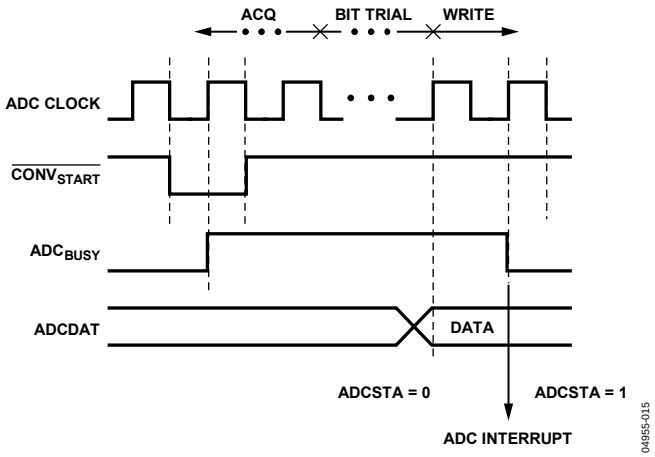

Figure 52. ADC Timing

ADuC7019

The ADuC7019 is identical to the ADuC7020 except for one buffered ADC channel, ADC3, and it has only three DACs. The output buffer of the fourth DAC is internally connected to the ADC3 channel as shown in Figure 53.

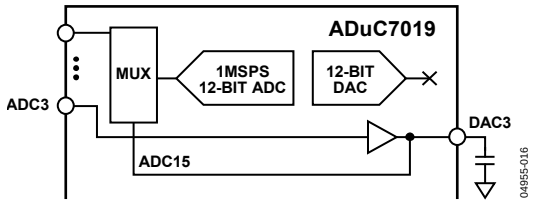

Figure 53. ADC3 Buffered Input

Note that the DAC3 output pin must be connected to a 10 nF capacitor to AGND. This channel should be used to measure dc voltages only. ADC calibration may be necessary on this channel.

MMRS INTERFACE

The ADC is controlled and configured via the eight MMRs described in this section.

Table 17. ADCCON Register

Name	Address	Default Value	Access
ADCCON	0xFFFF0500	0x0600	R/W

ADCCON is an ADC control register that allows the programmer to enable the ADC peripheral, select the mode of operation of the ADC (in single-ended mode, pseudo differential mode, or fully differential mode), and select the conversion type. This MMR is described in Table 18.

Table 18. ADCCON MMR Bit Designations

Bit	Value	Description
15:13		Reserved.
12:10		ADC clock speed.
	000	fADC/1. This divider is provided to obtain 1 MSPS ADC with an external clock <41.78 MHz.
	001	fADC/2 (default value).
	010	fADC/4.
	011	fADC/8.
	100	fADC/16.
	101	fADC/32.
9:8		ADC acquisition time.
	00	Two clocks.
	01	Four clocks.
	10	Eight clocks (default value).
	11	16 clocks.
7		Enable start conversion. Set by the user to start any type of conversion command. Cleared by the user to disable a start conversion (clearing this bit does not stop the ADC when continuously converting).
6		Reserved.
5		ADC power control. Set by the user to place the ADC in normal mode (the ADC must be powered up for at least 5 µs before it converts correctly). Cleared by the user to place the ADC in power-down mode.
4:3		Conversion mode.
	00	Single-ended mode.
	01	Differential mode.
	10	Pseudo differential mode.
	11	Reserved.
2:0		Conversion type.
	000	Enable $\overline{CONV}_{START}$ pin as a conversion input.
	001	Enable Timer1 as a conversion input.
	010	Enable Timer0 as a conversion input.
	011	Single software conversion. Sets to 000 after conversion (note that Bit 7 of ADCCON MMR should be cleared after starting a single software conversion to avoid further conversions triggered by the $\overline{CONV}_{START}$ pin).
	100	Continuous software conversion.
	101	PLA conversion.
	Other	Reserved.

Table 19. ADCCP Register

Name	Address	Default Value	Access
ADCCP	0xFFFF0504	0x00	R/W

ADCCP is an ADC positive channel selection register. This MMR is described in Table 20.

Table 20. ADCCP[1] MMR Bit Designation

Bit	Value	Description
7:5		Reserved.
4:0		Positive channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Temperature sensor.
	10001	AGND (self-diagnostic feature).
	10010	Internal reference (self-diagnostic feature).
	10011	$AV_{DD}/2$.
	Others	Reserved.

[1] ADC and DAC channel availability depends on the part model. See Ordering Guide for details.

Table 21. ADCCN Register

Name	Address	Default Value	Access
ADCCN	0xFFFF0508	0x01	R/W

ADCCN is an ADC negative channel selection register. This MMR is described in Table 22.

SECURITY

The 62 kB of Flash/EE memory available to the user can be read and write protected.

Bit 31 of the FEEPRO/FEEHIDE MMR (see Table 42) protects the 62 kB from being read through JTAG programming mode. The other 31 bits of this register protect writing to the flash memory. Each bit protects four pages, that is, 2 kB. Write protection is activated for all types of access.

Three Levels of Protection

- Protection can be set and removed by writing directly into FEEHIDE MMR. This protection does not remain after reset.
- Protection can be set by writing into the FEEPRO MMR. It takes effect only after a save protection command (0x0C) and a reset. The FEEPRO MMR is protected by a key to avoid direct access. The key is saved once and must be entered again to modify FEEPRO. A mass erase sets the key back to 0xFFFF but also erases all the user code.
- Flash can be permanently protected by using the FEEPRO MMR and a particular value of key: 0xDEADDEAD. Entering the key again to modify the FEEPRO register is not allowed.

Sequence to Write the Key

1. Write the bit in FEEPRO corresponding to the page to be protected.
2. Enable key protection by setting Bit 6 of FEEMOD (Bit 5 must equal 0).
3. Write a 32-bit key in FEEADR and FEEDAT.
4. Run the write key command 0x0C in FEECON; wait for the read to be successful by monitoring FEESTA.
5. Reset the part.

To remove or modify the protection, the same sequence is used with a modified value of FEEPRO. If the key chosen is the value 0xDEAD, the memory protection cannot be removed. Only a mass erase unprotects the part, but it also erases all user code.

The sequence to write the key is illustrated in the following example (this protects writing Page 4 to Page 7 of the Flash):

```
FEEPRO=0xFFFFFFFD;     //Protect pages 4 to 7
FEEMOD=0x48;           //Write key enable
FEEADR=0x1234;         //16 bit key value
FEEDAT=0x5678;         //16 bit key value
FEECON= 0x0C;          // Write key command
```

The same sequence should be followed to protect the part permanently with FEEADR = 0xDEAD and FEEDAT = 0xDEAD.

FLASH/EE CONTROL INTERFACE

Serial and JTAG programming use the Flash/EE control interface, which includes the eight MMRs outlined in this section.

Table 31. FEESTA Register

Name	Address	Default Value	Access
FEESTA	0xFFFFF800	0x20	R

FEESTA is a read-only register that reflects the status of the flash control interface as described in Table 32.

Table 32. FEESTA MMR Bit Designations

Bit	Description
15:6	Reserved.
5	Reserved.
4	Reserved.
3	Flash interrupt status bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEEMOD register is set. Cleared when reading the FEESTA register.
2	Flash/EE controller busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.
1	Command fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading the FEESTA register.
0	Command pass. Set by the MicroConverter when a command completes successfully. Cleared automatically when reading the FEESTA register.

Table 33. FEEMOD Register

Name	Address	Default Value	Access
FEEMOD	0xFFFFF804	0x0000	R/W

FEEMOD sets the operating mode of the flash control interface. Table 34 shows FEEMOD MMR bit designations.

Table 34. FEEMOD MMR Bit Designations

Bit	Description
15:9	Reserved.
8	Reserved. This bit should always be set to 0.
7:5	Reserved. These bits should always be set to 0 except when writing keys. See the Sequence to Write the Key section.
4	Flash/EE interrupt enable. Set by user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by user to disable the Flash/EE interrupt.
3	Erase/write command protection. Set by user to enable the erase and write commands. Cleared to protect the Flash against the erase/write command.
2:0	Reserved. These bits should always be set to 0.

Reset Operation

There are four kinds of reset: external, power-on, watchdog expiration, and software force. The RSTSTA register indicates the source of the last reset, and RSTCLR allows clearing of the RSTSTA register. These registers can be used during a reset exception service routine to identify the source of the reset. If RSTSTA is null, the reset is external.

Table 44. REMAP Register

Name	Address	Default Value	Access
REMAP	0xFFFF0220	0xXX[1]	R/W

[1] Depends on the model.

Table 45. REMAP MMR Bit Designations

Bit	Name	Description
4		Read-only bit. Indicates the size of the Flash/EE memory available. If this bit is set, only 32 kB of Flash/EE memory is available.
3		Read-only bit. Indicates the size of the SRAM memory available. If this bit is set, only 4 kB of SRAM is available.
2:1		Reserved.
0	Remap	Remap bit. Set by user to remap the SRAM to Address 0x00000000. Cleared automatically after reset to remap the Flash/EE memory to Address 0x00000000.

Table 46. RSTSTA Register

Name	Address	Default Value	Access
RSTSTA	0xFFFF0230	0x01	R/W

Table 47. RSTSTA MMR Bit Designations

Bit	Description
7:3	Reserved.
2	Software reset. Set by user to force a software reset. Cleared by setting the corresponding bit in RSTCLR.
1	Watchdog timeout. Set automatically when a watchdog timeout occurs. Cleared by setting the corresponding bit in RSTCLR.
0	Power-on reset. Set automatically when a power-on reset occurs. Cleared by setting the corresponding bit in RSTCLR.

Table 48. RSTCLR Register

Name	Address	Default Value	Access
RSTCLR	0xFFFF0234	0x00	W

Note that to clear the RSTSTA register, the user must write 0x07 to the RSTCLR register.

OTHER ANALOG PERIPHERALS

DAC

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate two, three, or four 12-bit voltage output DACs on-chip, depending on the model. Each DAC has a rail-to-rail voltage output buffer capable of driving 5 kΩ/100 pF.

Each DAC has three selectable ranges: 0 V to V_{REF} (internal band gap 2.5 V reference), 0 V to DAC_{REF}, and 0 V to AV_{DD}. DAC_{REF} is equivalent to an external reference for the DAC. The signal range is 0 V to AV_{DD}.

MMRs Interface

Each DAC is independently configurable through a control register and a data register. These two registers are identical for the four DACs. Only DAC0CON (see Table 50) and DAC0DAT (see Table 52) are described in detail in this section.

Table 49. DACxCON Registers

Name	Address	Default Value	Access
DAC0CON	0xFFFF0600	0x00	R/W
DAC1CON	0xFFFF0608	0x00	R/W
DAC2CON	0xFFFF0610	0x00	R/W
DAC3CON	0xFFFF0618	0x00	R/W

Table 50. DAC0CON MMR Bit Designations

Bit	Name	Value	Description
7:6			Reserved.
5	DACCLK		DAC update rate. Set by user to update the DAC using Timer1. Cleared by user to update the DAC using HCLK (core clock).
4	DACCLR		DAC clear bit. Set by user to enable normal DAC operation. Cleared by user to reset data register of the DAC to 0.
3			Reserved. This bit should be left at 0.
2			Reserved. This bit should be left at 0.
1:0			DAC range bits.
		00	Power-down mode. The DAC output is in three-state.
		01	0 V to DAC_{REF} range.
		10	0 V to V_{REF} (2.5 V) range.
		11	0 V to AV_{DD} range.

Table 51. DACxDAT Registers

Name	Address	Default Value	Access
DAC0DAT	0xFFFF0604	0x00000000	R/W
DAC1DAT	0xFFFF060C	0x00000000	R/W
DAC2DAT	0xFFFF0614	0x00000000	R/W
DAC3DAT	0xFFFF061C	0x00000000	R/W

Table 52. DAC0DAT MMR Bit Designations

Bit	Description
31:28	Reserved.
27:16	12-bit data for DAC0.
15:0	Reserved.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier. The functional equivalent is shown in Figure 63.

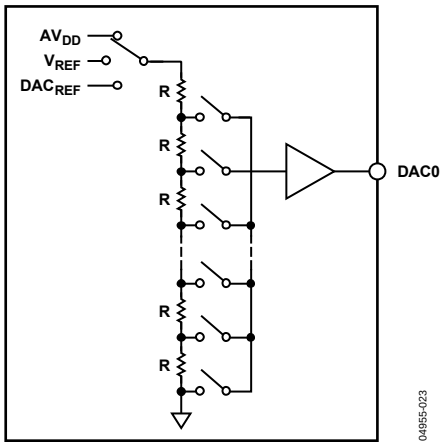

Figure 63. DAC Structure

As illustrated in Figure 63, the reference source for each DAC is user-selectable in software. It can be AV_{DD}, V_{REF}, or DAC_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-DAC_{REF} mode, the DAC output transfer function spans from 0 V to the voltage at the DAC_{REF} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 2.5 V reference, V_{REF}.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function, except Code 0 to Code 100, and, in 0-to-AV_{DD} mode only, Code 3995 to Code 4095.

Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is one-half the width of the hysteresis range.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 56.

Table 55. CMPCON Register

Name	Address	Default Value	Access
CMPCON	0xFFFF0444	0x0000	R/W

Table 56. CMPCON MMR Bit Descriptions

Bit	Name	Value	Description
15:11			Reserved.
10	CMPEN		Comparator enable bit. Set by user to enable the comparator. Cleared by user to disable the comparator.
9:8	CMPIN		Comparator negative input select bits.
		00	$AV_{DD}/2$.
		01	ADC3 input.
		10	DAC0 output.
		11	Reserved.
7:6	CMPOC		Comparator output configuration bits.
		00	Reserved.
		01	Reserved.
		10	Output on CMP_{OUT}.
		11	IRQ.
5	CMPOL		Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
4:3	CMPRES		Response time.
		00	5 µs response time is typical for large signals (2.5 V differential). 17 µs response time is typical for small signals (0.65 mV differential).
		11	3 µs typical.
		01/10	Reserved.
2	CMPHYST		Comparator hysteresis bit. Set by user to have a hysteresis of about 7.5 mV. Cleared by user to have no hysteresis.
1	CMPORI		Comparator output rising edge interrupt. Set automatically when a rising edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.
0	CMPOFI		Comparator output falling edge interrupt. Set automatically when a falling edge occurs on the monitored voltage (CMP0). Cleared by user.

OSCILLATOR AND PLL—POWER CONTROL

Clocking System

Each ADuC7019/20/21/22/24/25/26/27/28/29 integrates a 32.768 kHz ±3% oscillator, a clock divider, and a PLL. The PLL locks onto a multiple (1275) of the internal oscillator or an external 32.768 kHz crystal to provide a stable 41.78 MHz clock (UCLK) for the system. To allow power saving, the core can operate at this frequency, or at binary submultiples of it. The actual core operating frequency, $UCLK/2^{CD}$, is refered to as HCLK. The default core clock is the PLL clock divided by 8 (CD = 3) or 5.22 MHz. The core clock frequency can also come from an external clock on the ECLK pin as described in Figure 67. The core clock can be outputted on ECLK when using an internal oscillator or external crystal.

Note that when the ECLK pin is used to output the core clock, the output signal is not buffered and is not suitable for use as a clock source to an external device without an external buffer.

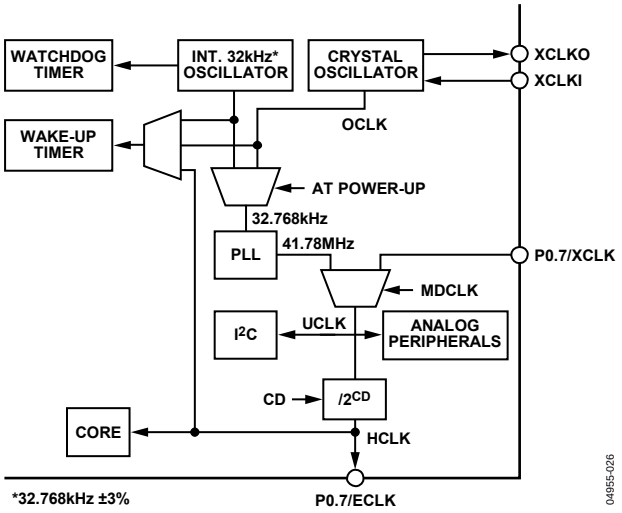

Figure 67. Clocking System

The selection of the clock source is in the PLLCON register. By default, the part uses the internal oscillator feeding the PLL.

External Crystal Selection

To switch to an external crystal, the user must do the following:

1. Enable the Timer2 interrupt and configure it for a timeout period of >120 µs.
2. Follow the write sequence to the PLLCON register, setting the MDCLK bits to 01 and clearing the OSEL bit.
3. Force the part into NAP mode by following the correct write sequence to the POWCON register.

   When the part is interrupted from NAP mode by the Timer2 interrupt source, the clock source has switched to the external clock.

DIGITAL PERIPHERALS

3-PHASE PWM

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides a flexible and programmable, 3-phase pulse-width modulation (PWM) waveform generator. It can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor control (ACIM). Note that only active high patterns can be produced.

The PWM generator produces three pairs of PWM signals on the six PWM output pins ($PWM0_H$, $PWM0_L$, $PWM1_H$, $PWM1_L$, $PWM2_H$, and $PWM2_L$). The six PWM output signals consist of three high-side drive signals and three low-side drive signals.

The switching frequency and dead time of the generated PWM patterns are programmable using the PWMDAT0 and PWMDAT1 MMRs. In addition, three duty-cycle control registers (PWMCH0, PWMCH1, and PWMCH2) directly control the duty cycles of the three pairs of PWM signals.

Each of the six PWM output signals can be enabled or disabled by separate output enable bits of the PWMEN register. In addition, three control bits of the PWMEN register permit crossover of the two signals of a PWM pair. In crossover mode, the PWM signal destined for the high-side switch is diverted to the complementary low-side output. The signal destined for the low-side switch is diverted to the corresponding high-side output signal.

In many applications, there is a need to provide an isolation barrier in the gate-drive circuits that turn on the inverter power devices. In general, there are two common isolation techniques: optical isolation using optocouplers and transformer isolation using pulse transformers. The PWM controller permits mixing of the output PWM signals with a high frequency chopping signal to permit easy interface to such pulse transformers. The features of this gate-drive chopping mode can be controlled by the PWMCFG register. An 8-bit value within the PWMCFG register directly controls the chopping frequency. High frequency chopping can be independently enabled for the high-side and low-side outputs using separate control bits in the PWMCFG register.

The PWM generator can operate in one of two distinct modes: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period so that the resulting PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM duty cycle values is implemented at the midpoint of the PWM period.

In double update mode, it is also possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters. This technique permits closed-loop controllers to change the average voltage applied to the machine windings at a faster rate. As a result, faster closed-loop bandwidths are achieved. The operating mode of the PWM block is selected by a control bit in the PWMCON register. In single update mode, an internal synchronization pulse, PWMSYNC, is produced at the start of each PWM period. In double update mode, an additional PWMSYNC pulse is produced at the midpoint of each PWM period.

The PWM block can also provide an internal synchronization pulse on the PWM_{SYNC} pin that is synchronized to the PWM switching frequency. In single update mode, a pulse is produced at the start of each PWM period. In double update mode, an additional pulse is produced at the mid-point of each PWM period. The width of the pulse is programmable through the PWMDAT2 register. The PWM block can also accept an external synchronization pulse on the PWM_{SYNC} pin. The selection of external synchronization or internal synchronization is in the PWMCON register. The SYNC input timing can be synchronized to the internal peripheral clock, which is selected in the PWMCON register. If the external synchronization pulse from the chip pin is asynchronous to the internal peripheral clock (typical case), the external PWMSYNC is considered asynchronous and should be synchronized. The synchronization logic adds latency and jitter from the external pulse to the actual PWM outputs. The size of the pulse on the PWM_{SYNC} pin must be greater than two core clock periods.

The PWM signals produced by the ADuC7019/20/21/22/24/25/26/27/28/29 can be shut off via a dedicated asynchronous PWM shutdown pin, PWM_{TRIP}. When brought low, PWM_{TRIP} instantaneously places all six PWM outputs in the off state (high). This hardware shutdown mechanism is asynchronous so that the associated PWM disable circuitry does not go through any clocked logic. This ensures correct PWM shutdown even in the event of a core clock loss.

Status information about the PWM system is available to the user in the PWMSTA register. In particular, the state of the PWM_{TRIP} pin is available, as well as a status bit that indicates whether operation is in the first half or the second half of the PWM period.

40-Pin Package Devices

On the 40-pin package devices, the PWM outputs are not directly accessible, as described in the General-Purpose Input/Output section. One channel can be brought out on a GPIO (see Table 78) via the PLA as shown in the following example:

```
PWMCON = 0x1;           // enables PWM o/p
PWMDAT0 = 0x055F;       // PWM switching freq
// Configure Port Pins
GP4CON = 0x300;         // P4.2 as PLA output
GP3CON = 0x1;           // P3.0 configured as
                        // output of PWM0
                        //(internally)
// PWM0 onto P4.2
PLAELM8 = 0x0035;       // P3.0 (PWM output)
                        // input of element 8
PLAELM10 = 0x0059;      // PWM from element 8
```

Output Control Unit

The operation of the output control unit is controlled by the 9-bit read/write PWMEN register. This register controls two distinct features of the output control unit that are directly useful in the control of electronic counter measures (ECM) or binary decimal counter measures (BDCM). The PWMEN register contains three crossover bits, one for each pair of PWM outputs. Setting Bit 8 of the PWMEN register enables the crossover mode for the 0H/0L pair of PWM signals, setting Bit 7 enables crossover on the 1H/1L pair of PWM signals, and setting Bit 6 enables crossover on the 2H/2L pair of PWM signals. If crossover mode is enabled for any pair of PWM signals, the high-side PWM signal from the timing unit (0H, for example) is diverted to the associated low-side output of the output control unit so that the signal ultimately appears at the $PWM0_L$ pin. Of course, the corresponding low-side output of the timing unit is also diverted to the complementary high-side output of the output control unit so that the signal appears at the $PWM0_H$ pin. Following a reset, the three crossover bits are cleared, and the crossover mode is disabled on all three pairs of PWM signals. The PWMEN register also contains six bits (Bit 0 to Bit 5) that can be used to individually enable or disable each of the six PWM outputs. If the associated bit of the PWMEN register is set, the corresponding PWM output is disabled regardless of the corresponding value of the duty cycle register. This PWM output signal remains in the off state as long as the corresponding enable/disable bit of the PWMEN register is set. The implementation of this output enable function is implemented after the crossover function.

Following a reset, all six enable bits of the PWMEN register are cleared, and all PWM outputs are enabled by default. In a manner identical to the duty cycle registers, the PWMEN is latched on the rising edge of the PWMSYNC signal. As a result, changes to this register become effective only at the start of each PWM cycle in single update mode. In double update mode, the PWMEN register can also be updated at the midpoint of the PWM cycle.

In the control of an ECM, only two inverter legs are switched at any time, and often the high-side device in one leg must be switched on at the same time as the low-side driver in a second leg. Therefore, by programming identical duty cycle values for two PWM channels (for example, PWMCH0 = PWMCH1) and setting Bit 7 of the PWMEN register to cross over the 1H/1L pair of PWM signals, it is possible to turn on the high-side switch of Phase A and the low-side switch of Phase B at the same time. In the control of ECM, it is usual for the third inverter leg (Phase C in this example) to be disabled for a number of PWM cycles. This function is implemented by disabling both the 2H and 2L PWM outputs by setting Bit 0 and Bit 1 of the PWMEN register.

This situation is illustrated in Figure 71, where it can be seen that both the 0H and 1L signals are identical because PWMCH0 = PWMCH1 and the crossover bit for Phase B is set.

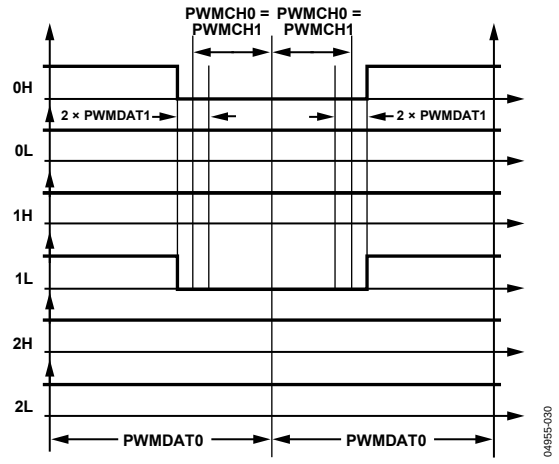

Figure 71. Active Low PWM Signals Suitable for ECM Control, PWMCH0 = PWMCH1, Crossover 1H/1L Pair and Disable 0L, 1H, 2H, and 2L Outputs in Single Update Mode.

In addition, the other four signals (0L, 1H, 2H, and 2L) have been disabled by setting the appropriate enable/disable bits of the PWMEN register. In Figure 71, the appropriate value for the PWMEN register is 0x00A7. In normal ECM operation, each inverter leg is disabled for certain periods of time to change the PWMEN register based on the position of the rotor shaft (motor commutation).

Gate Drive Unit

The gate drive unit of the PWM controller adds features that simplify the design of isolated gate-drive circuits for PWM inverters. If a transformer-coupled, power device, gate-drive amplifier is used, the active PWM signal must be chopped at a high frequency. The 16-bit read/write PWMCFG register programs this high frequency chopping mode. The chopped active PWM signals can be required for the high-side drivers only, the low-side drivers only, or both the high-side and low-side switches. Therefore, independent control of this mode for both high-side and low-side switches is included with two separate control bits in the PWMCFG register.

Typical PWM output signals with high frequency chopping enabled on both high-side and low-side signals are shown in Figure 72. Chopping of the high-side PWM outputs (0H, 1H, and 2H) is enabled by setting Bit 8 of the PWMCFG register. Chopping of the low-side PWM outputs (0L, 1L, and 2L) is enabled by setting Bit 9 of the PWMCFG register. The high chopping frequency is controlled by the 8-bit word (GDCLK) placed in Bit 0 to Bit 7 of the PWMCFG register. The period of this high frequency carrier is

$$t_{CHOP} = (4 \times (GDCLK + 1)) \times t_{CORE}$$

The chopping frequency is, therefore, an integral subdivision of the MicroConverter core frequency

$$f_{CHOP} = f_{CORE}/(4 \times (GDCLK + 1))$$

Table 85. GPxDAT Registers

Name	Address	Default Value[1]	Access
GP0DAT	0xFFFFF420	0x000000XX	R/W
GP1DAT	0xFFFFF430	0x000000XX	R/W
GP2DAT	0xFFFFF440	0x000000XX	R/W
GP3DAT	0xFFFFF450	0x000000XX	R/W
GP4DAT	0xFFFFF460	0x000000XX	R/W

[1] X = 0, 1, 2, or 3.

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins configured as output, and store the input value of the pins configured as input.

Table 86. GPxDAT MMR Bit Descriptions

Bit	Description
31:24	Direction of the data. Set to 1 by user to configure the GPIO pin as an output. Cleared to 0 by user to configure the GPIO pin as an input.
23:16	Port x data output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x data input (read only).

Table 87. GPxSET Registers

Name	Address	Default Value[1]	Access
GP0SET	0xFFFFF424	0x000000XX	W
GP1SET	0xFFFFF434	0x000000XX	W
GP2SET	0xFFFFF444	0x000000XX	W
GP3SET	0xFFFFF454	0x000000XX	W
GP4SET	0xFFFFF464	0x000000XX	W

[1] X = 0, 1, 2, or 3.

GPxSET are data set Port x registers.

Table 88. GPxSET MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x set bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

Table 89. GPxCLR Registers

Name	Address	Default Value[1]	Access
GP0CLR	0xFFFFF428	0x000000XX	W
GP1CLR	0xFFFFF438	0x000000XX	W
GP2CLR	0xFFFFF448	0x000000XX	W
GP3CLR	0xFFFFF458	0x000000XX	W
GP4CLR	0xFFFFF468	0x000000XX	W

[1] X = 0, 1, 2, or 3.

GPxCLR are data clear Port x registers.

Table 90. GPxCLR MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x clear bit. Set to 1 by user to clear bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

SERIAL PORT MUX

The serial port mux multiplexes the serial port peripherals (an SPI, UART, and two I^2Cs) and the programmable logic array (PLA) to a set of 10 GPIO pins. Each pin must be configured to one of its specific I/O functions as described in Table 91.

Table 91. SPM Configuration

SPMMUX	GPIO (00)	UART (01)	UART/I^2C/SPI (10)	PLA (11)
SPM0	P1.0	SIN	I2C0SCL	PLAI[0]
SPM1	P1.1	SOUT	I2C0SDA	PLAI[1]
SPM2	P1.2	RTS	I2C1SCL	PLAI[2]
SPM3	P1.3	CTS	I2C1SDA	PLAI[3]
SPM4	P1.4	RI	SCLK	PLAI[4]
SPM5	P1.5	DCD	MISO	PLAI[5]
SPM6	P1.6	DSR	MOSI	PLAI[6]
SPM7	P1.7	DTR	$\overline{CS}$	PLAO[0]
SPM8	P0.7	ECLK/XCLK	SIN	PLAO[4]
SPM9	P2.0	CONV	SOUT	PLAO[5]

Table 91 also details the mode for each of the SPMMUX pins. This configuration must be done via the GP0CON, GP1CON, and GP2CON MMRs. By default, these 10 pins are configured as GPIOs.

UART SERIAL INTERFACE

The UART peripheral is a full-duplex, universal, asynchronous receiver/transmitter. It is fully compatible with the 16,450 serial port standard. The UART performs serial-to-parallel conversions on data characters received from a peripheral device or modem, and parallel-to-serial conversions on data characters received from the CPU. The UART includes a fractional divider for baud rate generation and has a network addressable mode. The UART function is made available on the 10 pins of the ADuC7019/20/21/22/24/25/26/27/28/29 (see Table 92).

Table 92. UART Signal Description

Pin	Signal	Description
SPM0 (Mode 1)	SIN	Serial receive data.
SPM1 (Mode 1)	SOUT	Serial transmit data.
SPM2 (Mode 1)	RTS	Request to send.
SPM3 (Mode 1)	CTS	Clear to send.
SPM4 (Mode 1)	RI	Ring indicator.
SPM5 (Mode 1)	DCD	Data carrier detect.
SPM6 (Mode 1)	DSR	Data set ready.
SPM7 (Mode 1)	DTR	Data terminal ready.
SPM8 (Mode 2)	SIN	Serial receive data.
SPM9 (Mode 2)	SOUT	Serial transmit data.

Table 137. I2CxALT Registers

Name	Address	Default Value	Access
I2C0ALT	0xFFFF0828	0x00	R/W
I2C1ALT	0xFFFF0928	0x00	R/W

I2CxALT are hardware general call ID registers used in slave mode.

Table 138. I2CxCFG Registers

Name	Address	Default Value	Access
I2C0CFG	0xFFFF082C	0x00	R/W
I2C1CFG	0xFFFF092C	0x00	R/W

I2CxCFG are configuration registers.

Table 139. I2C0CFG MMR Bit Descriptions

Bit	Description
31:5	Reserved. These bits should be written by the user as 0.
14	Enable stop interrupt. Set by the user to generate an interrupt upon receiving a stop condition and after receiving a valid start condition and matching address. Cleared by the user to disable the generation of an interrupt upon receiving a stop condition.
13	Reserved.
12	Reserved.
11	Enable stretch SCL (holds SCL low). Set by the user to stretch the SCL line. Cleared by the user to disable stretching of the SCL line.
10	Reserved.
9	Slave Tx FIFO request interrupt enable. Set by the user to disable the slave Tx FIFO request interrupt. Cleared by the user to generate an interrupt request just after the negative edge of the clock for the R/W bit. This allows the user to input data into the slave Tx FIFO if it is empty. At 400 ksps and the core clock running at 41.78 MHz, the user has 45 clock cycles to take appropriate action, taking interrupt latency into account.
8	General call status bit clear. Set by the user to clear the general call status bits. Cleared automatically by hardware after the general call status bits are cleared.
7	Master serial clock enable bit. Set by user to enable generation of the serial clock in master mode. Cleared by user to disable serial clock in master mode.
6	Loopback enable bit. Set by user to internally connect the transition to the reception to test user software. Cleared by user to operate in normal mode.
5	Start backoff disable bit. Set by user in multimaster mode. If losing arbitration, the master immediately tries to retransmit. Cleared by user to enable start backoff. After losing arbitration, the master waits before trying to retransmit.
4	Hardware general call enable. When this bit and Bit 3 are set and have received a general call (Address 0x00) and a data byte, the device checks the contents of I2C0ALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a "to whom it may concern" call. The ADuC7019/20/21/22/24/25/26/27/28/29 watch for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2C0ALT register should always be written to 1, as indicated in *The I²C-Bus Specification*, January 2000, from NXP.
3	General call enable bit. This bit is set by the user to enable the slave device to acknowledge (ACK) an I²C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of slave address by hardware) as the data byte, the I²C interface resets as as indicated in *The I²C-Bus Specification,* January 2000, from NXP. This command can be used to reset an entire I²C system. The general call interrupt status bit sets on any general call. The user must take corrective action by setting up the I²C interface after a reset. If it receives a 0x04 (write programmable part of slave address by hardware) as the data byte, the general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address.
2	Reserved.
1	Master enable bit. Set by user to enable the master I²C channel. Cleared by user to disable the master I²C channel.
0	Slave enable bit. Set by user to enable the slave I²C channel. A slave transfer sequence is monitored for the device address in I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3. At 400 kSPs, the core clock should run at 41.78 MHz because the interrupt latency could be up to 45 clock cycles alone. After the I²C read bit, the user has 0.5 of an I²C clock cycle to load the Tx FIFO. AT 400 kSPS, this is 1.26 µs, the interrupt latency.

Table 153. PLAADC Register

Name	Address	Default Value	Access
PLAADC	0xFFFF0B48	0x00000000	R/W

PLAADC is the PLA source for the ADC start conversion signal.

Table 154. PLAADC MMR Bit Descriptions

Bit	Value	Description
31:5		Reserved.
4		ADC start conversion enable bit. Set by user to enable ADC start conversion from PLA. Cleared by user to disable ADC start conversion from PLA.
3:0		ADC start conversion source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 155. PLADIN Register

Name	Address	Default Value	Access
PLADIN	0xFFFF0B4C	0x00000000	R/W

PLADIN is a data input MMR for PLA.

Table 156. PLADIN MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Input bit to Element 15 to Element 0.

Table 157. PLADOUT Register

Name	Address	Default Value	Access
PLADOUT	0xFFFF0B50	0x00000000	R

PLADOUT is a data output MMR for PLA. This register is always updated.

Table 158. PLADOUT MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Output bit from Element 15 to Element 0.

Table 159. PLALCK Register

Name	Address	Default Value	Access
PLALCK	0xFFFF0B54	0x00	W

PLALCK is a PLA lock option. Bit 0 is written only once. When set, it does not allow modifying any of the PLA MMRs, except PLADIN. A PLA tool is provided in the development system to easily configure the PLA.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 23 interrupt sources on the ADuC7019/20/21/22/24/25/26/27/28/29 that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals, such as ADC and UART. Four additional interrupt sources are generated from external interrupt request pins, IRQ0, IRQ1, IRQ2, and IRQ3. The ARM7TDMI CPU core only recognizes interrupts as one of two types: a normal interrupt request IRQ or a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system are managed through nine interrupt-related registers, four dedicated to IRQ, and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ register (except for Bit 23) represent the same interrupt source as described in Table 160.

Table 160. IRQ/FIQ MMRs Bit Description

Bit	Description
0	All interrupts OR'ed (FIQ only)
1	SWI
2	Timer0
3	Timer1
4	Wake-up timer (Timer2)
5	Watchdog timer (Timer3)
6	Flash control
7	ADC channel
8	PLL lock
9	I2C0 slave
10	I2C0 master
11	I2C1 master
12	SPI slave
13	SPI master
14	UART
15	External IRQ0
16	Comparator
17	PSM
18	External IRQ1
19	PLA IRQ0
20	PLA IRQ1
21	External IRQ2
22	External IRQ3
23	PWM trip (IRQ only)/PWM sync (FIQ only)

IRQ

The interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It is used to service general-purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are IRQSTA, IRQSIG, IRQEN, and IRQCLR.

Table 161. IRQSTA Register

Name	Address	Default Value	Access
IRQSTA	0xFFFF0000	0x00000000	R

IRQSTA (read-only register) provides the current-enabled IRQ source status. When set to 1, that source should generate an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically OR'ed to create the IRQ signal to the ARM7TDMI core.

Table 162. IRQSIG Register

Name	Address	Default Value	Access
IRQSIG	0xFFFF0004	0x00XXX000[1]	R

[1] X indicates an undefined value.

IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read only.

Table 163. IRQEN Register

Name	Address	Default Value	Access
IRQEN	0xFFFF0008	0x00000000	R/W

IRQEN provides the value of the current enable mask. When each bit is set to 1, the source request is enabled to create an IRQ exception. When each bit is set to 0, the source request is disabled or masked, which does not create an IRQ exception.

Note that to clear an already enabled interrupt source, the user must set the appropriate bit in the IRQCLR register. Clearing an interrupt's IRQEN bit does not disable the interrupt.

Table 164. IRQCLR Register

Name	Address	Default Value	Access
IRQCLR	0xFFFF000C	0x00000000	W

IRQCLR (write-only register) clears the IRQEN register in order to mask an interrupt source. Each bit set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, independently manipulates the enable mask without requiring an atomic read-modify-write.

ORDERING GUIDE

Model[1, 2]	ADC Channels[3]	DAC Channels	FLASH/ RAM	GPIO	Down-loader	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7019BCPZ62I	5	3	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7019BCPZ62I-RL	5	3	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7019BCPZ62IRL7	5	3	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62	5	4	62 kB/8 kB	14	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62-RL7	5	4	62 kB/8 kB	14	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62I	5	4	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62I-RL	5	4	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7020BCPZ62IRL7	5	4	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62-RL	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ62-RL7	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62I	8	2	62 kB/8 kB	13	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62I-RL	8	2	62 kB/8 kB	13	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ32	8	2	32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ32-RL7	8	2	32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ62	10		62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ62-RL7	10		62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ32	10		32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ32-RL	10		32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7024BCPZ62	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62-RL7	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	750
ADuC7024BCPZ62I	10	2	62 kB/8 kB	30	I²C	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62I-RL	10	2	62 kB/8 kB	30	I²C	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7024BSTZ62	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7024BSTZ62-RL	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7025BCPZ62	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ62-RL	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BCPZ32	12		32 kB/4 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ32-RL	12		32 kB/4 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BSTZ62	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7025BSTZ62-RL	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7026BSTZ62	12	4	62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62-RL	12	4	62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7026BSTZ62I	12	4	62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62I-RL	12	4	62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62	16		62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62-RL	16		62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62I	16		62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62I-RL	16		62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7028BBCZ62	8	4	62 kB/8 kB	30	UART	−40°C to +125°C	64-Ball CSP_BGA	BC-64-4	
ADuC7028BBCZ62-RL	8	4	62 kB/8 kB	30	UART	−40°C to +125°C	64-Ball CSP_BGA	BC-64-4	2,500
ADuC7029BBCZ62	7	4	62 kB/8 kB	22	UART	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62-RL	7	4	62 kB/8 kB	22	UART	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000
ADuC7029BBCZ62I	7	4	62 kB/8 kB	22	I²C	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62I-RL	7	4	62 kB/8 kB	22	I²C	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000