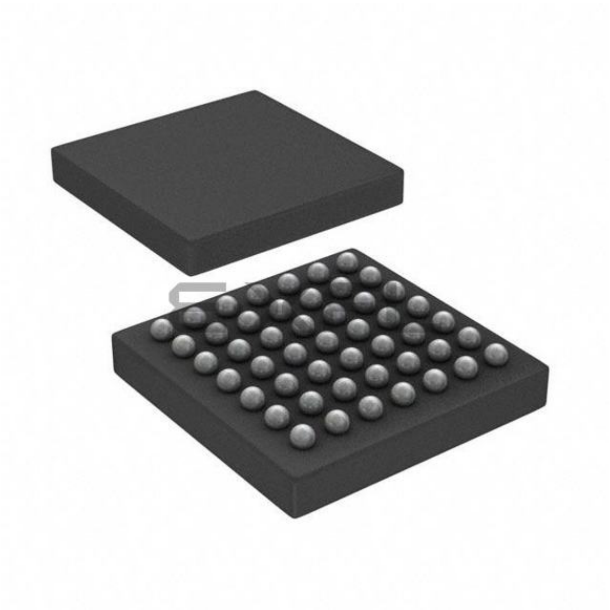

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	22
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	49-TFBGA, CSPBGA
Supplier Device Package	49-CSPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7029bbcz62

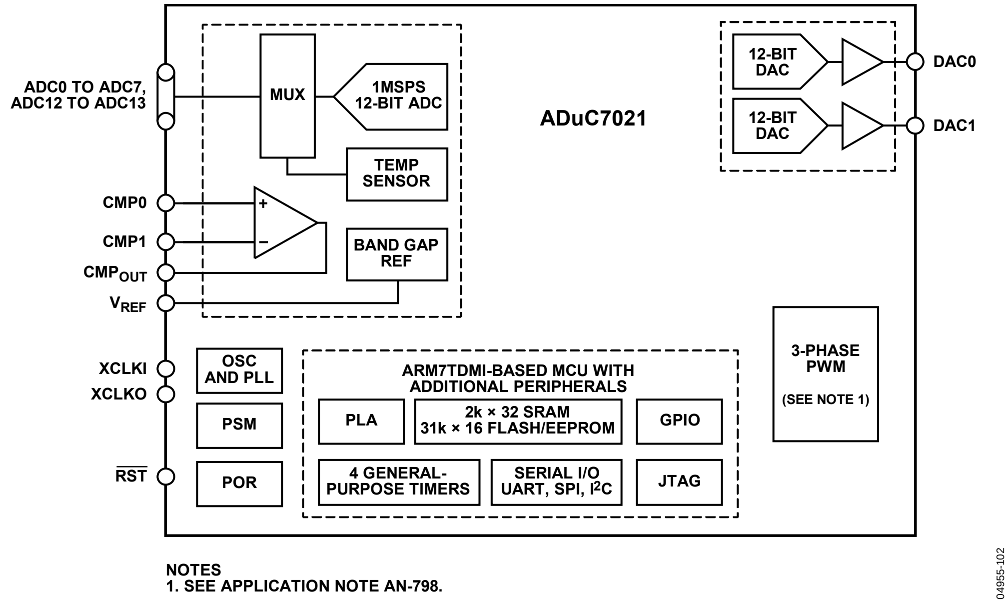

Figure 3.

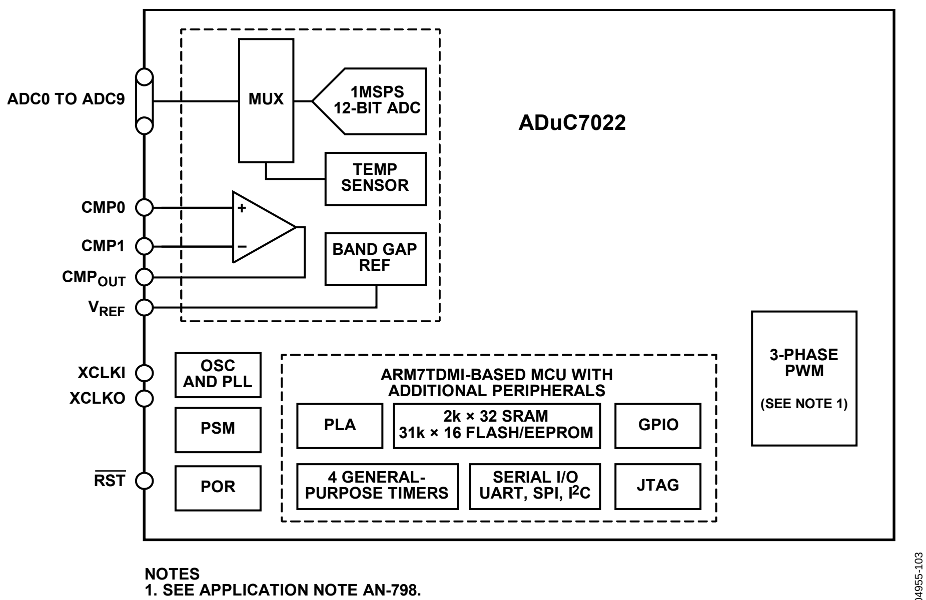

Figure 4.

DETAILED BLOCK DIAGRAM

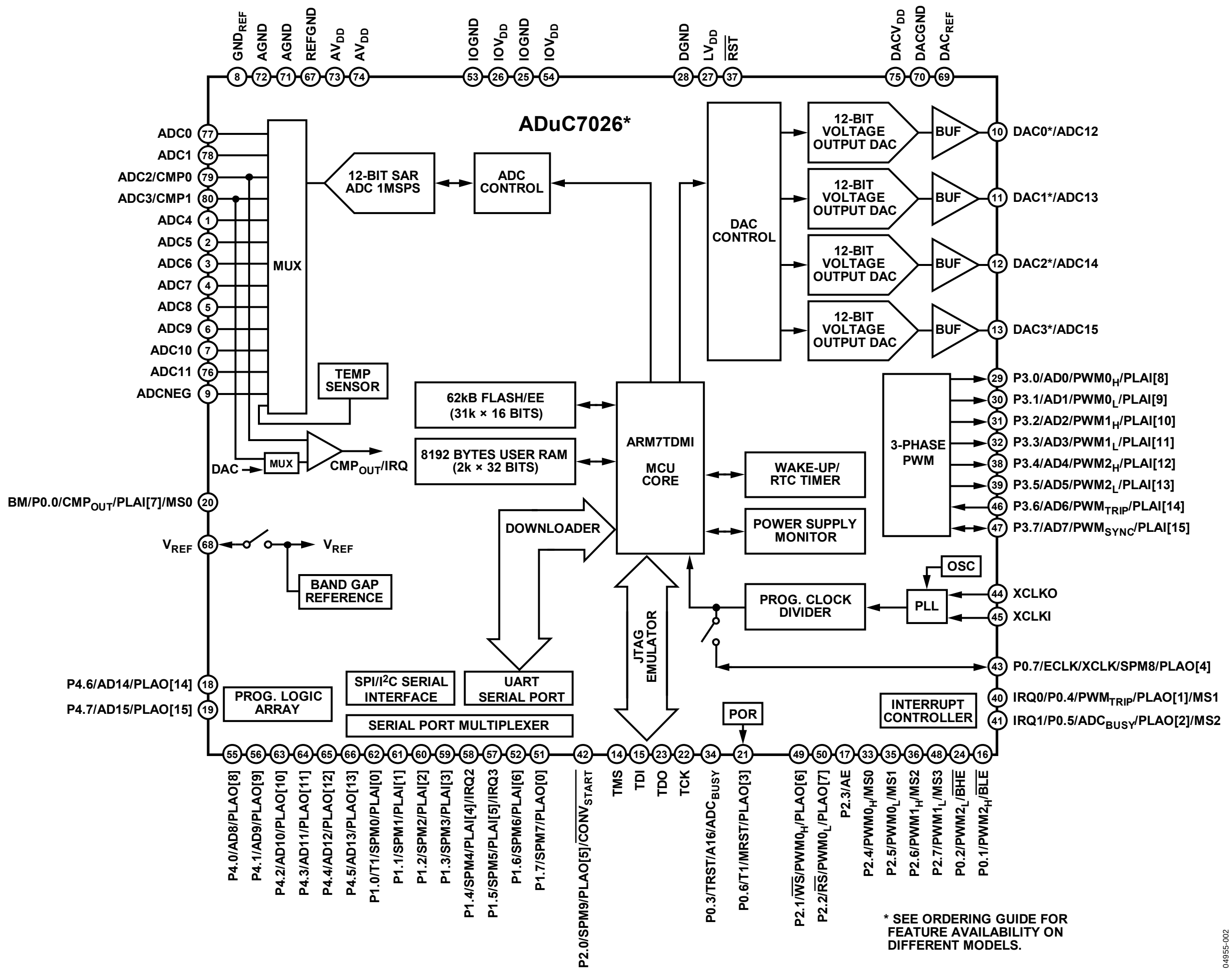

Figure 11.

SPECIFICATIONS

$AV_{DD} = IOV_{DD} = 2.7$ V to 3.6 V, $V_{REF} = 2.5$ V internal reference, $f_{CORE} = 41.78$ MHz, $T_A = -40°C$ to $+125°C$, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		μs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2	±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					$f_{IN} = 10$ kHz sine wave, $f_{SAMPLE} = 1$ MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise (PHSN)		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			V_{CM}[6] ± $V_{REF}/2$	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	μA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 μF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±5	mV	$T_A = 25°C$
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		70		Ω	$T_A = 25°C$
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					$R_L = 5$ kΩ, $C_L = 100$ pF
DC Accuracy[7]					
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range_0		0 to DAC_{REF}		V	DAC_{REF} range: DACGND to $DACV_{DD}$
Output Voltage Range_1		0 to 2.5		V	
Output Voltage Range_2		0 to $DACV_{DD}$		V	
Output Impedance		2		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC AC CHARACTERISTICS					
Voltage Output Settling Time		10		µs	
Digital-to-Analog Glitch Energy		±20		nV-sec	1 LSB change at major carry (where maximum number of bits simultaneously changes in the DACxDAT register)
COMPARATOR					
Input Offset Voltage		±15		mV	
Input Bias Current		1		µA	
Input Voltage Range	AGND		AV_{DD} − 1.2	V	
Input Capacitance		7		pF	
Hysteresis[4, 6]	2		15	mV	Hysteresis turned on or off via the CMPHYST bit in the CMPCON register
Response Time		3		µs	100 mV overdrive and configured with CMPRES = 11
TEMPERATURE SENSOR					
Voltage Output at 25°C		780		mV	
Voltage TC		−1.3		mV/°C	
Accuracy		±3		°C	
POWER SUPPLY MONITOR (PSM)					
IOV_{DD} Trip Point Selection		2.79		V	Two selectable trip points
		3.07		V	
Power Supply Trip Point Accuracy		±2.5		%	Of the selected nominal trip point voltage
POWER-ON-RESET		2.36		V	
GLITCH IMMUNITY ON RESET PIN[4]		50		µs	
WATCHDOG TIMER (WDT)					
Timeout Period	0		512	sec	
FLASH/EE MEMORY					
Endurance[9]	10,000			Cycles	
Data Retention[10]	20			Years	T_J = 85°C
DIGITAL INPUTS					All digital inputs excluding XCLKI and XCLKO
Logic 1 Input Current		±0.2	±1	µA	V_{IH} = IOV_{DD} or V_{IH} = 5 V
Logic 0 Input Current		−40	−60	µA	V_{IL} = 0 V; except TDI on ADuC7019/20/21/22/24/25/29
		−80	−120	µA	V_{IL} = 0 V; TDI on ADuC7019/20/21/22/24/25/29
Input Capacitance		10		pF	
LOGIC INPUTS[3]					All logic inputs excluding XCLKI
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.0			V	
LOGIC OUTPUTS					All digital outputs excluding XCLKO
V_{OH}, Output High Voltage	2.4			V	I_{SOURCE} = 1.6 mA
V_{OL}, Output Low Voltage[11]			0.4	V	I_{SINK} = 1.6 mA
CRYSTAL INPUTS XCLKI and XCLKO					
Logic Inputs, XCLKI Only					
V_{INL}, Input Low Voltage		1.1		V	
V_{INH}, Input High Voltage		1.7		V	
XCLKI Input Capacitance		20		pF	
XCLKO Output Capacitance		20		pF	
INTERNAL OSCILLATOR		32.768		kHz	
			±3	%	
			±2[4]	%	T_A = 0°C to 85°C range

Table 11. Pin Function Descriptions (ADuC7019/ADuC7020/ADuC7021/ADuC7022)

Pin No.				
7019/7020	7021	7022	Mnemonic	Description
38	37	36	ADC0	Single-Ended or Differential Analog Input 0.
39	38	37	ADC1	Single-Ended or Differential Analog Input 1.
40	39	38	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
1	40	39	ADC3/CMP1	Single-Ended or Differential Analog Input 3 (Buffered Input on ADuC7019)/ Comparator Negative Input.
2	1	40	ADC4	Single-Ended or Differential Analog Input 4.
–	2	1	ADC5	Single-Ended or Differential Analog Input 5.
–	3	2	ADC6	Single-Ended or Differential Analog Input 6.
–	4	3	ADC7	Single-Ended or Differential Analog Input 7.
–	–	4	ADC8	Single-Ended or Differential Analog Input 8.
–	–	5	ADC9	Single-Ended or Differential Analog Input 9.
3	5	6	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
4	6	–	DAC0/ADC12	DAC0 Voltage Output/Single-Ended or Differential Analog Input 12.
5	7	–	DAC1/ADC13	DAC1 Voltage Output/Single-Ended or Differential Analog Input 13.
6	–	–	DAC2/ADC14	DAC2 Voltage Output/Single-Ended or Differential Analog Input 14.
7	–	–	DAC3/ADC15	DAC3 Voltage Output on ADuC7020. On the ADuC7019, a 10 nF capacitor must be connected between this pin and AGND/Single-Ended or Differential Analog Input 15 (see Figure 53).
8	8	7	TMS	Test Mode Select, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases, an external pull-up resistor (~100K) is also required to ensure that the part does not enter an erroneous state.
9	9	8	TDI	Test Data In, JTAG Test Port Input. Debug and download access.
10	10	9	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot Mode (BM). The ADuC7019/20/21/22 enter serial download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
11	11	10	P0.6/T1/MRST/PLAO[3]	Multifunction Pin. Driven low after reset. General-Purpose Output Port 0.6/ Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
12	12	11	TCK	Test Clock, JTAG Test Port Input. Debug and download access. This pin has an internal pull-up resistor to IOV_{DD}. In some cases an external pull-up resistor (~100K) is also required to ensure that the part does not enter an erroneous state.
13	13	12	TDO	Test Data Out, JTAG Test Port Output. Debug and download access.
14	14	13	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
15	15	14	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
16	16	15	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
17	17	16	DGND	Ground for Core Logic.
18	18	17	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/Test Reset, JTAG Test Port Input/ ADC_{BUSY} Signal Output.
19	19	18	$\overline{RST}$	Reset Input, Active Low.
20	20	19	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
21	21	20	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

ADuC7024/ADuC7025

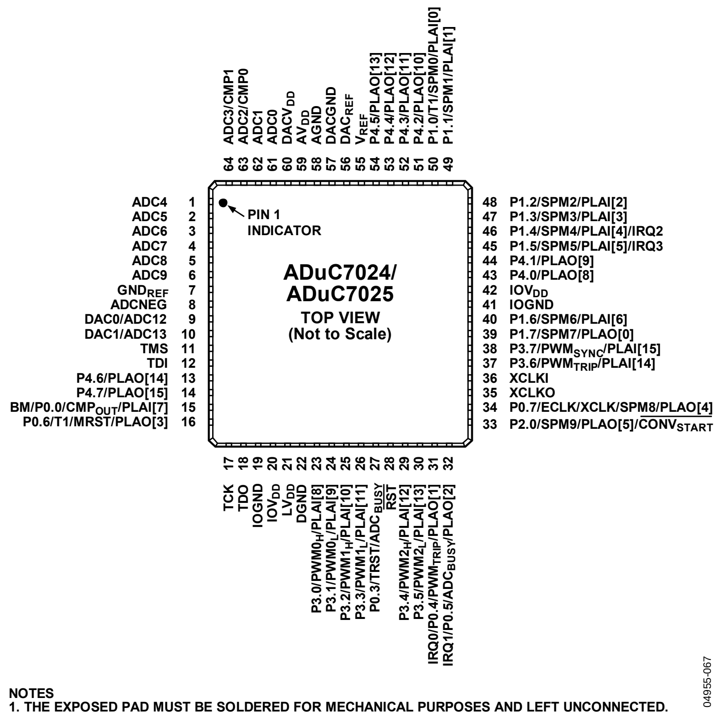

Figure 23. 64-Lead LFCSP_VQ Pin Configuration (ADuC7024/ADuC7025)

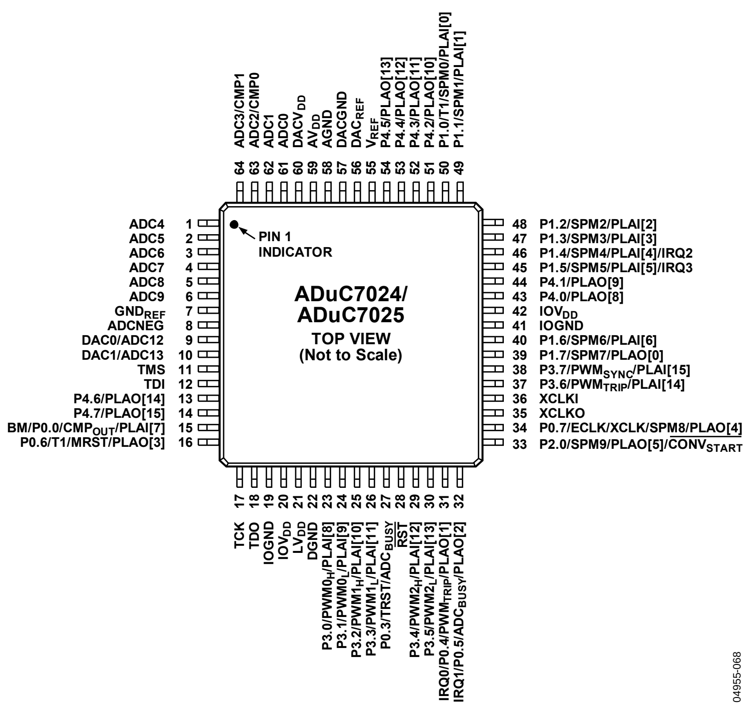

Figure 24. 64-Lead LQFP Pin Configuration (ADuC7024/ADuC7025)

Table 12. Pin Function Descriptions (ADuC7024/ADuC7025 64-Lead LFCSP_VQ and 64-Lead LQFP)

Pin No.	Mnemonic	Description
1	ADC4	Single-Ended or Differential Analog Input 4.
2	ADC5	Single-Ended or Differential Analog Input 5.
3	ADC6	Single-Ended or Differential Analog Input 6.
4	ADC7	Single-Ended or Differential Analog Input 7.
5	ADC8	Single-Ended or Differential Analog Input 8.
6	ADC9	Single-Ended or Differential Analog Input 9.
7	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
8	ADCNEG	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
9	DAC0/ADC12	DAC0 Voltage Output/Single-Ended or Differential Analog Input 12. DAC outputs are not present on the ADuC7025.
10	DAC1/ADC13	DAC1 Voltage Output/Single-Ended or Differential Analog Input 13. DAC outputs are not present on the ADuC7025.
11	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
12	TDI	JTAG Test Port Input, Test Data In. Debug and download access
13	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
14	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
15	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7024/ADuC7025 enter download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
16	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
17	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
18	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
19	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
20	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
21	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
22	DGND	Ground for Core Logic.
23	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
24	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
25	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
26	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
27	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
28	$\overline{RST}$	Reset Input, Active Low.
29	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
30	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
31	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
32	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.
33	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
34	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
35	XCLKO	Output from the Crystal Oscillator Inverter.
36	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.

Pin No.	Mnemonic	Description
37	P3.6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
38	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization Input and Output/ Programmable Logic Array Input Element 15.
39	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
40	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
41	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
42	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
43	P4.0/PLAO[8]	General-Purpose Input and Output Port 4.0/Programmable Logic Array Output Element 8.
44	P4.1/PLAO[9]	General-Purpose Input and Output Port 4.1/Programmable Logic Array Output Element 9.
45	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
46	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
47	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
48	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
49	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
50	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
51	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
52	P4.3/PLAO[11]	General-Purpose Input and Output Port 4.3/Programmable Logic Array Output Element 11.
53	P4.4/PLAO[12]	General-Purpose Input and Output Port 4.4/Programmable Logic Array Output Element 12.
54	P4.5/PLAO[13]	General-Purpose Input and Output Port 4.5/Programmable Logic Array Output Element 13.
55	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 μF capacitor when using the internal reference.
56	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
57	DACGND	Ground for the DAC. Typically connected to AGND.
58	AGND	Analog Ground. Ground reference point for the analog circuitry.
59	AV_{DD}	3.3 V Analog Power.
60	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
61	ADC0	Single-Ended or Differential Analog Input 0.
62	ADC1	Single-Ended or Differential Analog Input 1.
63	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
64	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
0	EP	Exposed Pad. The pin configuration for the ADuC7024/ADuC7025 LFCSP_VQ has an exposed pad that must be soldered for mechanical purposes and left unconnected.

ADUC7029

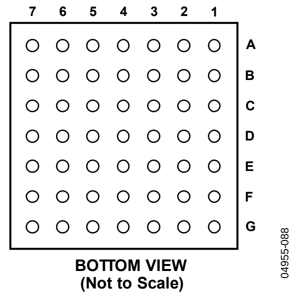

Figure 27. 49-Ball CSP_BGA Pin Configuration (ADuC7029)

Table 15. Pin Function Descriptions (ADuC7029)

Pin No.	Mnemonic	Description
A1	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
A2	ADC1	Single-Ended or Differential Analog Input 1.
A3	ADC0	Single-Ended or Differential Analog Input 0.
A4	AV_{DD}	3.3 V Analog Power.
A5	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 μF capacitor when using the internal reference.
A6	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
A7	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
B1	ADC6	Single-Ended or Differential Analog Input 6.
B2	ADC5	Single-Ended or Differential Analog Input 5.
B3	ADC4	Single-Ended or Differential Analog Input 4.
B4	AGND	Analog Ground. Ground reference point for the analog circuitry.
B5	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
B6	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
B7	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
C1	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
C2	AGND	Analog Ground. Ground reference point for the analog circuitry.
C3	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
C4	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
C5	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
C6	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
C7	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
D1	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
D2	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
D3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
D4	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
D5	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
D6	P3.6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
D7	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.

TYPICAL PERFORMANCE CHARACTERISTICS

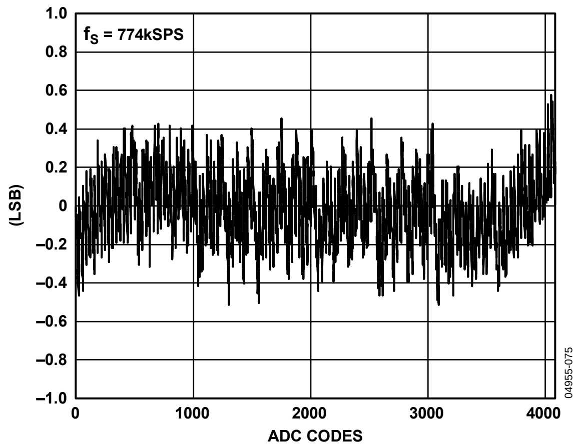

Figure 28. Typical INL Error, f_S = 774 kSPS

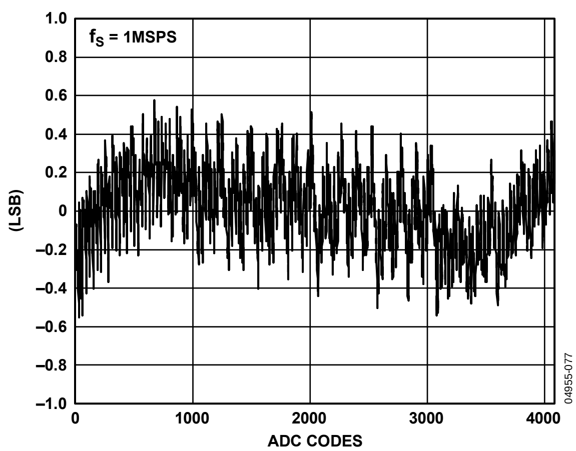

Figure 29. Typical INL Error, f_S = 1 MSPS

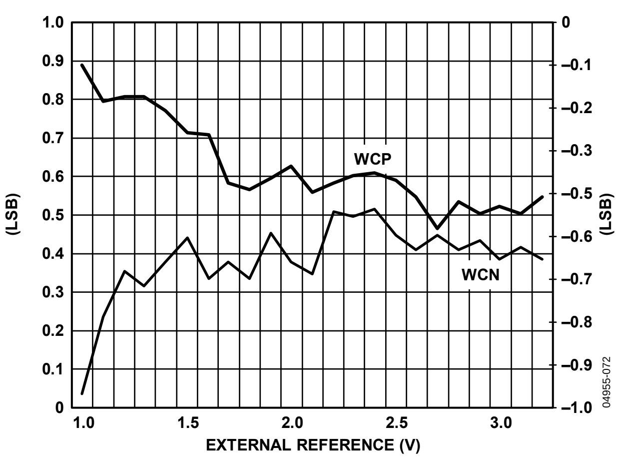

Figure 30. Typical Worst-Case (Positive (WCP) and Negative (WCN)) INL Error vs. V_{REF}, f_S = 774 kSPS

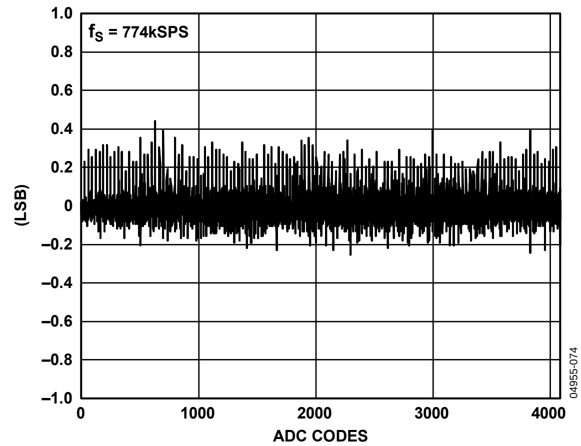

Figure 31. Typical DNL Error, f_S = 774 kSPS

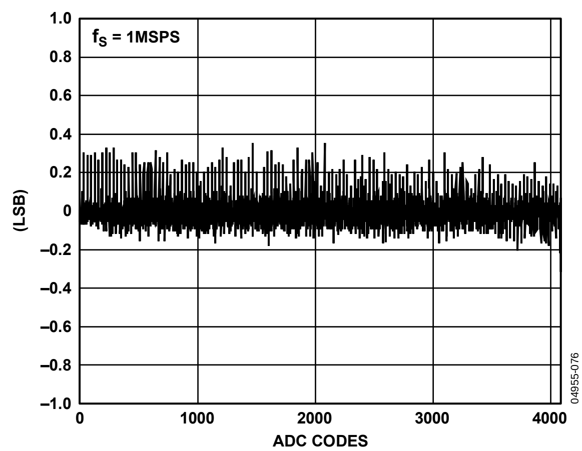

Figure 32. Typical DNL Error, f_S = 1 MSPS

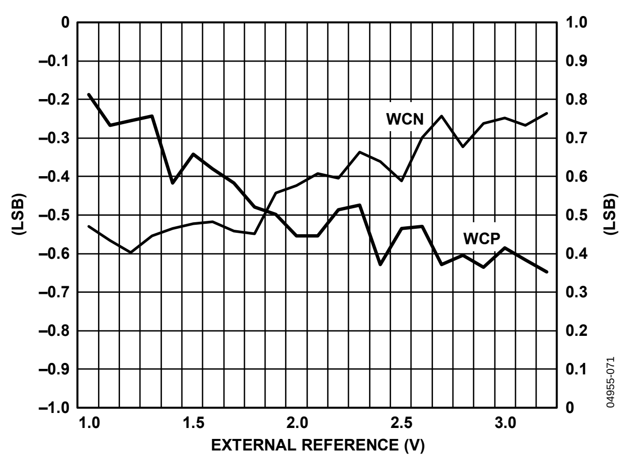

Figure 33. Typical Worst-Case (Positive (WCP)and Negative (WCN)) DNL Error vs. V_{REF}, f_S = 774 kSPS

TYPICAL OPERATION

Once configured via the ADC control and channel selection registers, the ADC converts the analog input and provides a 12-bit result in the ADC data register.

The top four bits are the sign bits. The 12-bit result is placed from Bit 16 to Bit 27, as shown in Figure 51. Again, it should be noted that, in fully differential mode, the result is represented in twos complement format. In pseudo differential and single-ended modes, the result is represented in straight binary format.

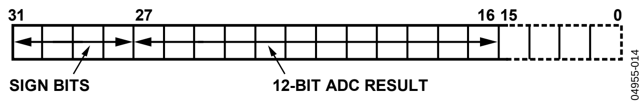

Figure 51. ADC Result Format

The same format is used in DACxDAT, simplifying the software.

Current Consumption

The ADC in standby mode, that is, powered up but not converting, typically consumes 640 µA. The internal reference adds 140 µA. During conversion, the extra current is 0.3 µA multiplied by the sampling frequency (in kilohertz (kHz)). Figure 43 shows the current consumption vs. the sampling frequency of the ADC.

Timing

Figure 52 gives details of the ADC timing. Users control the ADC clock speed and the number of acquisition clocks in the ADCCON MMR. By default, the acquisition time is eight clocks and the clock divider is 2. The number of extra clocks (such as bit trial or write) is set to 19, which gives a sampling rate of 774 kSPS. For conversion on the temperature sensor, the ADC acquisition time is automatically set to 16 clocks, and the ADC clock divider is set to 32. When using multiple channels, including the temperature sensor, the timing settings revert to the user-defined settings after reading the temperature sensor channel.

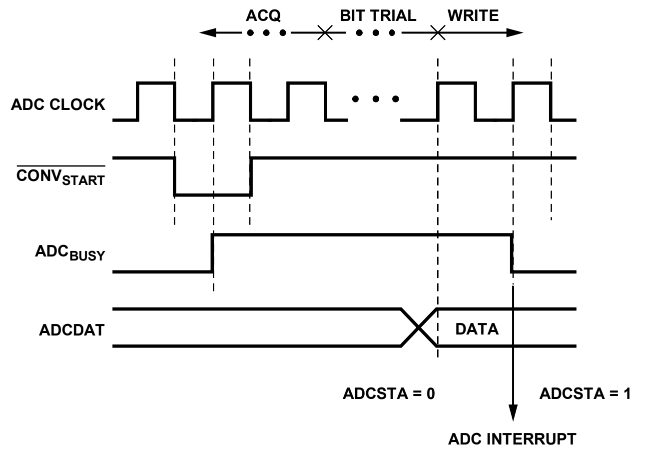

Figure 52. ADC Timing

ADuC7019

The ADuC7019 is identical to the ADuC7020 except for one buffered ADC channel, ADC3, and it has only three DACs. The output buffer of the fourth DAC is internally connected to the ADC3 channel as shown in Figure 53.

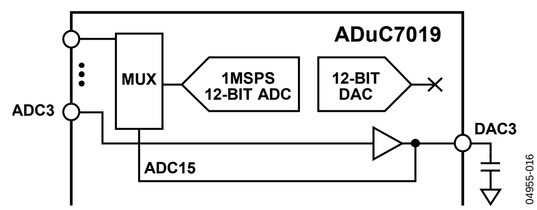

Figure 53. ADC3 Buffered Input

Note that the DAC3 output pin must be connected to a 10 nF capacitor to AGND. This channel should be used to measure dc voltages only. ADC calibration may be necessary on this channel.

MMRS INTERFACE

The ADC is controlled and configured via the eight MMRs described in this section.

Table 17. ADCCON Register

Name	Address	Default Value	Access
ADCCON	0xFFFF0500	0x0600	R/W

ADCCON is an ADC control register that allows the programmer to enable the ADC peripheral, select the mode of operation of the ADC (in single-ended mode, pseudo differential mode, or fully differential mode), and select the conversion type. This MMR is described in Table 18.

Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is one-half the width of the hysteresis range.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 56.

Table 55. CMPCON Register

Name	Address	Default Value	Access
CMPCON	0xFFFF0444	0x0000	R/W

Table 56. CMPCON MMR Bit Descriptions

Bit	Name	Value	Description
15:11			Reserved.
10	CMPEN		Comparator enable bit. Set by user to enable the comparator. Cleared by user to disable the comparator.
9:8	CMPIN		Comparator negative input select bits.
		00	$AV_{DD}/2$.
		01	ADC3 input.
		10	DAC0 output.
		11	Reserved.
7:6	CMPOC		Comparator output configuration bits.
		00	Reserved.
		01	Reserved.
		10	Output on CMP_{OUT}.
		11	IRQ.
5	CMPOL		Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
4:3	CMPRES		Response time.
		00	5 µs response time is typical for large signals (2.5 V differential). 17 µs response time is typical for small signals (0.65 mV differential).
		11	3 µs typical.
		01/10	Reserved.
2	CMPHYST		Comparator hysteresis bit. Set by user to have a hysteresis of about 7.5 mV. Cleared by user to have no hysteresis.
1	CMPORI		Comparator output rising edge interrupt. Set automatically when a rising edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.
0	CMPOFI		Comparator output falling edge interrupt. Set automatically when a falling edge occurs on the monitored voltage (CMP0). Cleared by user.

OSCILLATOR AND PLL—POWER CONTROL

Clocking System

Each ADuC7019/20/21/22/24/25/26/27/28/29 integrates a 32.768 kHz ±3% oscillator, a clock divider, and a PLL. The PLL locks onto a multiple (1275) of the internal oscillator or an external 32.768 kHz crystal to provide a stable 41.78 MHz clock (UCLK) for the system. To allow power saving, the core can operate at this frequency, or at binary submultiples of it. The actual core operating frequency, $UCLK/2^{CD}$, is refered to as HCLK. The default core clock is the PLL clock divided by 8 (CD = 3) or 5.22 MHz. The core clock frequency can also come from an external clock on the ECLK pin as described in Figure 67. The core clock can be outputted on ECLK when using an internal oscillator or external crystal.

Note that when the ECLK pin is used to output the core clock, the output signal is not buffered and is not suitable for use as a clock source to an external device without an external buffer.

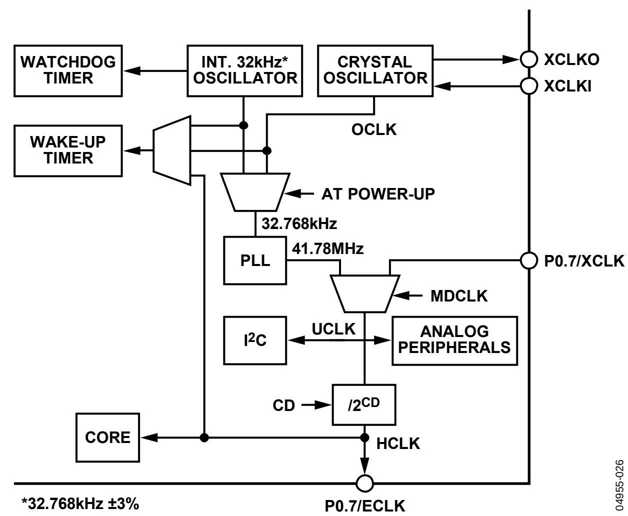

Figure 67. Clocking System

The selection of the clock source is in the PLLCON register. By default, the part uses the internal oscillator feeding the PLL.

External Crystal Selection

To switch to an external crystal, the user must do the following:

1. Enable the Timer2 interrupt and configure it for a timeout period of >120 µs.
2. Follow the write sequence to the PLLCON register, setting the MDCLK bits to 01 and clearing the OSEL bit.
3. Force the part into NAP mode by following the correct write sequence to the POWCON register.

   When the part is interrupted from NAP mode by the Timer2 interrupt source, the clock source has switched to the external clock.

Table 70. PWMCFG Register

Name	Address	Default Value	Access
PWMCFG	0xFFFFFC10	0x0000	R/W

PWMCFG is a gate chopping register.

Table 71. PWMCFG MMR Bit Descriptions

Bit	Name	Description
15:10		Reserved.
9	CHOPLO	Low-side gate chopping enable bit.
8	CHOPHI	High-side gate chopping enable bit.
7:0	GDCLK	PWM gate chopping period (unsigned).

Table 72. PWMEN Register

Name	Address	Default Value	Access
PWMEN	0xFFFFFC20	0x0000	R/W

PWMEN allows enabling of channel outputs and crossover. See its bit definitions in Table 73.

Table 73. PWMEN MMR Bit Descriptions

Bit	Name	Description
8	0H0L_XOVR	Channel 0 output crossover enable bit. Set to 1 by user to enable Channel 0 output crossover. Cleared to 0 by user to disable Channel 0 output crossover.
7	1H1L_XOVR	Channel 1 output crossover enable bit. Set to 1 by user to enable Channel 1 output crossover. Cleared to 0 by user to disable Channel 1 output crossover.
6	2H2L_XOVR	Channel 2 output crossover enable bit. Set to 1 by user to enable Channel 2 output crossover. Cleared to 0 by user to disable Channel 2 output crossover.
5	0L_EN	0L output enable bit. Set to 1 by user to disable the 0L output of the PWM. Cleared to 0 by user to enable the 0L output of the PWM.
4	0H_EN	0H output enable bit. Set to 1 by user to disable the 0H output of the PWM. Cleared to 0 by user to enable the 0H output of the PWM.
3	1L_EN	1L output enable bit. Set to 1 by user to disable the 1L output of the PWM. Cleared to 0 by user to enable the 1L output of the PWM.
2	1H_EN	1H Output Enable Bit. Set to 1 by user to disable the 1H output of the PWM. Cleared to 0 by user to enable the 1H output of the PWM.
1	2L_EN	2L output enable bit. Set to 1 by user to disable the 2L output of the PWM. Cleared to 0 by user to enable the 2L output of the PWM.
0	2H_EN	2H output enable bit. Set to 1 by user to disable the 2H output of the PWM. Cleared to 0 by user to enable the 2H output of the PWM.

Table 74. PWMDAT0 Register

Name	Address	Default Value	Access
PWMDAT0	0xFFFFFC08	0x0000	R/W

PWMDAT0 is an unsigned 16-bit register for switching period.

Table 75. PWMDAT1 Register

Name	Address	Default Value	Access
PWMDAT1	0xFFFFFC0C	0x0000	R/W

PWMDAT1 is an unsigned 10-bit register for dead time.

Table 76. PWMCHx Registers

Name	Address	Default Value	Access
PWMCH0	0xFFFFFC14	0x0000	R/W
PWMCH1	0xFFFFFC18	0x0000	R/W
PWMCH2	0xFFFFFC1C	0x0000	R/W

PWMCH0, PWMCH1, and PWMCH2 are channel duty cycles for the three phases.

Table 77. PWMDAT2 Register

Name	Address	Default Value	Access
PWMDAT2	0xFFFFFC24	0x0000	R/W

PWMDAT2 is an unsigned 10-bit register for PWM sync pulse width.

GENERAL-PURPOSE INPUT/OUTPUT

The ADuC7019/20/21/22/24/25/26/27/28/29 provide 40 general-purpose, bidirectional I/O (GPIO) pins. All I/O pins are 5 V tolerant, meaning the GPIOs support an input voltage of 5 V.

In general, many of the GPIO pins have multiple functions (see Table 78 for the pin function definitions). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ), and their drive capability is 1.6 mA. Note that a maximum of 20 GPIOs can drive 1.6 mA at the same time. Using the GPxPAR registers, it is possible to enable/disable the pull-up resistors for the following ports: P0.0, P0.4, P0.5, P0.6, P0.7, and the eight GPIOs of P1.

The 40 GPIOs are grouped in five ports, Port 0 to Port 4 (Port x). Each port is controlled by four or five MMRs.

Note that the kernel changes P0.6 from its default configuration at reset (MRST) to GPIO mode. If MRST is used for external circuitry, an external pull-up resistor should be used to ensure that the level on P0.6 does not drop when the kernel switches mode. Otherwise, P0.6 goes low for the reset period. For example, if MRST is required for power-down, it can be reconfigured in GP0CON MMR.

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the ADuC7019/20/21/22/24/25/26/27/28/29 part enters a power-saving mode, the GPIO pins retain their state.

Table 99. COMDIV1 Register

Name	Address	Default Value	Access
COMDIV1	0xFFFF0704	0x00	R/W

COMDIV1 is a divisor latch (high byte) register.

Table 100. COMIID0 Register

Name	Address	Default Value	Access
COMIID0	0xFFFF0708	0x01	R

COMIID0 is the interrupt identification register.

Table 101. COMIID0 MMR Bit Descriptions

Bit 2:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
00	1	N/A	No interrupt	N/A
11	0	1 (Highest)	Receive line status interrupt	Read COMSTA0
10	0	2	Receive buffer full interrupt	Read COMRX
01	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
00	0	4 (Lowest)	Modem status interrupt	Read COMSTA1

Table 102. COMCON0 Register

Name	Address	Default Value	Access
COMCON0	0xFFFF070C	0x00	R/W

COMCON0 is the line control register.

Table 103. COMCON0 MMR Bit Descriptions

Bit	Name	Description
7	DLAB	Divisor latch access. Set by user to enable access to the COMDIV0 and COMDIV1 registers. Cleared by user to disable access to COMDIV0 and COMDIV1 and enable access to COMRX and COMTX.
6	BRK	Set break. Set by user to force SOUT to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by user to force parity to defined values: 1 if EPS = 1 and PEN = 1, 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1:0	WLS	Word length select: 00 = five bits, 01 = six bits, 10 = seven bits, 11 = eight bits.

Table 104. COMCON1 Register

Name	Address	Default Value	Access
COMCON1	0xFFFF0710	0x00	R/W

COMCON1 is the modem control register.

Table 105. COMCON1 MMR Bit Descriptions

Bit	Name	Description
7:5		Reserved.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, SOUT (see Table 78) is forced high. The modem signals are also directly connected to the status inputs (RTS to CTS and DTR to DSR). Cleared by user to be in normal mode.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits, or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

Table 106. COMSTA0 Register

Name	Address	Default Value	Access
COMSTA0	0xFFFF0714	0x60	R

COMSTA0 is the line status register.

Table 107. COMSTA0 MMR Bit Descriptions

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and shift register are empty. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty. Set automatically if COMTX is empty. Cleared automatically when writing to COMTX.
4	BI	Break error. Set when SIN is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when an invalid stop bit occurs. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data is over-written before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

SPI Registers

The following MMR registers are used to control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

Table 119. SPISTA Register

Name	Address	Default Value	Access
SPISTA	0xFFFF0A00	0x00	R

SPISTA is an 8-bit read-only status register. Only Bit 1 or Bit 4 of this register generates an interrupt. Bit 6 of the SPICON register determines which bit generates the interrupt.

Table 120. SPISTA MMR Bit Descriptions

Bit	Description
7:6	Reserved.
5	SPIRX data register overflow status bit. Set if SPIRX is overflowing. Cleared by reading the SPIRX register.
4	SPIRX data register IRQ. Set automatically if Bit 3 or Bit 5 is set. Cleared by reading the SPIRX register.
3	SPIRX data register full status bit. Set automatically if a valid data is present in the SPIRX register. Cleared by reading the SPIRX register.
2	SPITX data register underflow status bit. Set automatically if SPITX is underflowing. Cleared by writing in the SPITX register.
1	SPITX data register IRQ. Set automatically if Bit 0 is clear or Bit 2 is set. Cleared by writing in the SPITX register or if finished transmission disabling the SPI.
0	SPITX data register empty status bit. Set by writing to SPITX to send data. This bit is set during transmission of data. Cleared when SPITX is empty.

Table 121. SPIRX Register

Name	Address	Default Value	Access
SPIRX	0xFFFF0A04	0x00	R

SPIRX is an 8-bit, read-only receive register.

Table 122. SPITX Register

Name	Address	Default Value	Access
SPITX	0xFFFF0A08	0x00	W

SPITX is an 8-bit, write-only transmit register.

Table 123. SPIDIV Register

Name	Address	Default Value	Access
SPIDIV	0xFFFF0A0C	0x1B	R/W

SPIDIV is an 8-bit, serial clock divider register.

Table 124. SPICON Register

Name	Address	Default Value	Access
SPICON	0xFFFF0A10	0x0000	R/W

SPICON is a 16-bit control register.

Table 125. SPICON MMR Bit Descriptions

Bit	Description	Function
15:13	Reserved	N/A
12	Continuous transfer enable	Set by user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the TX register. $\overline{\text{CS}}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until TX is empty. Cleared by user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period.
11	Loop back enable	Set by user to connect MISO to MOSI and test software. Cleared by user to be in normal mode.
10	Slave MISO output enable	Set this bit to disable the output driver on the MISO pin. The MISO pin becomes open drain when this bit is set. Clear this bit for MISO to operate as normal.
9	Clip select output enable	Set by user in master mode to disable the chip select output. cleared by user to enable the chip select output. P1.7 should be configured as $\overline{\text{CS}}$ before SPICON is configured as a master when the chip select output enabled is also selected.
8	SPIRX overflow overwrite enable	Set by user, the valid data in the RX register is overwritten by the new serial byte received. Cleared by user, the new serial byte received is discarded.
7	SPITX underflow mode	Set by user to transmit 0. Cleared by user to transmit the previous data.
6	Transfer and interrupt mode	Set by user to initiate transfer with a write to the SPITX register. Interrupt occurs only when TX is empty. Cleared by user to initiate transfer with a read of the SPIRX register. Interrupt occurs only when RX is full.
5	LSB first transfer enable bit	Set by user, the LSB is transmitted first. Cleared by user, the MSB is transmitted first.
4	Reserved	
3	Serial clock polarity mode bit	Set by user, the serial clock idles high. Cleared by user, the serial clock idles low.
2	Serial clock phase mode bit	Set by user, the serial clock pulses at the beginning of each serial bit transfer. Cleared by user, the serial clock pulses at the end of each serial bit transfer.
1	Master mode enable bit	Set by user to enable master mode. Cleared by user to enable slave mode.
0	SPI enable bit	Set by user to enable the SPI. Cleared by user to disable the SPI.

Table 129. I2C0SSTA MMR Bit Descriptions

Bit	Value	Description
31:15		Reserved. These bits should be written as 0.
14		Start decode bit. Set by hardware if the device receives a valid start plus matching address. Cleared by an I^{2}C stop condition or an I^{2}C general call reset.
13		Repeated start decode bit. Set by hardware if the device receives a valid repeated start and matching address. Cleared by an I^{2}C stop condition, a read of the I2CSSTA register, or an I^{2}C general call reset.
12:11		ID decode bits.
	00	Received Address Matched ID Register 0.
	01	Received Address Matched ID Register 1.
	10	Received Address Matched ID Register 2.
	11	Received Address Matched ID Register 3.
10		Stop after start and matching address interrupt. Set by hardware if the slave device receives an I^{2}C stop condition after a previous I^{2}C start condition and matching address. Cleared by a read of the I2C0SSTA register.
9:8		General call ID.
	00	No general call.
	01	General call reset and program address.
	10	General call program address.
	11	General call matching alternative ID.
7		General call interrupt. Set if the slave device receives a general call of any type. Cleared by setting Bit 8 of the I2CxCFG register. If it is a general call reset, all registers are at their default values. If it is a hardware general call, the Rx FIFO holds the second byte of the general call. This is similar to the I2C0ALT register (unless it is a general call to reprogram the device address). For more details, see the I^{2}C bus specification, Version 2.1, January 2000.
6		Slave busy. Set automatically if the slave is busy. Cleared automatically.
5		No ACK. Set if master asking for data and no data is available. Cleared automatically by reading the I2C0SSTA register.
4		Slave receive FIFO overflow. Set automatically if the slave receive FIFO is overflowing. Cleared automatically by reading the I2C0SSTA register.
3		Slave receive IRQ. Set after receiving data. Cleared automatically by reading the I2C0SRX register or flushing the FIFO.
2		Slave transmit IRQ. Set at the end of a transmission. Cleared automatically by writing to the I2C0STX register.
1		Slave transmit FIFO underflow. Set automatically if the slave transmit FIFO is underflowing. Cleared automatically by writing to the I2C0SSTA register.
0		Slave transmit FIFO not full. Set automatically if the slave transmit FIFO is not full. Cleared automatically by writing twice to the I2C0STX register.

Table 130. I2CxSRX Registers

Name	Address	Default Value	Access
I2C0SRX	0xFFFF0808	0x00	R
I2C1SRX	0xFFFF0908	0x00	R

I2CxSRX are receive registers for the slave channel.

Table 131. I2CxSTX Registers

Name	Address	Default Value	Access
I2C0STX	0xFFFF080C	0x00	W
I2C1STX	0xFFFF090C	0x00	W

I2CxSTX are transmit registers for the slave channel.

Table 132. I2CxMRX Registers

Name	Address	Default Value	Access
I2C0MRX	0xFFFF0810	0x00	R
I2C1MRX	0xFFFF0910	0x00	R

I2CxMRX are receive registers for the master channel.

Table 133. I2CxMTX Registers

Name	Address	Default Value	Access
I2C0MTX	0xFFFF0814	0x00	W
I2C1MTX	0xFFFF0914	0x00	W

I2CxMTX are transmit registers for the master channel.

Table 134. I2CxCNT Registers

Name	Address	Default Value	Access
I2C0CNT	0xFFFF0818	0x00	R/W
I2C1CNT	0xFFFF0918	0x00	R/W

I2CxCNT are 3-bit, master receive, data count registers. If a master read transfer sequence is initiated, the I2CxCNT registers denote the number of bytes (−1) to be read from the slave device. By default, this counter is 0, which corresponds to the one byte expected.

Table 135. I2CxADR Registers

Name	Address	Default Value	Access
I2C0ADR	0xFFFF081C	0x00	R/W
I2C1ADR	0xFFFF091C	0x00	R/W

I2CxADR are master address byte registers. The I2CxADR value is the device address that the master wants to communicate with. It automatically transmits at the start of a master transfer sequence if there is no valid data in the I2CxMTX register when the master enable bit is set.

Table 136. I2CxBYTE Registers

Name	Address	Default Value	Access
I2C0BYTE	0xFFFF0824	0x00	R/W
I2C1BYTE	0xFFFF0924	0x00	R/W

I2CxBYTE are broadcast byte registers. Data written to these registers does not go through the TxFIFO. This data is transmitted at the start of a transfer sequence before the address. After the byte is transmitted and acknowledged, the I^{2}C expects another byte written in I2CxBYTE or an address written to the address register.

FIQ

The fast interrupt request (FIQ) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface providing the second-level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

Table 165. FIQSTA Register

Name	Address	Default Value	Access
FIQSTA	0xFFFF0100	0x00000000	R

Table 166. FIQSIG Register

Name	Address	Default Value	Access
FIQSIG	0xFFFF0104	0x00XXX000[1]	R

[1] X indicates an undefined value.

Table 167. FIQEN Register

Name	Address	Default Value	Access
FIQEN	0xFFFF0108	0x00000000	R/W

Table 168. FIQCLR Register

Name	Address	Default Value	Access
FIQCLR	0xFFFF010C	0x00000000	W

Bit 31 to Bit 1 of FIQSTA are logically OR'd to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and IRQEN does not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to 1 in FIQEN does, as a side effect, clear the same bit in IRQEN. Also, a bit set to 1 in IRQEN does, as a side effect, clear the same bit in FIQEN. An interrupt source can be disabled in both the IRQEN and FIQEN masks.

Note that to clear an already enabled FIQ source, the user must set the appropriate bit in the FIQCLR register. Clearing an interrupt's FIQEN bit does not disable the interrupt.

Programmed Interrupts

Because the programmed interrupts are nonmaskable, they are controlled by another register, SWICFG, which simultaneously writes into the IRQSTA and IRQSIG registers and/or the FIQSTA and FIQSIG registers. The 32-bit SWICFG register is dedicated to software interrupts(see Table 170). This MMR allows the control of a programmed source interrupt.

Table 169. SWICFG Register

Name	Address	Default Value	Access
SWICFG	0xFFFF0010	0x00000000	W

Table 170. SWICFG MMR Bit Descriptions

Bit	Description
31:3	Reserved.
2	Programmed interrupt (FIQ). Setting/clearing this bit corresponds with setting/clearing Bit 1 of FIQSTA and FIQSIG.
1	Programmed interrupt (IRQ). Setting/clearing this bit corresponds with setting/clearing Bit 1 of IRQSTA and IRQSIG.
0	Reserved.

Note that any interrupt signal must be active for at least the equivalent of the interrupt latency time, which is detected by the interrupt controller and by the user in the IRQSTA/FIQSTA register.

TIMERS

The ADuC7019/20/21/22/24/25/26/27/28/29 have four general-purpose timer/counters.

- Timer0
- Timer1
- Timer2 or wake-up timer
- Timer3 or watchdog timer

These four timers in their normal mode of operation can be either free running or periodic.

In free-running mode, the counter decreases from the maximum value until zero scale and starts again at the minimum value. (It also increases from the minimum value until full scale and starts again at the maximum value.)

In periodic mode, the counter decrements/increments from the value in the load register (TxLD MMR) until zero/full scale and starts again at the value stored in the load register.

The timer interval is calculated as follows:

If the timer is set to count down then

$$Interval = \frac{(TxLD) \times Prescaler}{Source Clock}$$

If the timer is set to count up, then

$$Interval = \frac{(Fs - TxLD) \times Prescaler}{Source Clock}$$

The value of a counter can be read at any time by accessing its value register (TxVAL). Note that when a timer is being clocked from a clock other than core clock, an incorrect value may be read (due to an asynchronous clock system). In this configur-ation, TxVAL should always be read twice. If the two readings are different, it should be read a third time to get the correct value.

Timers are started by writing in the control register of the corresponding timer (TxCON).

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the core clock frequency, or an external GPIO (P1.0 or P0.6). The maximum frequency of the clock input is 44 Mhz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 78.

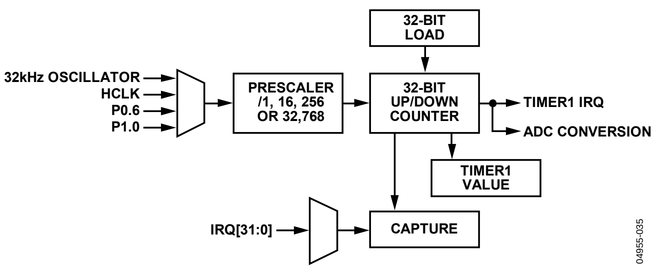

Figure 78. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

Table 177. T1LD Register

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000000	R/W

T1LD is a 32-bit load register.

Table 178. T1VAL Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0xFFFFFFFF	R

T1VAL is a 32-bit read-only register that represents the current state of the counter.

Table 179. T1CON Register

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

T1CON is the configuration MMR described in Table 180.

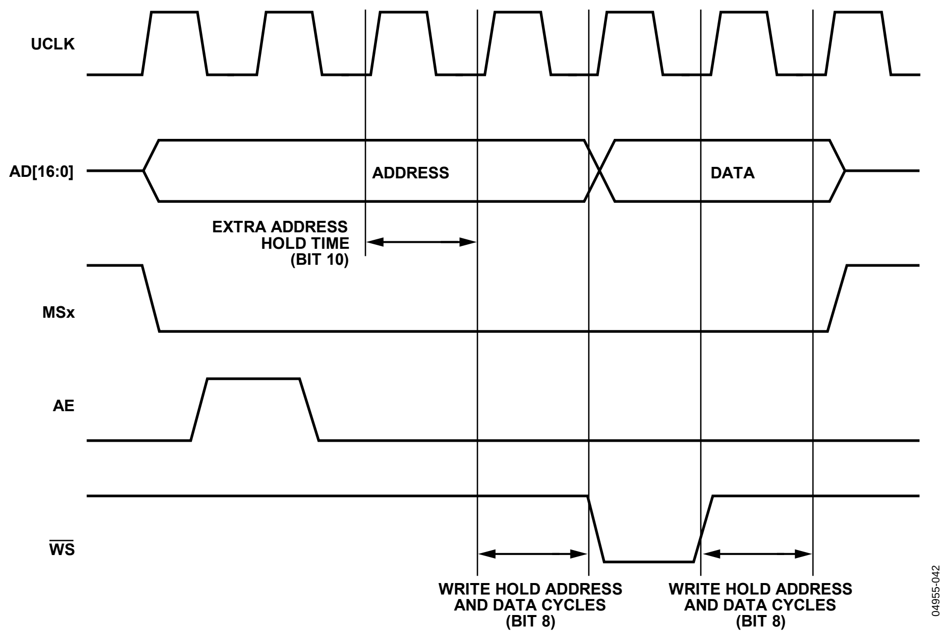

Figure 85. External Memory Write Cycle with Address and Write Hold Cycles

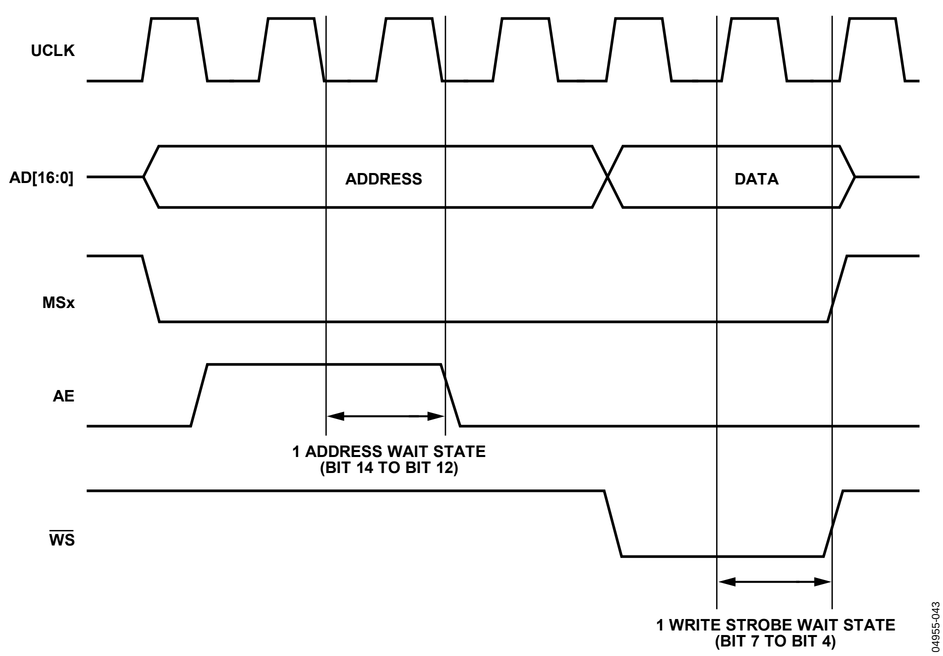

Figure 86. External Memory Write Cycle with Wait States

ORDERING GUIDE

Model[1, 2]	ADC Channels[3]	DAC Channels	FLASH/ RAM	GPIO	Down-loader	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7019BCPZ62I	5	3	62 kB/8 kB	14	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7019BCPZ62I-RL	5	3	62 kB/8 kB	14	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7019BCPZ62IRL7	5	3	62 kB/8 kB	14	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62	5	4	62 kB/8 kB	14	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62-RL7	5	4	62 kB/8 kB	14	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62I	5	4	62 kB/8 kB	14	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62I-RL	5	4	62 kB/8 kB	14	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7020BCPZ62IRL7	5	4	62 kB/8 kB	14	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62-RL	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ62-RL7	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62I	8	2	62 kB/8 kB	13	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62I-RL	8	2	62 kB/8 kB	13	I^2C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ32	8	2	32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ32-RL7	8	2	32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ62	10		62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ62-RL7	10		62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ32	10		32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ32-RL	10		32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7024BCPZ62	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62-RL7	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	750
ADuC7024BCPZ62I	10	2	62 kB/8 kB	30	I^2C	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62I-RL	10	2	62 kB/8 kB	30	I^2C	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7024BSTZ62	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7024BSTZ62-RL	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7025BCPZ62	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ62-RL	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BCPZ32	12		32 kB/4 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ32-RL	12		32 kB/4 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BSTZ62	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7025BSTZ62-RL	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7026BSTZ62	12	4	62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62-RL	12	4	62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7026BSTZ62I	12	4	62 kB/8 kB	40	I^2C	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62I-RL	12	4	62 kB/8 kB	40	I^2C	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62	16		62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62-RL	16		62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62I	16		62 kB/8 kB	40	I^2C	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62I-RL	16		62 kB/8 kB	40	I^2C	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7028BBCZ62	8	4	62 kB/8 kB	30	UART	−40°C to +125°C	64-Ball CSP_BGA	BC-64-4	
ADuC7028BBCZ62-RL	8	4	62 kB/8 kB	30	UART	−40°C to +125°C	64-Ball CSP_BGA	BC-64-4	2,500
ADuC7029BBCZ62	7	4	62 kB/8 kB	22	UART	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62-RL	7	4	62 kB/8 kB	22	UART	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000
ADuC7029BBCZ62I	7	4	62 kB/8 kB	22	I^2C	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62I-RL	7	4	62 kB/8 kB	22	I^2C	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000