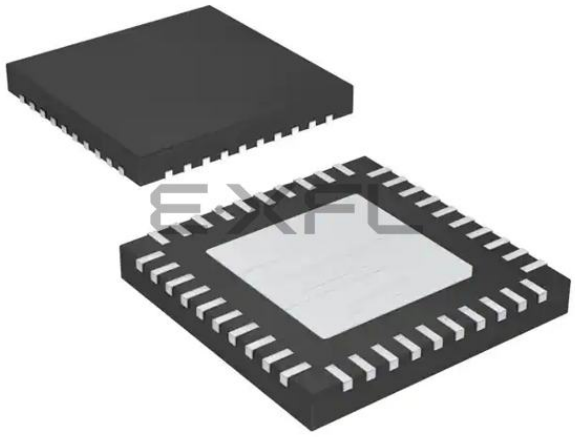
Renesas Electronics America Inc - R5F213M6UNNP#U0 Datasheet



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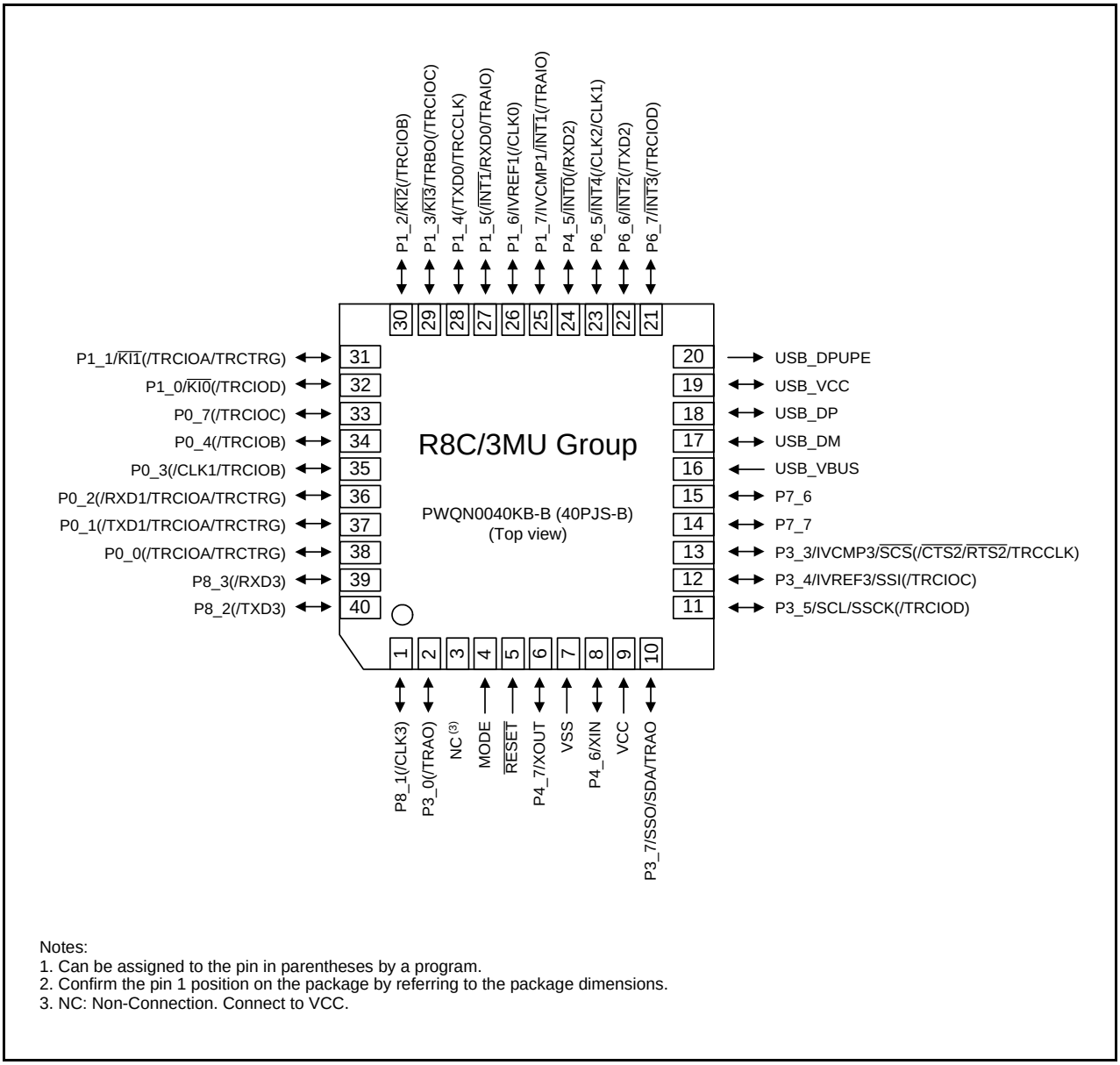
Details	
Product Status	Last Time Buy
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART, USB
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213m6unnp-u0

1.4 Pin Assignment

Figures 1.5 and 1.6 show Pin Assignment (Top View) of Each Group. Table 1.6 outlines the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.
3. NC: Non-Connection. Connect to VCC.

Figure 1.5 Pin Assignment (Top View) of R8C/3MU Group

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules						
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	USB	A/D Converter, Comparator B
1		P8_1			(CLK3)				
2		P3_0		(TRAO)					
3									VREF (2)
4	MODE								
5	$\overline{\text{RESET}}$								
6	XOUT	P4_7							
7	VSS/ AVSS (2)								
8	XIN	P4_6							
9	VCC/ AVCC (2)								
10		P3_7		TRAO		SSO	SDA		
11		P3_5		(TRCIOD)		SSCK	SCL		
12		P3_4		(TRCIOC)		SSI			IVREF3
13		P3_3		(TRCCLK)	($\overline{\text{CTS2}}$/ $\overline{\text{RTS2}}$)	$\overline{\text{SCS}}$			IVCMP3
14		P7_7						USB_VBUSEN (2)	
15		P7_6						USB_OVRCURA (2)	
16								USB_VBUS	
17								USB_DM	
18								USB_DP	
19								USB_VCC	
20								USB_DPUPE	
21		P6_7	$\overline{\text{INT3}}$	(TRCIOD)					
22		P6_6	$\overline{\text{INT2}}$		(TXD2)				
23		P6_5	$\overline{\text{INT4}}$		(CLK2/ CLK1)				
24		P4_5	$\overline{\text{INT0}}$		(RXD2)				$\overline{\text{ADTRG}}$ (2)
25		P1_7	$\overline{\text{INT1}}$	(TRAIO)					IVCMP1
26		P1_6			(CLK0)				IVREF1
27		P1_5	($\overline{\text{INT1}}$)	(TRAIO)	(RXD0)				
28		P1_4		(TRCCLK)	(TXD0)				
29		P1_3	$\overline{\text{KI3}}$	TRBO (/TRCIOC)					AN11 (2)
30		P1_2	$\overline{\text{KI2}}$	(TRCIOB)					AN10 (2)
31		P1_1	$\overline{\text{KI1}}$	(TRCIOA/ TRCTRG)					AN9 (2)
32		P1_0	$\overline{\text{KI0}}$	(TRCIOD)					AN8 (2)
33		P0_7		(TRCIOC)					AN0 (2)
34		P0_4		(TRCIOB)					AN3 (2)
35		P0_3		(TRCIOB)	(CLK1)				AN4 (2)
36		P0_2		(TRCIOA/ TRCTRG)	(RXD1)				AN5 (2)
37		P0_1		(TRCIOA/ TRCTRG)	(TXD1)				AN6 (2)
38		P0_0		(TRCIOA/ TRCTRG)					AN7 (2)
39		P8_3			(RXD3)				
40		P8_2			(TXD3)				

Notes:
1. Can be assigned to the pin in parentheses by a program.
2. This pin is not available in the R8C/3MU Group.

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS (2)	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. (1) To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Serial interface	CLK0, CLK1, CLK2, CLK3	I/O	Transfer clock I/O pins.
	RXD0, RXD1, RXD2, RXD3	I	Serial data input pins.
	TXD0, TXD1, TXD2, TXD3	O	Serial data output pins.
	$\overline{\text{CTS2}}$	I	Transmission control input pin.
	$\overline{\text{RTS2}}$	O	Reception control output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I^2C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.

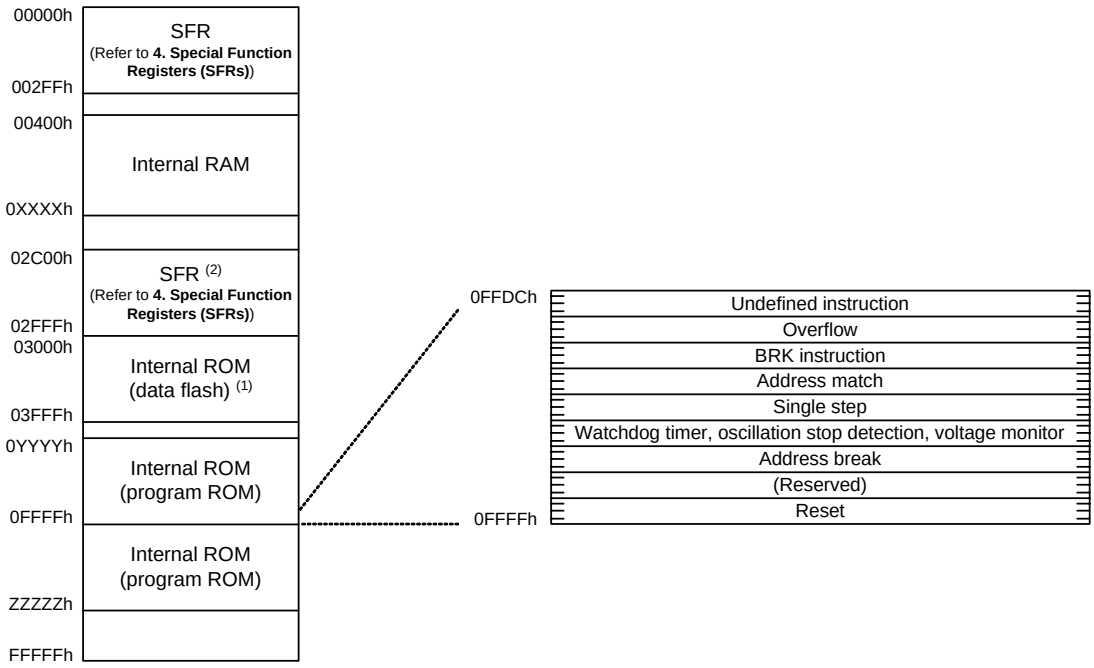
I: Input O: Output I/O: Input and output

Notes:

1. Refer to the oscillator manufacturer for oscillation characteristics.
2. This pin is not available in the R8C/3MU Group.

3.2 R8C/3MK Group

Figure 3.2 is a Memory Map of R8C/3MK Group. The R8C/3MK Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. A 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 8-Kbyte internal RAM area is allocated addresses 00400h to 023FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F213M8KNNP R5F213M8KNXXXNP	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh
R5F213MCKNNP R5F213MCKNXXXNP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.2 Memory Map of R8C/3MK Group

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

5.1 R8C/3MU Group

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	$-20°C \leq T_{opr} \leq 85°C$	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 5.9 Voltage Detection 2 Circuit Electrical Characteristics

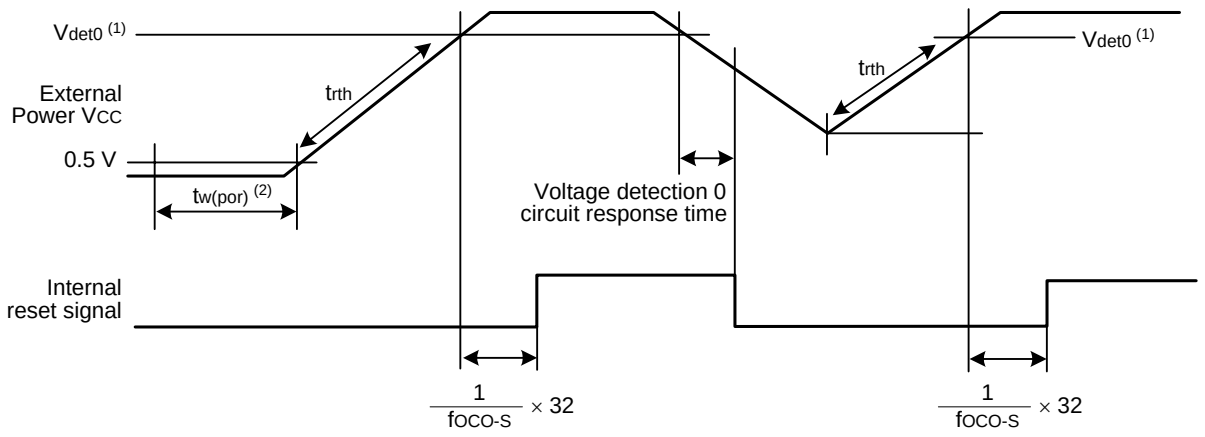
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	At the falling of V_{CC}	3.70	4.00	4.30	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of V_{CC} from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.10 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.5 Power-on Reset Circuit Electrical Characteristics

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V	36.0	40	44.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	V_{CC} = 1.8 V to 5.5 V	33.178	36.864	40.550	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V	28.8	32	35.2	MHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	0.5	3	ms
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	400	—	µA

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	30	100	µs
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	2	—	µA

Note:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.14 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_{H}	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

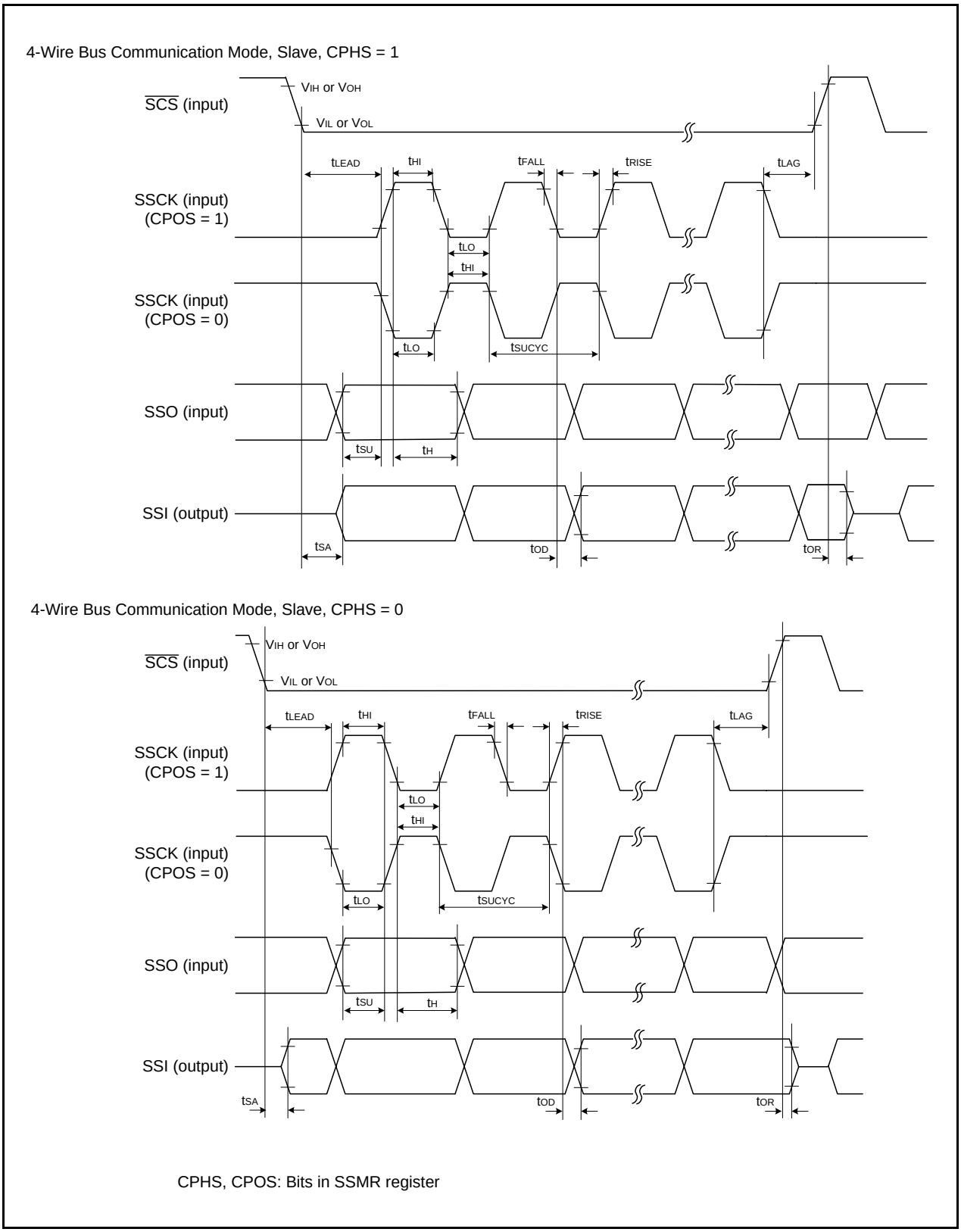


Figure 5.7 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{W(CKH)}$	CLKi input “H” width	150	—	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

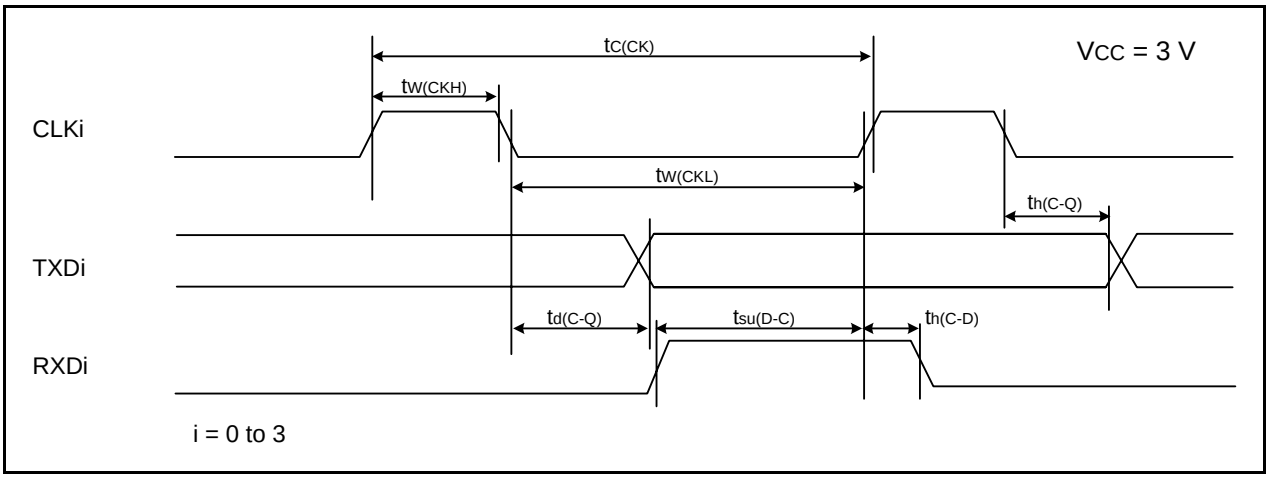


Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

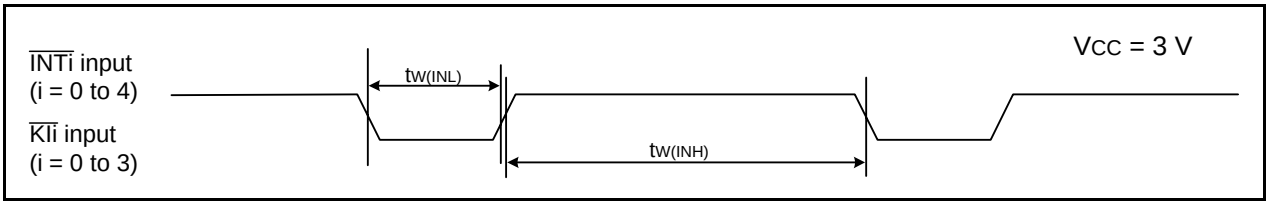


Figure 5.17 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

Table 5.29 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	2.2	—	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	0.8	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.7	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC=MSTTRC=1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing requirements (Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 5.30 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	—	ns

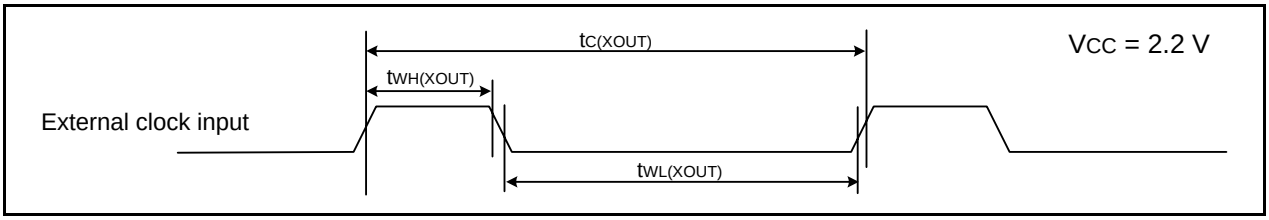


Figure 5.18 External Clock Input Timing Diagram when V_{CC} = 2.2 V

Table 5.31 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

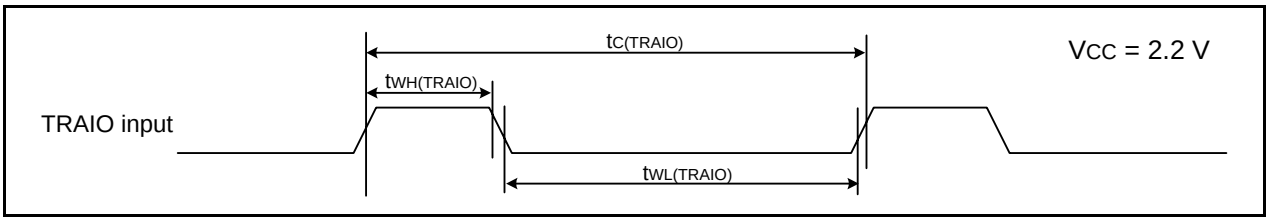


Figure 5.19 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

5.2 R8C/3MK Group

Table 5.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	–20°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 5.41 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (4)	At the falling of V_{CC} from 5.0 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.42 Voltage Detection 1 Circuit Electrical Characteristics

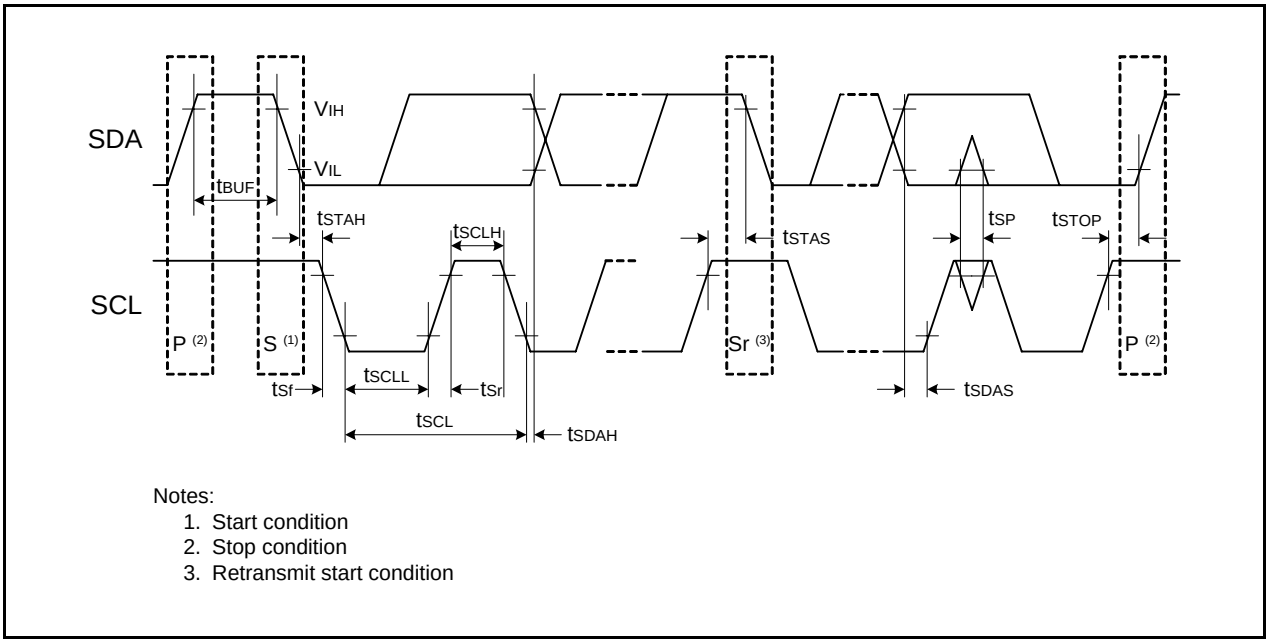
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (2)	At the falling of V_{CC}	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of V_{CC}	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of V_{CC}	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of V_{CC}	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of V_{CC}	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of V_{CC}	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of V_{CC}	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of V_{CC}	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of V_{CC}	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of V_{CC}	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of V_{CC}	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of V_{CC}	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of V_{CC}	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of V_{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 5.0 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.49 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.30 I/O Timing of I²C bus Interface

Table 5.54 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{W(CKH)}$	CLKi input “H” width	100	—	ns
$t_{W(CKL)}$	CLKi input “L” width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

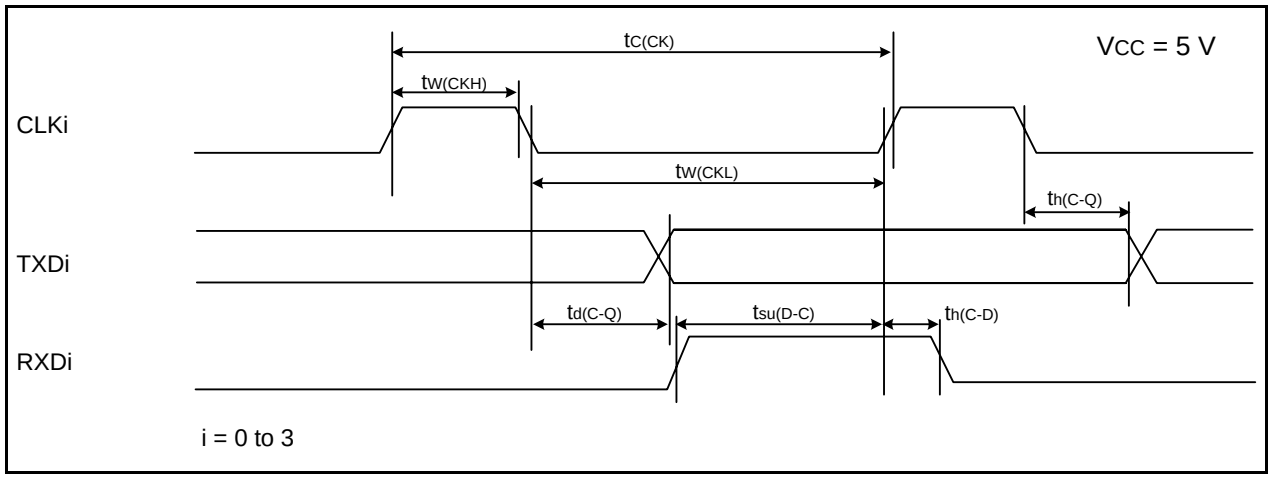


Figure 5.33 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.55 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

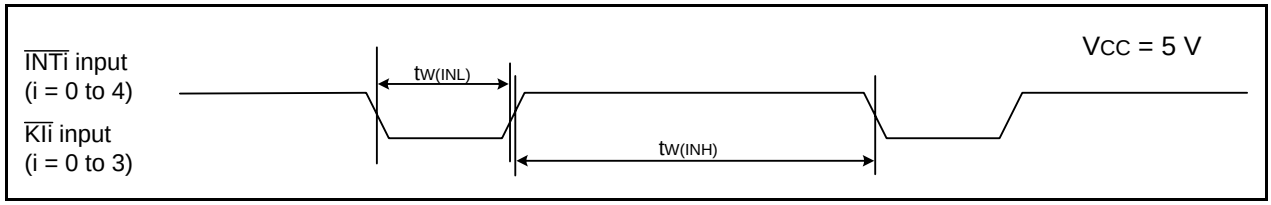


Figure 5.34 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V

Table 5.57 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V] (Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	4.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Table 5.66 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{W(CKH)}$	CLKi input “H” width	400	—	ns
$t_{W(CKL)}$	CLKi input “L” width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

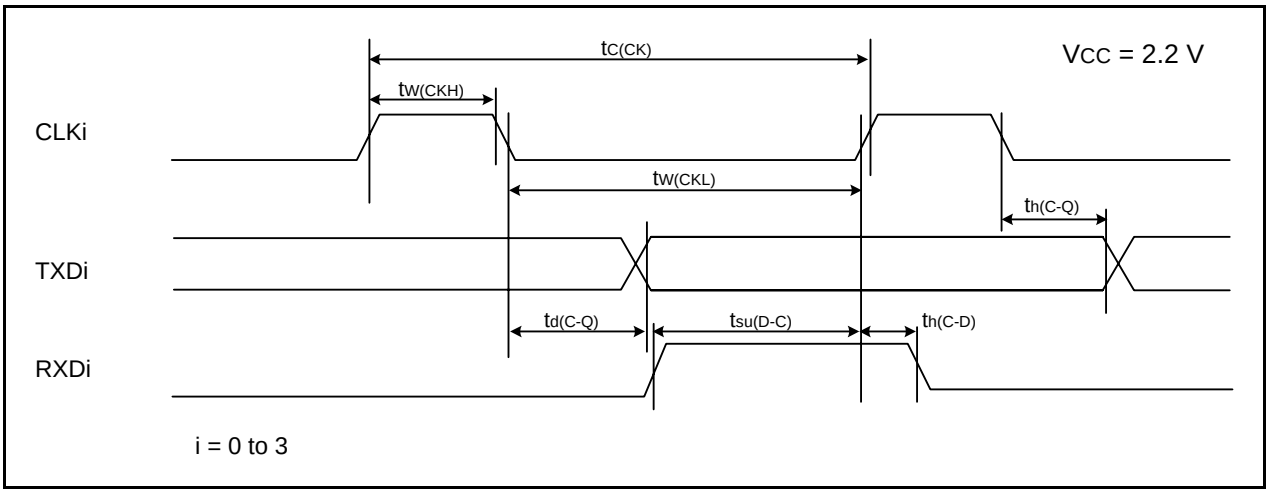


Figure 5.41 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.67 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

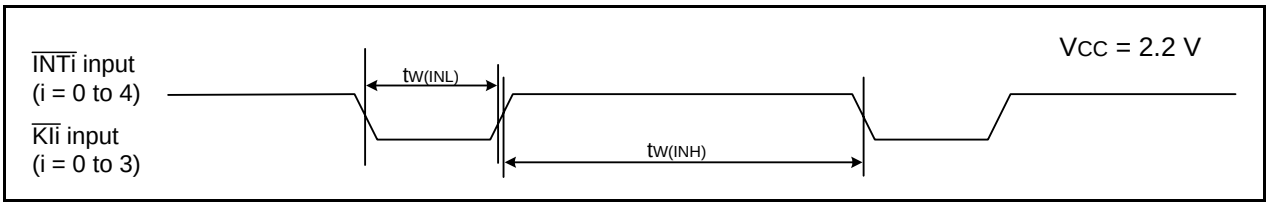


Figure 5.42 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 2.2 V

REVISION HISTORY	R8C/3MU Group, R8C/3MK Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.02	Nov 08, 2010	3	Table 1.2 A/D converter, Package revised
		4	Table 1.3 "(D)"added Table 1.3, Figure 1.1 Package revised
		5	Figure 1.2 I/O Ports, A/D converter revised LIN Module added
		6	Figure 1.3 revised
		7	Table 1.4 Pin Number 2, 7, 9, 22 revised
		9	Table 1.6 USB "USB_OVRCURA" added
		14	Table 4.1 0026h "On-Chip Reference Voltage Control Register OCVREFCR 00h" added
		15	Table 4.2 004Ah deleted
		16	Table 4.3 00BBh "UART2 Special Mode Register 5 U2SMR5 XXh" added 00BDh "UART2 Special Mode Register 3 U2SMR3 000X0X0Xb2" added
		18	Table 4.5 0105h "LIN Control Register 2 LINCR2 00h" added 0106h "LIN Control Register LINCR 00h" added 0107h "LIN Status Register LINST 00h" added
		25	Table 4.12 2E02h, 2E03h deleted
		29	Package Dimensions added
1.00	Feb 25, 2011	All pages	"Preliminary", "Under development" deleted
		3	Table 1.2 revised
		4	Table 1.3, Figure 1.1 revised
		5	Figure 1.2 revised
		6	Figure 1.3 revised
		7	Table 1.4 revised
		9	Table 1.6 revised
		13	3.1 revised, Figure 3.1 "Part Number" added
		14	Table 4.1 0026h revised
		15	Table 4.2 0041h revised
		16	Table 4.3 00BBh revised
		20	Table 4.7 0181h revised
		25	Table 4.12 2E04h and 2E05h revised
		26	Table 4.13 2E40h to 2E43h revised
		27	Table 4.14 2ED2h to 2ED7h deleted
		28	Table 4.15 2F04h, 2F11h and 2F13h deleted, 2F10h added
		29 to 56	5. Electrical Characteristics added