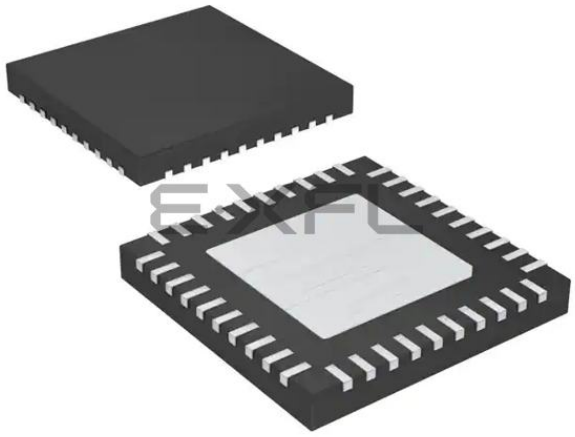
Renesas Electronics America Inc - R5F213M8KNNP#W0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART, USB
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	30
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213m8knnp-w0

Table 1.5 Product List for R8C/3MK Group **Current of Jun 2011**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F213M8KNNP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B	N version	
R5F213MCKNNP	128Kbytes	1 Kbyte × 4	10 Kbytes	PWQN0040KB-B		
R5F213M8KNXXXNP	64Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B	N version	Factory programming product (1)
R5F213MCKNXXXNP	128Kbytes	1 Kbyte × 4	10 Kbytes	PWQN0040KB-B		

Note:
1. The user ROM is programmed before shipment.

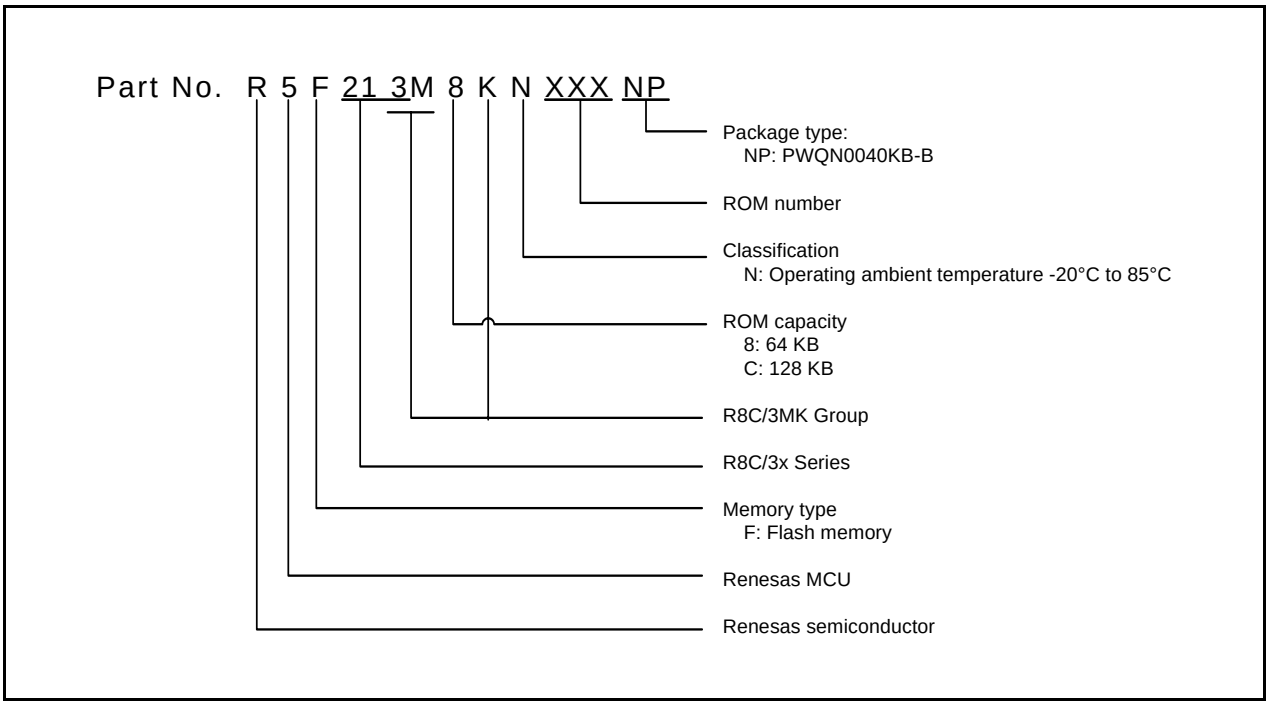


Figure 1.2 Part Number, Memory Size, and Package of R8C/3MK Group

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS (2)	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. (1) To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Serial interface	CLK0, CLK1, CLK2, CLK3	I/O	Transfer clock I/O pins.
	RXD0, RXD1, RXD2, RXD3	I	Serial data input pins.
	TXD0, TXD1, TXD2, TXD3	O	Serial data output pins.
	$\overline{\text{CTS2}}$	I	Transmission control input pin.
	$\overline{\text{RTS2}}$	O	Reception control output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I^2C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.

I: Input O: Output I/O: Input and output

Notes:

1. Refer to the oscillator manufacturer for oscillation characteristics.
2. This pin is not available in the R8C/3MU Group.

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O Type	Description
USB	USB_DP/USB_DM	I/O	D+/D- I/O pin of the USB on-chip transceiver. Connect this pin to the D+/D- pin of the USB bus.
	USB_VBUS	I	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. Whether VBUS is connected or disconnected can be detected during operation as a function.
	USB_VBUSEN (1)	O	VBUS (5 V) supply enable signal for external power supply chip.
	USB_OVRCURA (1)	I	External overcurrent detection signal should be connected to this pin. VBUS comparator signal should be connected to this pin when the USB host power supply chip is connected.
	USB_DPUPE	O	1.5 kΩ pull-up resistor control signal for USB D+ signal when operating as a function controller.
	USB_VCC	I/O	USB power supply pin.
Reference voltage input	VREF (1)	I	Reference voltage input pin to A/D converter.
A/D converter	AN0, AN3 to AN11 (1)	I	Analog input pins to A/D converter.
	$\overline{\text{ADTRG}}$ (1)	I	AD external trigger input pin.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_4, P0_7, P1_0 to P1_7, P3_0, P3_3 to P3_5, P3_7, P4_5 to P4_7, P6_5 to P6_7, P7_6, P7_7, P8_1 to P8_3	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input O: Output I/O: Input and output

Note:
1. This pin is not available in the R8C/3MU Group.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh			
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh			
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh			
00BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h	Drive Capacity Control Register 2	DRR2	00h
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2E30h	Interrupt Enable Register 0	INTENB0	00h
2E31h			00h
2E32h	Interrupt Enable Register 1 (2)	INTENB1	00h
2E33h			00h
2E34h			
2E35h			
2E36h	BRDY Interrupt Enable Register	BRDYENB	00h
2E37h			00h
2E38h	NRDY Interrupt Enable Register	NRDYENB	00h
2E39h			00h
2E3Ah	BEMP Interrupt Enable Register	BEMPENB	00h
2E3Bh			00h
2E3Ch	SOF Output Configuration Register	SOFCFG	00h
2E3Dh			00h
2E3Eh			
2E3Fh			
2E40h	Interrupt Status Register 0	INTSTS0	X0000000b
2E41h			X0000000b
2E42h	Interrupt Status Register 1 (2)	INTSTS1	00h
2E43h			XX0X0000b
2E44h			
2E45h			
2E46h	BRDY Interrupt Status Register	BRDYSTS	00h
2E47h			00h
2E48h	NRDY Interrupt Status Register	NRDYSTS	00h
2E49h			00h
2E4Ah	BEMP Interrupt Status Register	BEMPSTS	00h
2E4Bh			00h
2E4Ch	Frame Number Register	FRMNUM	00h
2E4Dh			00h
2E4Eh			
2E4Fh			
2E50h	USB Address Register	USBADDR	00h
2E51h			00h
2E52h			
2E53h			
2E54h	USB Request Type Register	USBREQ	00h
2E55h			00h
2E56h	USB Request Value Register	USBVAL	00h
2E57h			00h
2E58h	USB Request Index Register	USBINDX	00h
2E59h			00h
2E5Ah	USB Request Length Register	USBLENG	00h
2E5Bh			00h
2E5Ch	DCP Configuration Register	DCPCFG	00h
2E5Dh			00h
2E5Eh	DCP Max Packet Size Register	DCPMAXP	40h
2E5Fh			00h
2E60h	DCP Control Register	DCPCTR	00h
2E61h			00h
2E62h			
2E63h			
2E64h	Pipe Window Select Register	PIPESEL	00h
2E65h			00h
2E66h			
2E67h			
2E68h	Pipe Configuration Register	PIPECFG	00h
2E69h			00h
2E6Ah			
2E6Bh			
2E6Ch	Pipe Max Packet Size Register	PIPEMAXP	00h
2E6Dh			00h
2E6Eh	Pipe Period Control Register (2)	PIPEPERI	00h
2E6Fh			00h

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/3MU Group.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After Reset
2E70h			
2E71h			
2E72h			
2E73h			
2E74h			
2E75h			
2E76h	Pipe 4 Control Register	PIPE4CTR	00h
2E77h			00h
2E78h	Pipe 5 Control Register	PIPE5CTR	00h
2E79h			00h
2E7Ah	Pipe 6 Control Register	PIPE6CTR	00h
2E7Bh			00h
2E7Ch	Pipe 7 Control Register	PIPE7CTR	00h
2E7Dh			00h
2E7Eh			
2E7Fh			
2E80h			
:			
2E8Fh			
2E90h			
2E91h			
2E92h			
2E93h			
2E94h			
2E95h			
2E96h			
2E97h			
2E98h			
2E99h			
2E9Ah			
2E9Bh			
2E9Ch	Pipe 4 Transaction Counter Enable Register	PIPE4TRE	00h
2E9Dh			00h
2E9Eh	Pipe 4 Transaction Counter Register	PIPE4TRN	00h
2E9Fh			00h
2EA0h	Pipe 5 Transaction Counter Enable Register	PIPE5TRE	00h
2EA1h			00h
2EA2h	Pipe 5 Transaction Counter Register	PIPE5TRN	00h
2EA3h			00h
2EA4h			
2EA5h			
2EA6h			
2EA7h			
2EA8h			
2EA9h			
2EAAh			
2EABh			
2EACh			
2EADh			
:			
2ECFh			
2ED0h	Device Address 0 Configuration Register (2)	DEVADD0	00h
2ED1h			00h
2ED2h	Device Address 1 Configuration Register (2)	DEVADD1	00h
2ED3h			00h
2ED4h	Device Address 2 Configuration Register (2)	DEVADD2	00h
2ED5h			00h
2ED6h	Device Address 3 Configuration Register (2)	DEVADD3	00h
2ED7h			00h
2ED8h	Device Address 4 Configuration Register (2)	DEVADD4	00h
2ED9h			00h
2EDAh	Device Address 5 Configuration Register (2)	DEVADD5	00h
2EDBh			00h
2EDCh			
2EDDh			
:			
2EFFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/3MU Group.

Table 5.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20	—	85	°C
—	Data hold time (7)	Ambient temperature = 55 °C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

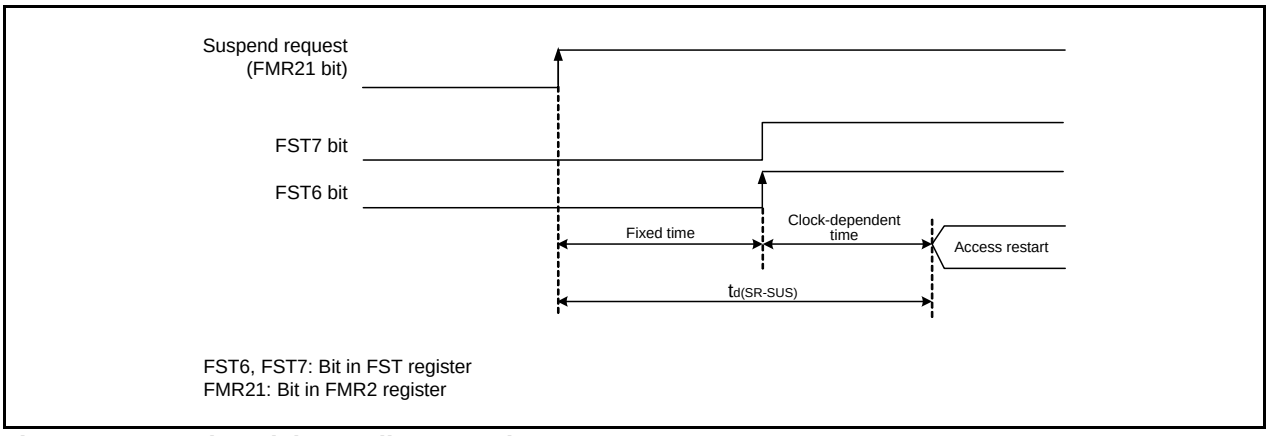


Figure 5.4 Time delay until Suspend

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V	36.0	40	44.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	V_{CC} = 1.8 V to 5.5 V	33.178	36.864	40.550	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V	28.8	32	35.2	MHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	0.5	3	ms
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	400	—	µA

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	30	100	µs
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	2	—	µA

Note:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

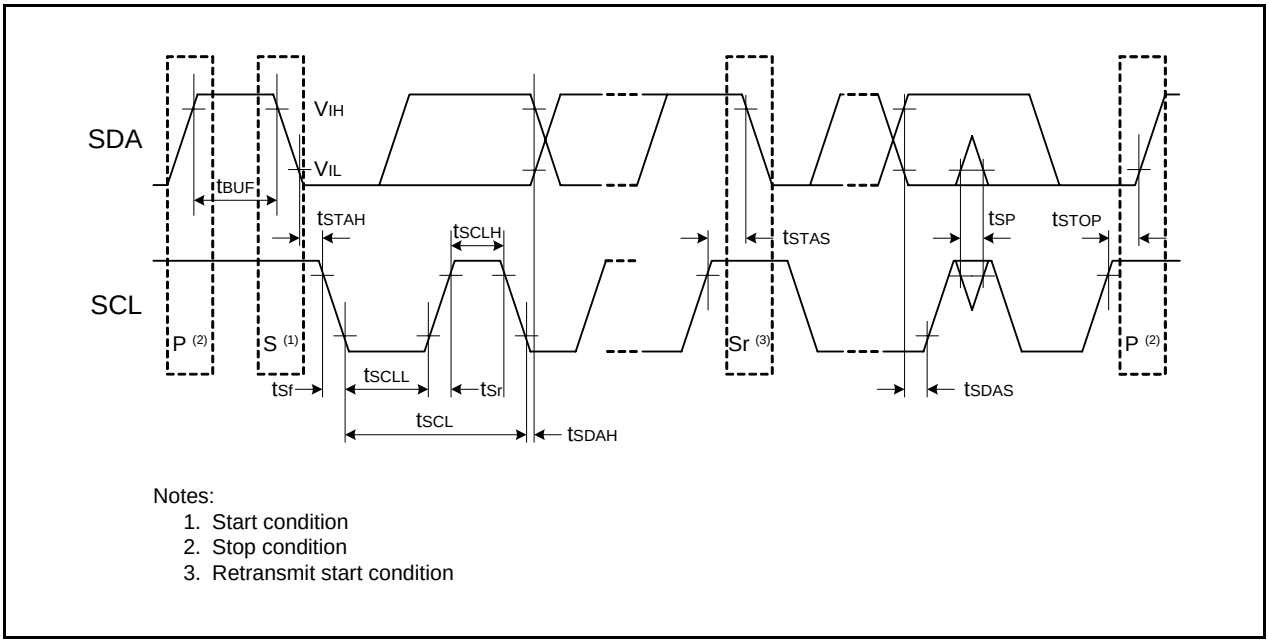
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.15 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.9 I/O Timing of I²C bus Interface

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{W(CKH)}$	CLKi input “H” width	400	—	ns
$t_{W(CKL)}$	CLKi input “L” width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

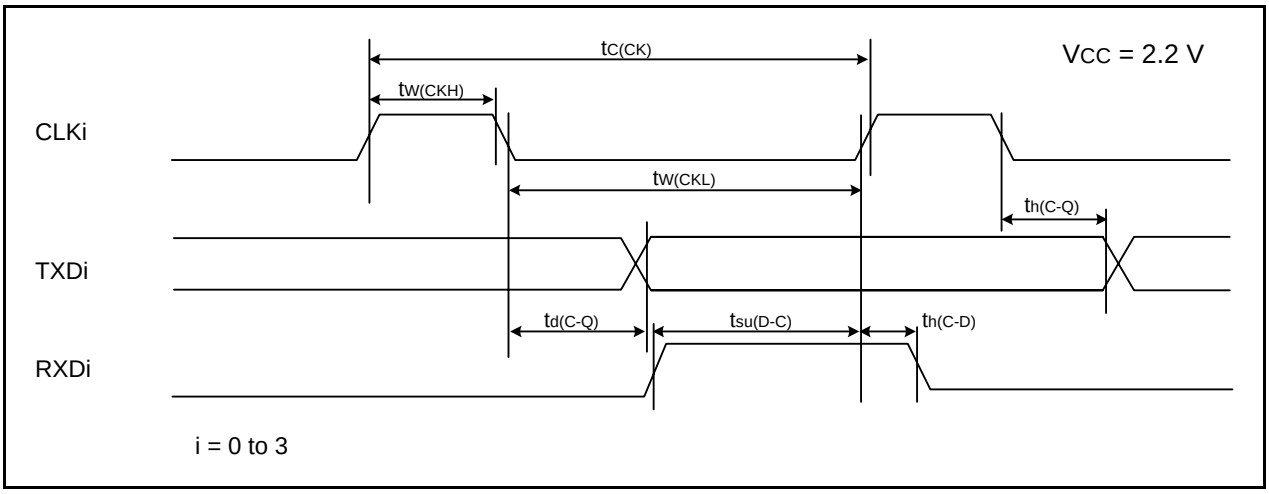


Figure 5.20 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.33 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

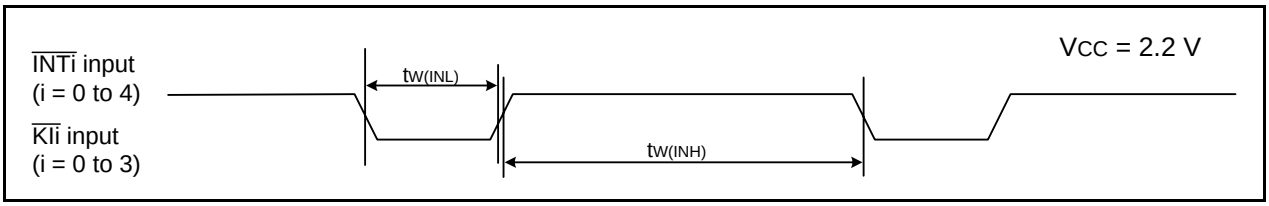


Figure 5.21 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 2.2 V

Table 5.35 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage	When USB function is used				3.0	5.0	5.5	V
		When USB function is not used				1.8	5.0	5.5	V
UV_{CC}	USB Supply Voltage (When UVCC pin is input)	When USB function is used			V_{CC}/AV_{CC} = 3.0 to 3.6 V	—	V_{CC}/AV_{CC} (4)	—	V
		When USB function is not used			V_{CC}/AV_{CC} = 1.8 to 5.5 V	—	V_{CC}/AV_{CC} (4)	—	V
V_{SS}/AV_{SS}	Supply voltage					—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	—	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65 V_{CC}	—	V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8 V_{CC}	—	V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85 V_{CC}	—	V_{CC}	V
		External clock input (XOUT)				1.2	—	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.2 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2 V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.3 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2 V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.45 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.35 V_{CC}	V
		External clock input (XOUT)				0	—	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				—	—	−160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				—	—	−80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				—	—	−10	mA
		Drive capacity High				—	—	−40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				—	—	−5	mA
		Drive capacity High				—	—	−20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
fOCO40M	When used as the count source for timer RC (3)				2.7 V ≤ V_{CC} ≤ 5.5 V	32	—	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$t_{su(PLL)}$	PLL frequency symthesizer stabilization wait time				4.0 V ≤ V_{CC} ≤ 5.5 V	—	—	2	ms
					2.7 V ≤ V_{CC} < 4.0 V	—	—	3	ms

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85 °C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of V_{CC} = 2.7 to 5.5 V.
4. Connect V_{CC}/AV_{CC} for the UV_{CC} pin input.

Table 5.36 A/D Converter Characteristics

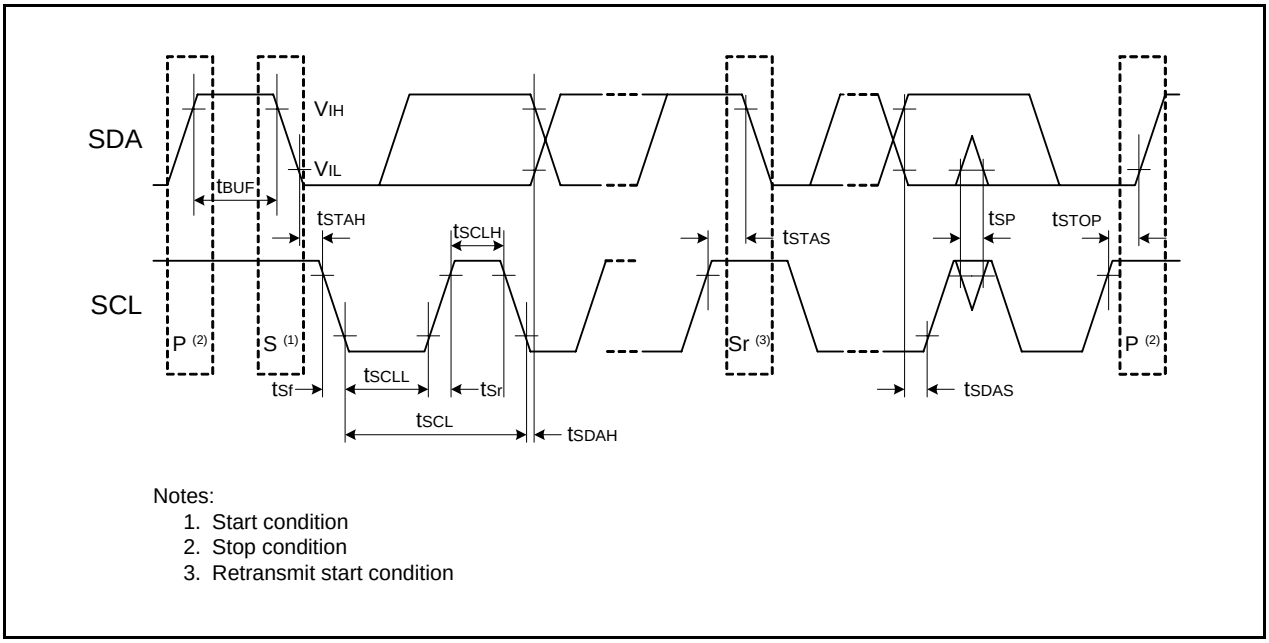
Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AV_{CC}		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
I_{Vref}	V_{ref} current		V_{CC} = 5.0 V, XIN = f1 = ϕAD = 20 MHz		—	45	—	µA
V_{ref}	Reference voltage				2.2	—	AV_{CC}	V
VIA	Analog input voltage(3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.49 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.30 I/O Timing of I²C bus Interface

Timing requirements (Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 5.58 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

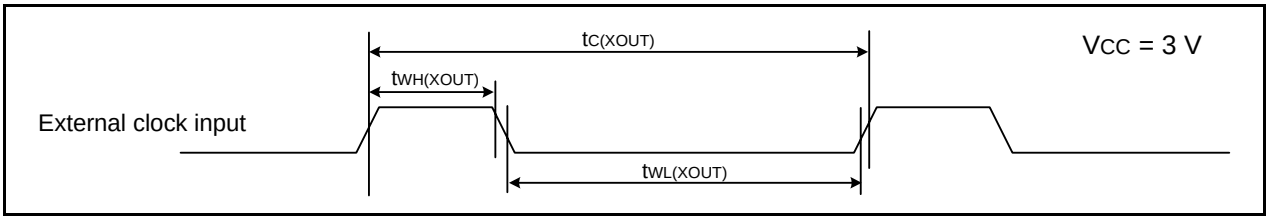


Figure 5.35 External Clock Input Timing Diagram when V_{CC} = 3 V

Table 5.59 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

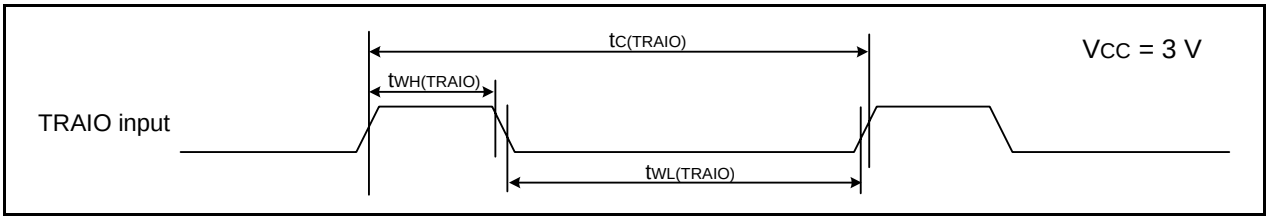


Figure 5.36 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.62 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	—	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, SDA, SSO, SSCK, $\overline{SCS}$			0.05	0.20	—	V
		$\overline{RESET}$			0.05	0.20	—	V
I_{IH}	Input “H” current		V_I = 2.2 V, V_{CC} = 2.2 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 2.2 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 1.8 V ≤ V_{CC} < 2.7 V, T_{opr} = –20 to 85 °C (N version), and f(XIN) = 5 MHz, unless otherwise specified.

REVISION HISTORY	R8C/3MU Group, R8C/3MK Group Datasheet

Rev.	Date	Description	
		Page	Summary
• R8C/3MU Group Datasheet (R01DS0037EJ0100)			
0.01	May 17, 2010	—	First Edition issued
0.02	Nov 08, 2010	All	Package code: “PWQN0040KB-A (previous code: 40PJS-A)” → “PWQN0040KB-B (previous code: 40PJS-B)”
		2	Table 1.1 I/O Ports, DTC revised LIN Module added
		3	Table 1.2 Package revised
		4	Table 1.3 revised Figure 1.1 revised
		5	Figure 1.2 LIN Module, Note 1 and 2 added
		6	Figure 1.3 revised
		7	Table 1.4 Part Number 25, 34, 38 revised
		8	Table 1.5 Serial interface revised
		13	Figure 3.1 “Part Number” revised
		15	Table 4.2 004Ah deleted
		16	Table 4.3 008Ch, 008Dh, 009Ch to 009Fh, 00BCh, 00BEh, 00BFh deleted
		20	Table 4.7 0186h deleted
		25	Table 4.12 2E02h, 2E03h deleted
		29	Package Dimensions added
1.00	Feb 25, 2011	All pages	“Preliminary”, “Under development” deleted
		2	Table 1.1 DTC revised
		3	Table 1.2 revised
		4	Table 1.3, Figure 1.1 revised
		5	Figure 1.2 revised
		6	Figure 1.3 revised
		8	Table 1.5 revised
		13	3.1 revised, Figure 3.1 “Part Number” added
		15	Table 4.2 0041h revised
		16	Table 4.3 00BBh revised
		18	Table 4.5 0133h deleted
		20	Table 4.7 0181h revised
		25	Table 4.12 2E04h and 2E05h revised
		26	Table 4.13 2E40h and 2E41h revised 2E32h, 2E33h, 2E42h, 2E43h, 2E6Eh and 2E6Fh deleted
		27	Table 4.14 2ED0h to 2EDBh deleted
		28	Table 4.15 2F04h, 2F11h and 2F13h deleted
		29 to 54	5. Electrical Characteristics added
• R8C/3MK Group Datasheet (R01DS0038EJ0100)			
0.01	Jun 30, 2010	—	First Edition issued
0.02	Nov 08, 2010	All	Package code: “PWQN0040KB-A (previous code: 40PJS-A)” → “PWQN0040KB-B (previous code: 40PJS-B)”
		2	Table 1.1 I/O Ports, DTC revised LIN Module added

REVISION HISTORY	R8C/3MU Group, R8C/3MK Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.02	Nov 08, 2010	3	Table 1.2 A/D converter, Package revised
		4	Table 1.3 "(D)"added Table 1.3, Figure 1.1 Package revised
		5	Figure 1.2 I/O Ports, A/D converter revised LIN Module added
		6	Figure 1.3 revised
		7	Table 1.4 Pin Number 2, 7, 9, 22 revised
		9	Table 1.6 USB "USB_OVRCURA" added
		14	Table 4.1 0026h "On-Chip Reference Voltage Control Register OCVREFCR 00h" added
		15	Table 4.2 004Ah deleted
		16	Table 4.3 00BBh "UART2 Special Mode Register 5 U2SMR5 XXh" added 00BDh "UART2 Special Mode Register 3 U2SMR3 000X0X0Xb2" added
		18	Table 4.5 0105h "LIN Control Register 2 LINCR2 00h" added 0106h "LIN Control Register LINCR 00h" added 0107h "LIN Status Register LINST 00h" added
		25	Table 4.12 2E02h, 2E03h deleted
		29	Package Dimensions added
1.00	Feb 25, 2011	All pages	"Preliminary", "Under development" deleted
		3	Table 1.2 revised
		4	Table 1.3, Figure 1.1 revised
		5	Figure 1.2 revised
		6	Figure 1.3 revised
		7	Table 1.4 revised
		9	Table 1.6 revised
		13	3.1 revised, Figure 3.1 "Part Number" added
		14	Table 4.1 0026h revised
		15	Table 4.2 0041h revised
		16	Table 4.3 00BBh revised
		20	Table 4.7 0181h revised
		25	Table 4.12 2E04h and 2E05h revised
		26	Table 4.13 2E40h to 2E43h revised
		27	Table 4.14 2ED2h to 2ED7h deleted
		28	Table 4.15 2F04h, 2F11h and 2F13h deleted, 2F10h added
		29 to 56	5. Electrical Characteristics added

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SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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