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Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152rdt6

1.2 Product List

Tables 1.4 and 1.5 list Product List for Each Group. Figures 1.1 and 1.2 show a Part Number, Memory Size, and Package of Each Group.

Table 1.4 Product List for R8C/3MU Group

Current of Jun 2011

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F213M6UNNP	32 Kbytes	1 Kbyte × 4	4 Kbytes	PWQN0040KB-B	N version	
R5F213M8UNNP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B		
R5F213M6UNXXXNP	32 Kbytes	1 Kbyte × 4	4 Kbytes	PWQN0040KB-B	N version	Factory programming product ⁽¹⁾
R5F213M8UNXXXNP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B		

Note:

1. The user ROM is programmed before shipment.

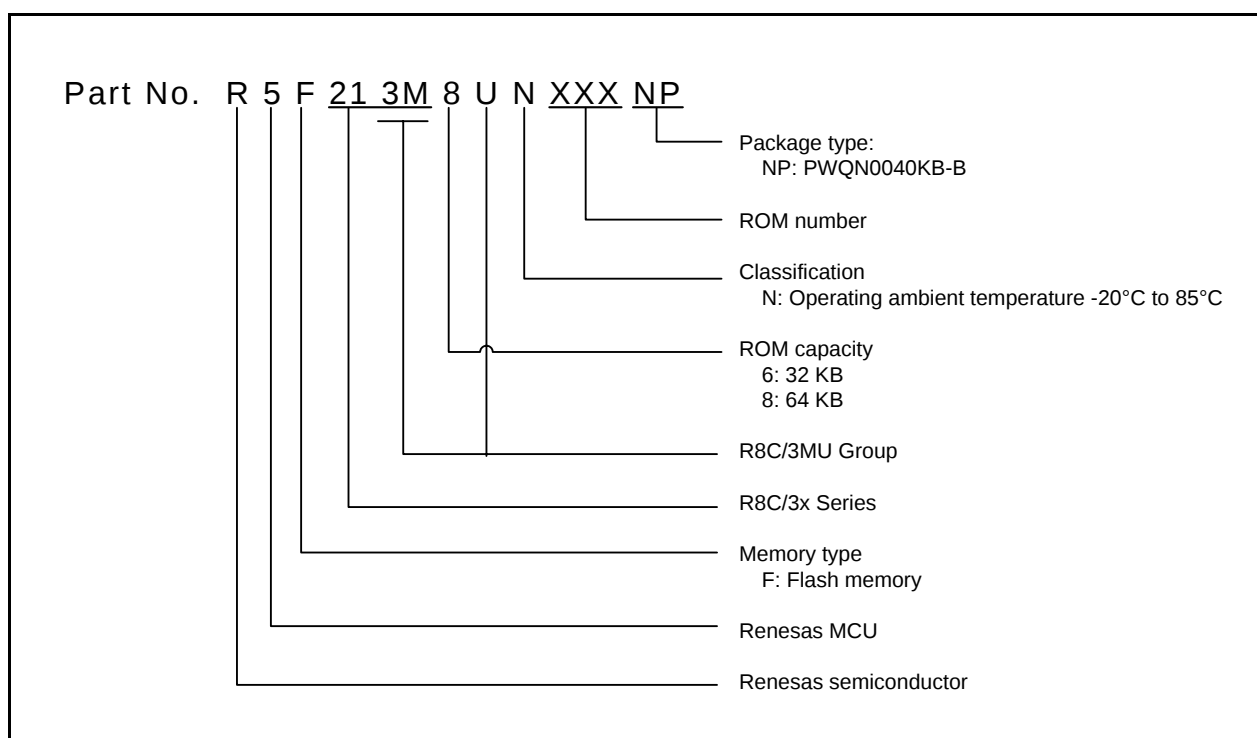


Figure 1.1 Part Number, Memory Size, and Package of R8C/3MU Group

1.4 Pin Assignment

Figures 1.5 and 1.6 show Pin Assignment (Top View) of Each Group. Table 1.6 outlines the Pin Name Information by Pin Number.

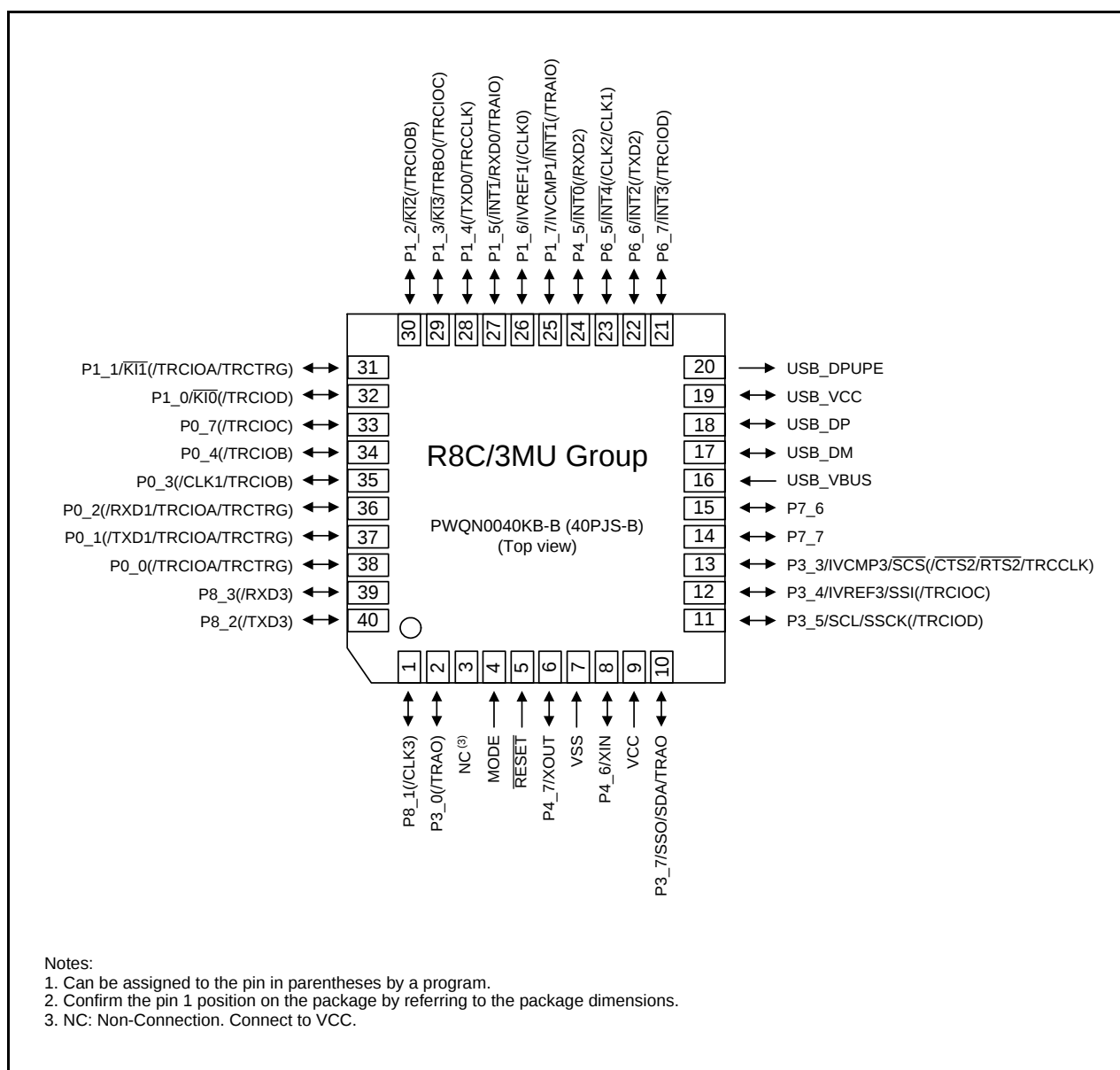


Figure 1.5 Pin Assignment (Top View) of R8C/3MU Group

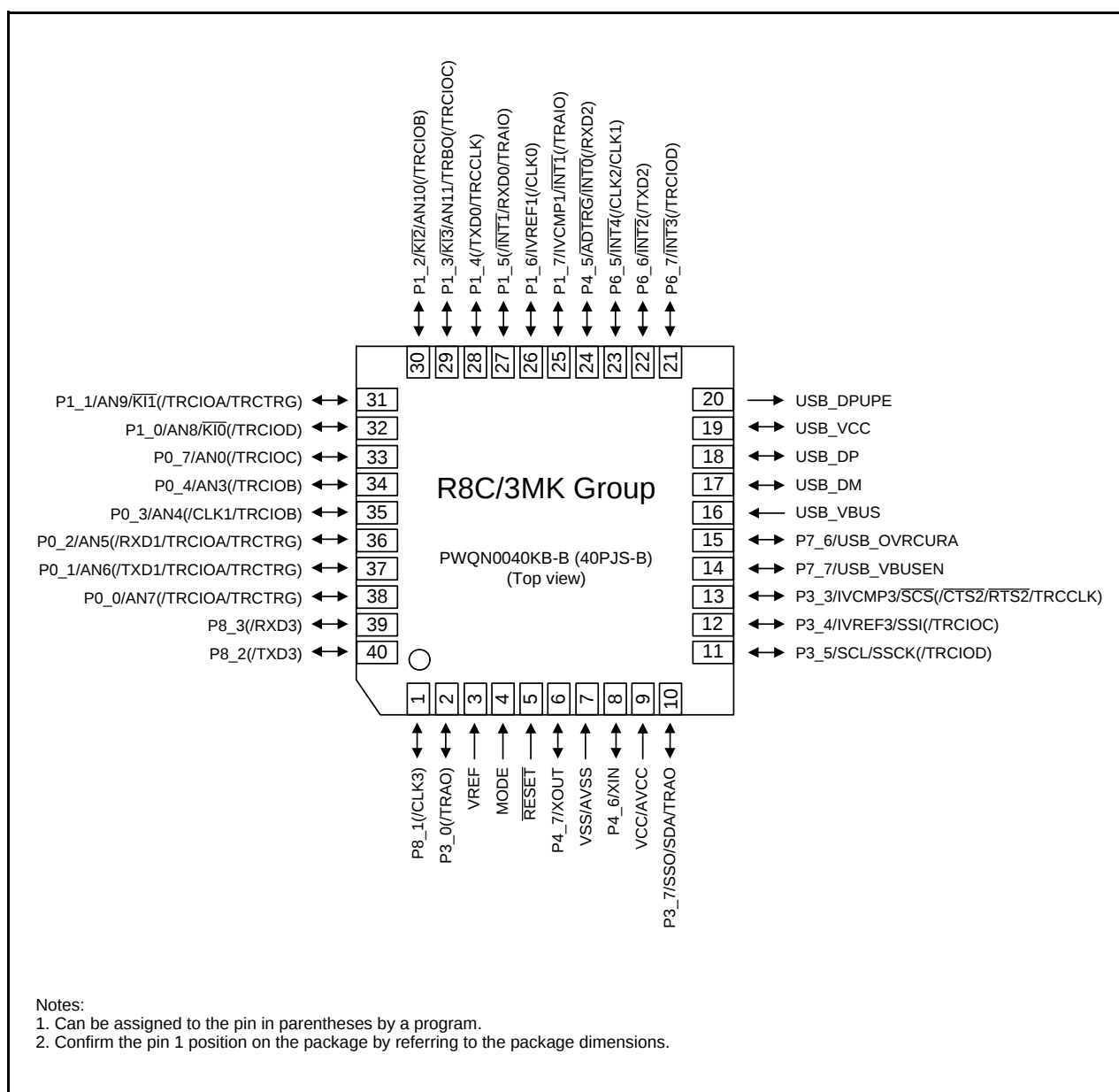


Figure 1.6 Pin Assignment (Top View) of R8C/3MK Group

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules						
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	USB	A/D Converter, Comparator B
1		P8_1			(CLK3)				
2		P3_0		(TRA0)					
3									VREF ⁽²⁾
4	MODE								
5	RESET								
6	XOUT	P4_7							
7	VSS/ AVSS ⁽²⁾								
8	XIN	P4_6							
9	VCC/ AVCC ⁽²⁾								
10		P3_7		TRA0		SSO	SDA		
11		P3_5		(TRCIOD)		SSCK	SCL		
12		P3_4		(TRCIOC)		SSI			IVREF3
13		P3_3		(TRCCLK)	(CTS2/ RTS2)	SCS			IVCMP3
14		P7_7						USB_VBUSEN ⁽²⁾	
15		P7_6						USB_OVRCURA ⁽²⁾	
16								USB_VBUS	
17								USB_DM	
18								USB_DP	
19								USB_VCC	
20								USB_DPUPE	
21		P6_7	INT3	(TRCIOD)					
22		P6_6	INT2		(TXD2)				
23		P6_5	INT4		(CLK2/ CLK1)				
24		P4_5	INT0		(RXD2)				ADTRG ⁽²⁾
25		P1_7	INT1	(TRAIO)					IVCMP1
26		P1_6			(CLK0)				IVREF1
27		P1_5	(INT1)	(TRAIO)	(RXD0)				
28		P1_4		(TRCCLK)	(TXD0)				
29		P1_3	KI3	TRBO (/TRCIOC)					AN11 ⁽²⁾
30		P1_2	KI2	(TRCIOB)					AN10 ⁽²⁾
31		P1_1	KI1	(TRCIOA/ TRCTRG)					AN9 ⁽²⁾
32		P1_0	KI0	(TRCIOD)					AN8 ⁽²⁾
33		P0_7		(TRCIOC)					AN0 ⁽²⁾
34		P0_4		(TRCIOB)					AN3 ⁽²⁾
35		P0_3		(TRCIOB)	(CLK1)				AN4 ⁽²⁾
36		P0_2		(TRCIOA/ TRCTRG)	(RXD1)				AN5 ⁽²⁾
37		P0_1		(TRCIOA/ TRCTRG)	(TXD1)				AN6 ⁽²⁾
38		P0_0		(TRCIOA/ TRCTRG)					AN7 ⁽²⁾
39		P8_3			(RXD3)				
40		P8_2			(TXD3)				

Notes:

1. Can be assigned to the pin in parentheses by a program.
2. This pin is not available in the R8C/3MU Group.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.3 SFR Information (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh			
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh			
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh			
00BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.14 SFR Information (14) ⁽¹⁾

Address	Register	Symbol	After Reset
2E70h			
2E71h			
2E72h			
2E73h			
2E74h			
2E75h			
2E76h	Pipe 4 Control Register	PIPE4CTR	00h
2E77h			00h
2E78h	Pipe 5 Control Register	PIPE5CTR	00h
2E79h			00h
2E7Ah	Pipe 6 Control Register	PIPE6CTR	00h
2E7Bh			00h
2E7Ch	Pipe 7 Control Register	PIPE7CTR	00h
2E7Dh			00h
2E7Eh			
2E7Fh			
2E80h			
:			
2E8Fh			
2E90h			
2E91h			
2E92h			
2E93h			
2E94h			
2E95h			
2E96h			
2E97h			
2E98h			
2E99h			
2E9Ah			
2E9Bh			
2E9Ch	Pipe 4 Transaction Counter Enable Register	PIPE4TRE	00h
2E9Dh			00h
2E9Eh	Pipe 4 Transaction Counter Register	PIPE4TRN	00h
2E9Fh			00h
2EA0h	Pipe 5 Transaction Counter Enable Register	PIPE5TRE	00h
2EA1h			00h
2EA2h	Pipe 5 Transaction Counter Register	PIPE5TRN	00h
2EA3h			00h
2EA4h			
2EA5h			
2EA6h			
2EA7h			
2EA8h			
2EA9h			
2EAAh			
2EABh			
2EACH			
2EADh			
:			
2ECFh			
2ED0h	Device Address 0 Configuration Register ⁽²⁾	DEVADD0	00h
2ED1h			00h
2ED2h	Device Address 1 Configuration Register ⁽²⁾	DEVADD1	00h
2ED3h			00h
2ED4h	Device Address 2 Configuration Register ⁽²⁾	DEVADD2	00h
2ED5h			00h
2ED6h	Device Address 3 Configuration Register ⁽²⁾	DEVADD3	00h
2ED7h			00h
2ED8h	Device Address 4 Configuration Register ⁽²⁾	DEVADD4	00h
2ED9h			00h
2EDAh	Device Address 5 Configuration Register ⁽²⁾	DEVADD5	00h
2EDBh			00h
2EDCh			
2EDDh			
:			
2EFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/3MU Group.

5. Electrical Characteristics

5.1 R8C/3MU Group

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{cc}	Supply voltage		–0.3 to 6.5	V
V _i	Input voltage		–0.3 to V _{cc} + 0.3	V
V _o	Output voltage		–0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	–20°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		–20 to 85 (N version)	°C
T _{stg}	Storage temperature		–65 to 150	°C

Table 5.14 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (2)
tHI	SSCK clock "H" width			0.4	—	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	—	0.6	tsucyc
tRISE	SSCK clock rising time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tFALL	SSCK clock falling time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
tH	SSO, SSI data input hold time			1	—	—	tcyc (2)
tLEAD	SCS setup time	Slave		1tcyc + 50	—	—	ns
tLAG	SCS hold time	Slave		1tcyc + 50	—	—	ns
tOD	SSO, SSI data output delay time			—	—	1	tcyc (2)
tsA	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns
toR	SSI slave out open time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V, and T_{opr} = -20 to 85 °C (N version), unless otherwise specified.
2. 1tcyc = 1/f_l(s)

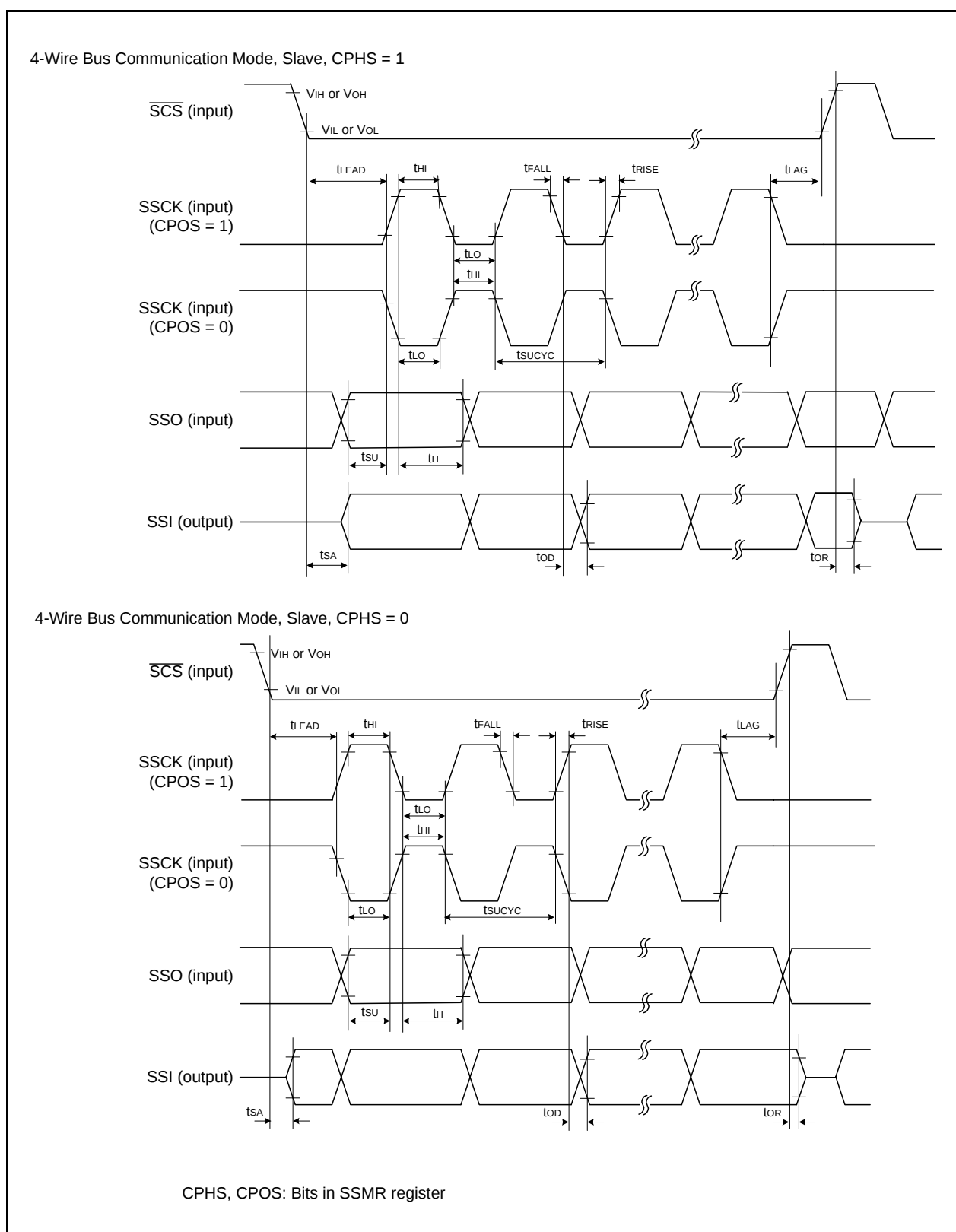


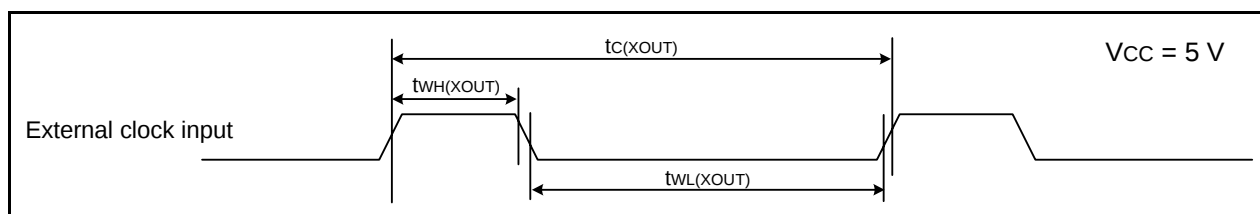
Figure 5.7 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.17 Electrical Characteristics (2) [$3.3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$]
($T_{opr} = -20$ to $85\text{ }^{\circ}\text{C}$ (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15
		XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8		—	3.0	—	mA
		XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC=MSTTRC=1		—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	μA
			Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0
		XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0		—	15	—	μA

Timing Requirements (Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = 25\text{ }^{\circ}\text{C}$)**Table 5.18 External Clock Input (XOUT)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input "H" width	24	—	ns
$t_{WL(XOUT)}$	XOUT input "L" width	24	—	ns

**Figure 5.10 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.19 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	—	ns

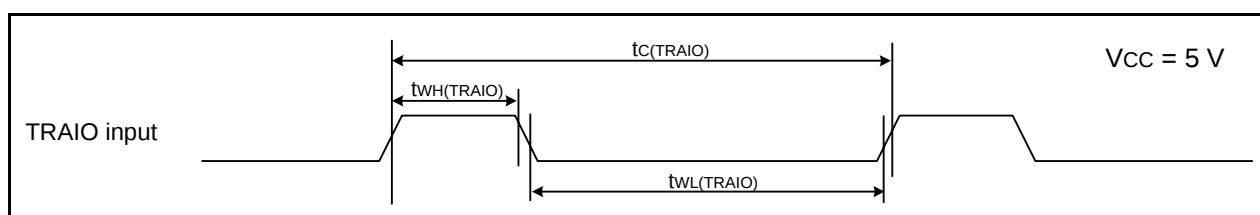
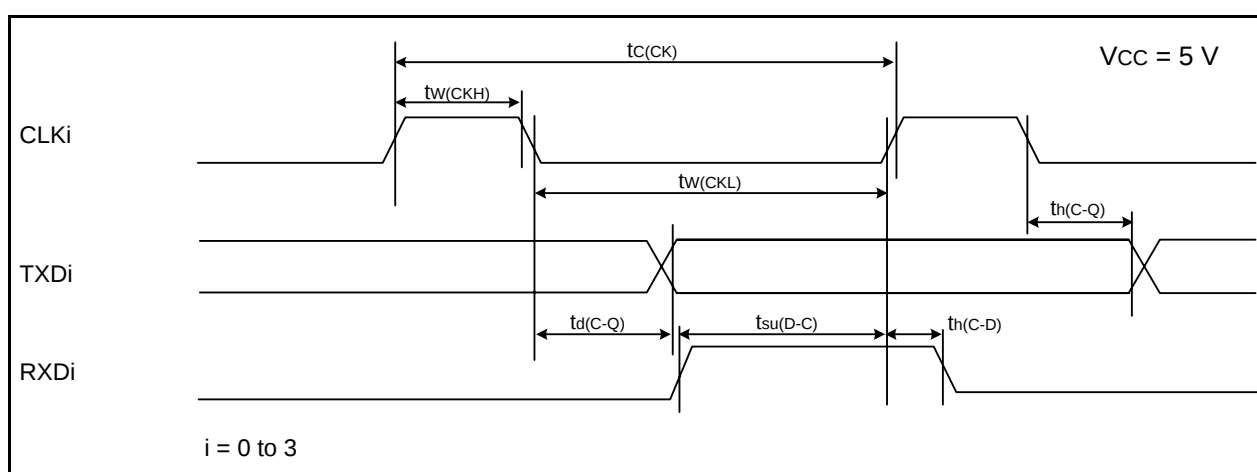
**Figure 5.11 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.20 Serial Interface

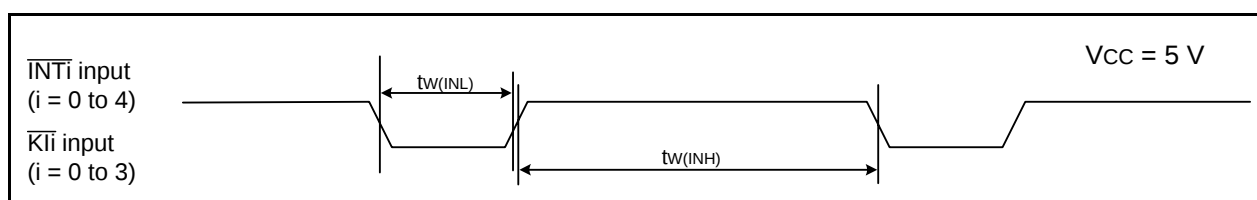
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 3$ **Figure 5.12 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	250 ⁽²⁾	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

**Figure 5.13 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 5 V**

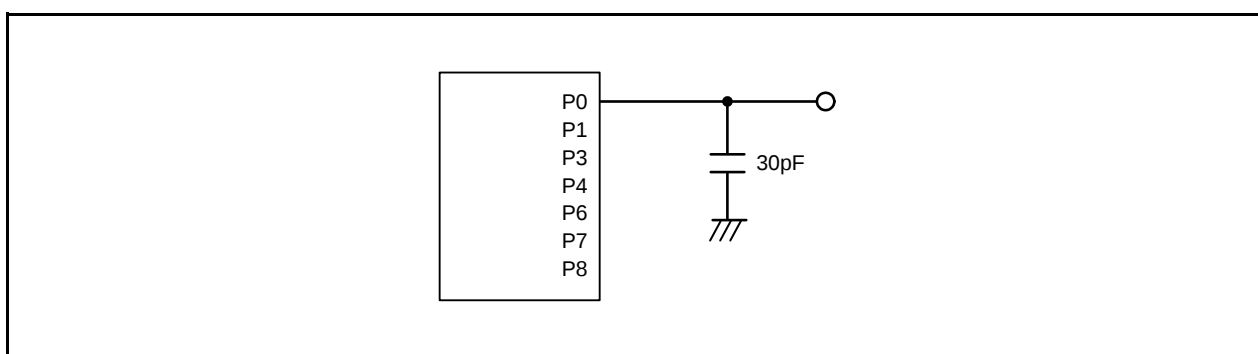


Figure 5.22 Ports P0, P1, P3, P4, P6, P7 and P8 Timing Measurement Circuit

Table 5.39 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.48 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (2)
tHI	SSCK clock "H" width			0.4	—	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	—	0.6	tsucyc
tRISE	SSCK clock rising time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tFALL	SSCK clock falling time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
tH	SSO, SSI data input hold time			1	—	—	tcyc (2)
tLEAD	SCS setup time	Slave		1tcyc + 50	—	—	ns
tLAG	SCS hold time	Slave		1tcyc + 50	—	—	ns
tOD	SSO, SSI data output delay time			—	—	1	tcyc (2)
tsA	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns
toR	SSI slave out open time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V, and T_{opr} = -20 to 85 °C (N version), unless otherwise specified.
2. 1tcyc = 1/f1(s)

Table 5.49 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cyC} + 600 ⁽²⁾	—	—	ns
t _{SCLH}	SCL input "H" width		3t _{cyC} + 300 ⁽²⁾	—	—	ns
t _{SCLL}	SCL input "L" width		5t _{cyC} + 500 ⁽²⁾	—	—	ns
t _{sf}	SCL, SDA input fall time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1t _{cyC} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cyC} ⁽²⁾	—	—	ns
t _{STAH}	Start condition input hold time		3t _{cyC} ⁽²⁾	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cyC} ⁽²⁾	—	—	ns
t _{STOP}	Stop condition input setup time		3t _{cyC} ⁽²⁾	—	—	ns
t _{SDAS}	Data input setup time		1t _{cyC} + 40 ⁽²⁾	—	—	ns
t _{SDAH}	Data input hold time		10	—	—	ns

Notes:

1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -20 to 85 °C (N version), unless otherwise specified.
2. 1t_{cyC} = 1/f₁(s)

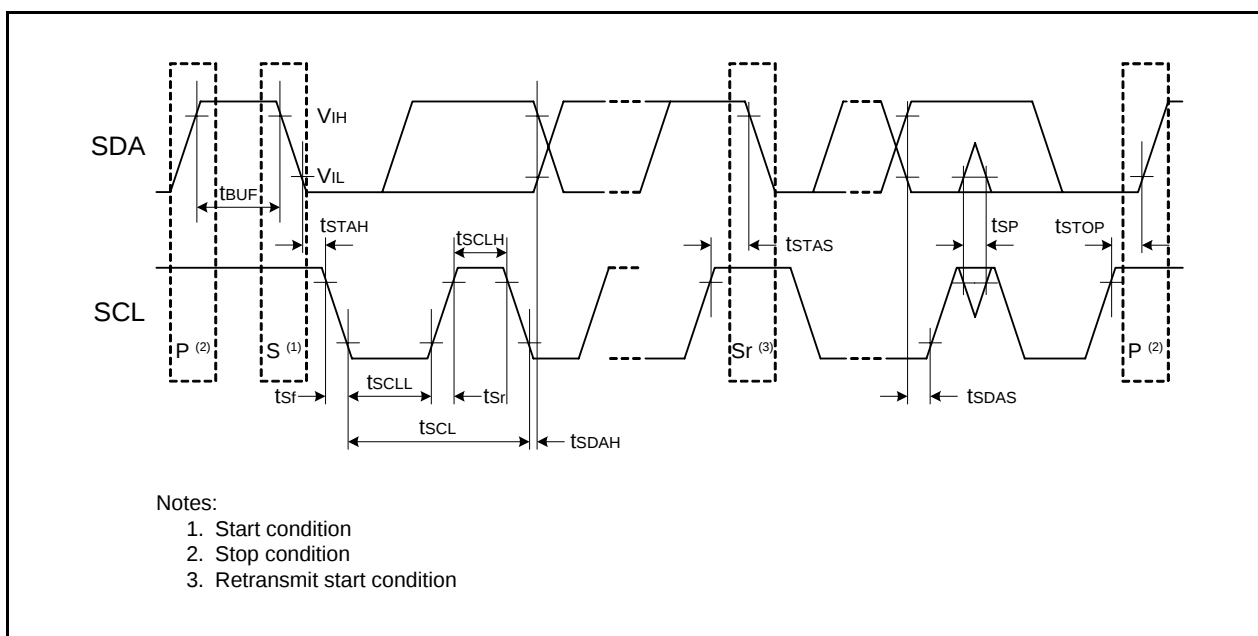
**Figure 5.30 I/O Timing of I²C bus Interface**

Table 5.50 Electrical Characteristics (1) [$4.2\text{ V} \leq V_{CC} \leq 5.5\text{ V}$]

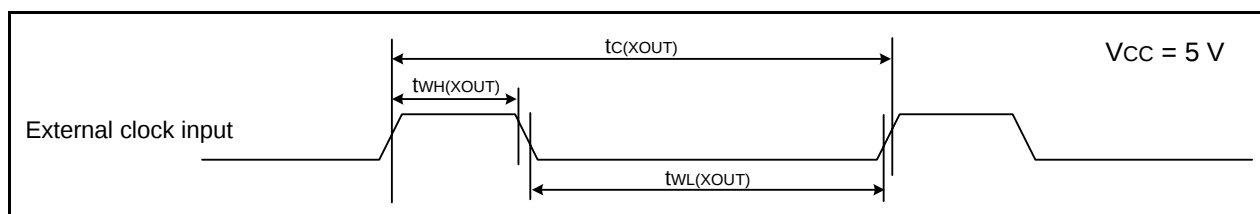
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High $V_{CC} = 5\text{ V}$	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity Low $V_{CC} = 5\text{ V}$	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	V _{CC} = 5 V	I _{OH} = -200 μA	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High $V_{CC} = 5\text{ V}$	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low $V_{CC} = 5\text{ V}$	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	V _{CC} = 5 V	I _{OL} = 200 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, USB_OVRCURA, USB_VBUS, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, RXD3, CLK0, CLK1, CLK2, CLK3, CTS2, SSI, SCL, SDA, SSO, SSCK, SCS			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5.0 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5.0 V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0 V		25	50	100	k Ω
R _{FXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

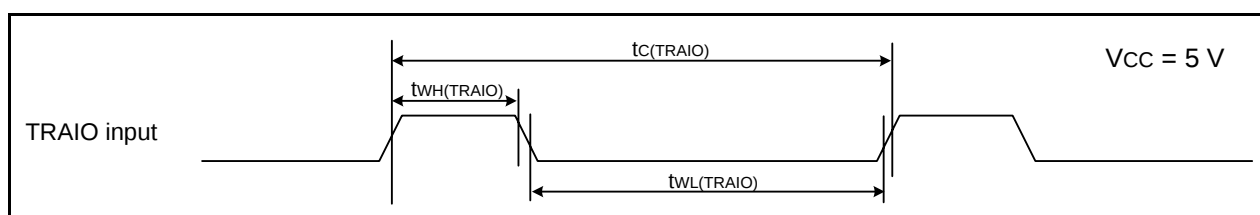
1. $4.2\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, T_{opr} = -20 to 85 °C (N version), and f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements (Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = 25\text{ }^{\circ}\text{C}$)**Table 5.52 External Clock Input (XOUT)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{XOUT})$	XOUT input cycle time	50	—	ns
$t_{WH}(\text{XOUT})$	XOUT input "H" width	24	—	ns
$t_{WL}(\text{XOUT})$	XOUT input "L" width	24	—	ns

**Figure 5.31 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.53 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	100	—	ns
$t_{WH}(\text{TRAIO})$	TRAIO input "H" width	40	—	ns
$t_{WL}(\text{TRAIO})$	TRAIO input "L" width	40	—	ns

**Figure 5.32 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

