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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MCS 51
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-55°C ~ 225°C (TA)
Mounting Type	Through Hole
Package / Case	40-CDIP (0.600", 15.24mm)
Supplier Device Package	40-Cerdip
Purchase URL	https://www.e-xfl.com/product-detail/honeywell-microelectronics-and-precision-sensors/ht83c51

High Temperature 83C51 Microcontroller HT83C51

The HT83C51 is a monolithic 8-bit microcontroller that is pin equivalent to the Intel 8XC51FC microcontroller. Fabricated with Honeywell's HTMOS™ dielectrically isolated high temperature process, the HT83C51 is designed specifically for severe high temperature applications such as downhole oil well, aerospace, turbine engine and industrial control.

The HT83C51 uses the standard MCS-51 instruction set which is optimized for control applications. Pin-for-pin equivalent to the MCS-51 series product, it is compatible with all known development environments. Key features include the programmable counter array, watch dog timer, enhanced serial port for multi-processor communication and a hierarchical interrupt structure. Software selectable idle is included for reduced power. The HT83C51 varies from the standard 83C51FC, in that it supports half-duplex serial communication, and has 8k Bytes of Mask programmable ROM. The device is available in a standard pinout DIP, with optional packages considered. These microcontrollers provide guaranteed performance supporting operating frequencies in excess of 16 MHz over the full -55 to +225ºC temperature range. Typically, parts will operate up to +300ºC for a year, with derated performance.

APPLICATIONS

Downhole Oil Well, Avionics, Turbine Engine Control, Industrial Process Control, Nuclear Reactor, Electric Power Conversion, and Heavy Duty Internal Combustion Engine

FEATURES

▶ Specified Over -55 to +225°C

▶ 8-bit CPU Optimized for 5 Volt Control Applications

▶ Four 8-bit Bidirectional Parallel Ports

▶ Three 16-bit Timer/Counters with One Up/Down Timer/Counter and Clock Out

▶ 64K External Data Memory Address Space

▶ MCS-51 Compatible Instructions Set

▶ Programmable Counter Array with:
Capture/Compare, Software Timer with Watchdog Capability, High Speed Output, and Pulse Width Modulator

▶ On-Chip Oscillator

▶ Interrupt Structure with Seven Sources and Four Priority Levels

▶ Half Duplex Programmable Serial Port with Framing Error Detection and Automatic Address Recognition

▶ 256 Bytes Internal Data Memory

▶ Hermetic 40-pin Ceramic Dip

▶ Parts burned in at 250ºC

HT83C51

FUNCTIONAL DIAGRAM

HT83C51
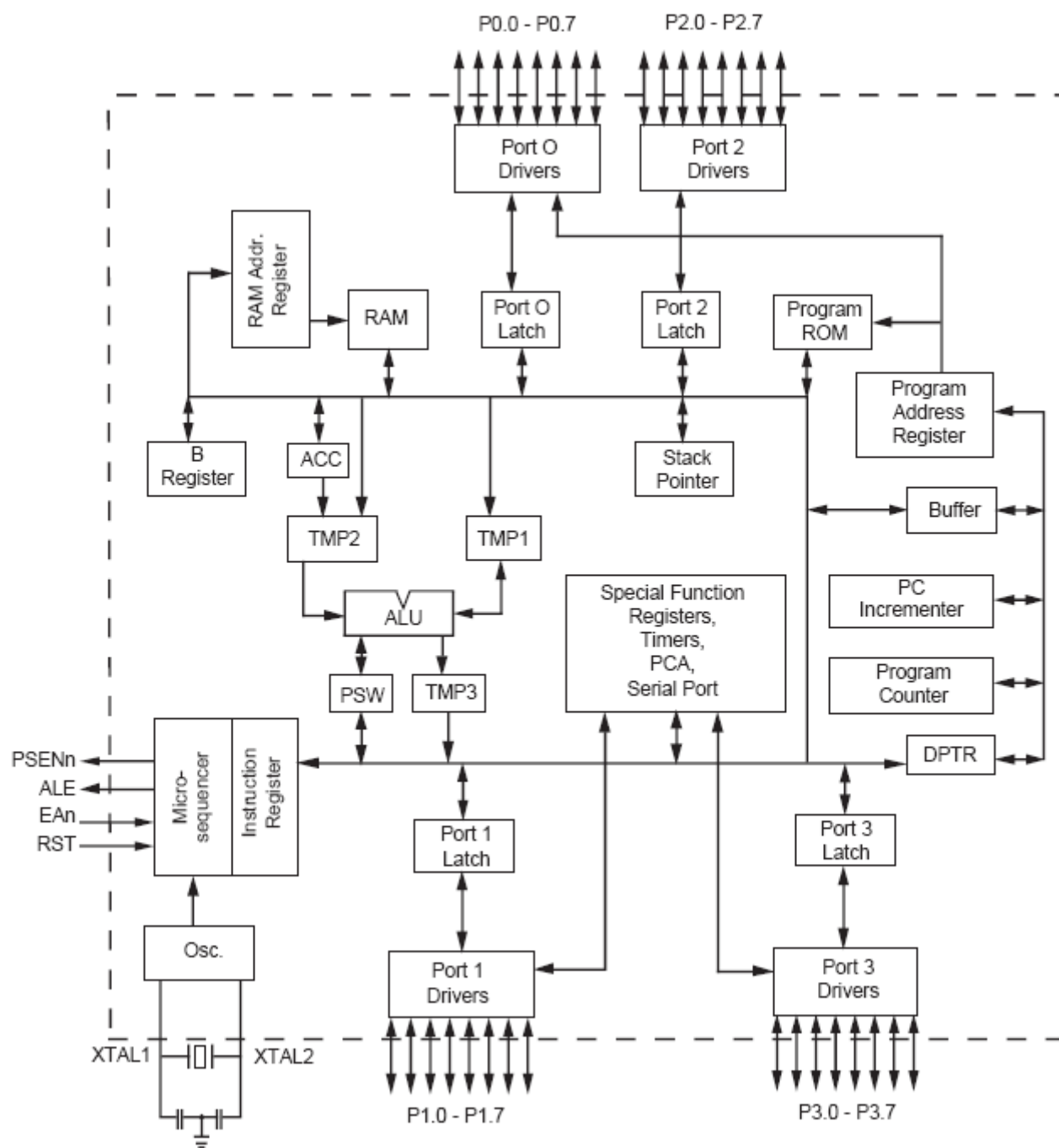
PIN DESCRIPTIONS

VDD: +5V Supply Voltage

VSS: Circuit Ground

Port 0 (P0.0 – P0.7): Port 0 is an 8-bit bidirectional I/O port. If external Program and/or Data memory are used, port 0 cannot be used for general purpose I/O. During accesses to external Program and Data memory Port 0 is used as the low-order multiplexed address and data bus. In this mode, Port 0 pins use strong internal pullups when emitting 1's, and are TTL compatible. IF external Program and Data memory are not used, Port 0 pins can be used as general purpose I/O. When the Port pins have 1's written to them in I/O mode, the pins are floating and can be driven as inputs. An external pullup is required to generate logic high output in I/O mode.

Port 1 (P1.0-P1.7): Port 1 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 1 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 1 pins have the alternate uses shown in the table below:

Port Pin	Name	Alternate Function
P3.0	RXD	Serial port input
P3.1	TXD	Serial port output
P3.2	INT0n	External interrupt 0
P3.3	INT1n	External interrupt 1
P3.4	T0	External clock input for Timer 0
P3.5	T1	External clock input for Timer 1
P3.6	WRn	External Data Memory write strobe
P3.7	RDn	External Data Memory read strobe

Port 2 (P2.0-P2.7): Port 2 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 2 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups.

Port 2 is used as the high-order address byte during accesses to external Porgram Memory and during accesses to external Data Memeory that use

16-bit addressess (i.e. MOVX @DPTR). It uses strong internal pullups when emitting 1's in this mode. During accesses to external Data Memory that use 8 bit addresses, Port 2 emits the contents of the P2 SFR.

Port 3 (P3.0-P3.7): Port 3 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 3 pins have 1's written to them, they are pulled high by the internal pullpus and canb euses as iputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 3 pins have the alternate uses shown in the table below:

Port Pin	Name	Alternate Function
P1.0	T2	External clock input to timer/clock out
P1.1	T2EX	Timer/Counter 2 Capture/Reload trigger and direction control
P1.2	ECI	External count input to PCA
P1.3	CEX0	External I/O for PCA capture/compare Module 0
P1.4	CEX1	External I/O for PCA capture/compare Module 1
P1.5	CEX2	External I/O for PCA capture/compare Module 2
P1.6	CEX3	External I/O for PCA capture/compare Module 3
P1.7	CEX4	External I/O for PCA capture/compare Module 4

RST: Reset input. A high on this input for 2 or more oscillator periods while the oscillatoris running resets the device. All ports and Special Function Registers will be reset to their default conditions. Internal data memory is undefined after reset. Program execution will begin within 12 oscillator periods (one machine cycle) after the RST signal is brought low. RST contains an internal pulldown resistor to allow implementing power-up reset with only an external capacitor.

ALE: Address Latch Enable. The ALE output is a pulse for latching the low byte of the address during accesses to output every 6th oscillator cycle and may be used for external timing or clocking. However, during each access to external Data Memory (MOVX instruction), one ALE pulse is skipped. If desired, ALE operation can be disabled by setting bit 0 of SFR 8EH. When this bit is set, ALE is active only during a MOVX instruction. Otherwise, the pin is held low. When ALE is disabled, program execution must be limited to the internal 8K program ROM.

PSENn: Program Store Enable. This active low signal is the read strobe to the external program memory. PSENn is activated every 6th oscillator cycle except that 2 PSENn activiations are skipped during external data memory accesses.

EAn: External Access Enable. The EAn pin must be strapped to VSS for the HT51 to fetch code from external Program Memory locations 0000H to 1FFFH. The HT83C51 does not contain on-chip program memory. If the EAn pin is held high then code fetched from mrmory locations 0000H to 1FFFH will return all zeroes.

XTAL 1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

The input is XTAL1 and the output is XTAL2 for an inverting amplifier which can be used as an on-chip oscillator as shown in Figure 1. Make sure to qualify the crystal or alternate timing source over the temperature range of the intended application. If an external clock source such as the HTOSC is used , XTAL1 should be driven whil XTAL2 floats as shown in Figure 2. There are no duty cycle requirements on the external clock signal, but minimum and maximum high and low times must be observed
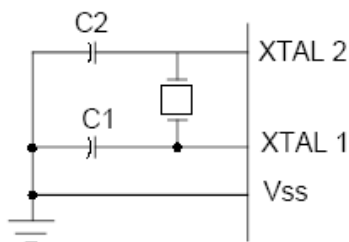

For C1 and C2 values,
contact crystal manufacturer
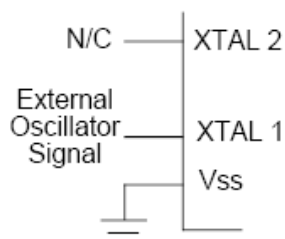
Figure 1. Oscillator Connections

Figure 2. External Clock Drive Configuration

IDLE MODE

An instruction that sets the PCON. 0-bit causes that to be the last instruction executed prior to going into Idle mode. In the Idle mode, the internal clock to the CPU is gated off but not to the Interrupt, Timer, and Serial Port functions. The PCA can be programmed to either pause or continue operating during Idle Mode. The CPU status is completely preserved and all registers maintain their previous values during Idle Mode. The port pins hold the logical vlaues that they had at the time the Idel mode was activated. ALE and PSENn hold at logic high levels.

Idle mode can be terminated in two ways. Activiation of any enabled interrupt will cause te PCON. 0-bit to be cleared by hardware, terminating Idle mode. The interrupt will be serviced, and following the RETI instruction execution, the instruction after the one that caused Idle mode will be executed. Recovery from Idle mode is 3 oscillator periods plus 3 instruction cycles.

The other way that Idle mode can be terminated is through a hardware reset, which ca be accomplished by holding the RST pin high for 4 clock periods while the clock is running. Exiting Idle mode with a hardware reset will retain the contents of the on-chip RAM but the values in the SRFs will be lost and program execution will begin at address 0.

MEMORY

The HT51 has a separate address space for Program and Data Memory. Internally the HT51 contains 256 bytes of Data Memory. It can address up to 64 Kbytes of external Data Memory and 64 Kbytes of external Program Memory. All program memory is internal.

The EAn pin must be tied to Vss (ground) to enable access to external program memory. When the EAn pin is tied to Vdd, program fetches to addresses 0000H and 1FFFH will return all zeroes. The EAn pin must be tied to Vss (ground) to enable access to external program memory locations 0000H through 1FFFH.

HT83C51

The HT51 implements 256 bytes of internal data RAM. The upper 128 bytes of this RAM occupy a parallel address space to the Special Function Registers (SFR's). The CPU determines if the internal access to an address above 7FH is to the upper 128 bytes of RAM or to the SFR space by the addressing mode of the instruction. If direct addressing is used, the access is to the SFR space. If indirect addressing is used, the acess is to the internal RAM. Stack operations are indirectly addressed so the upper portion of RAM can be used as stack space.

TIMER/COUNTERS

The HT51 contains three 16-bit timer/counters. Each of these are made up to two 8-bit registers (THx, TLx where x=0, 1, or 2). Each of these three can operate in either timer or counter mode. In the timer mode, the TLx register is incremented once every machine cycle (12 oscillator periods). The count rate is $1/12^{th}$ of the oscillator frequency. In counter mode, the register is incremented when a 1 to 0 transition is detected on the alternate function input corresponding to that timer (Tx where x=0, 1, or 2). The maximum rate of count in counter mode that the HT51 can detect is $1/24^{th}$ of the oscillator frequency.

PCA COUNTER/TIMER

The Programmable Counter Array (PCA) contains a single 16-bit counter/timer made up of the CL and CH registers. This timer is used by all 5 capture/compare modules. Its clock input can be programmed to be from one of four sources. These are the oscillator frequency divided by 12, the oscillator frequency divided by 4, Timer 0 overfllow, and an external clock input, ECI, on the alternate function of port pin P1.2.

SERIAL PORT

The serial port has physically separate receive and transmit buffers, automoatic address recognition and four modes of operation as shown below.

Mode	Description	Baud Rate
0	8-bit shift register	1/12 times oscillator freq.
1	8-bit UART	Variable
2	9-bit UART	1/64 or 1/32 times oscillator freq.
3	9-bit UART	variable

INTERRUPTS

There are seven interrupt sources in the HT51. Two are external interrupts (INT0n, INT1n), three are timer interrupts (Timer 0, Timer 1, and Timer 2), one is a PCA interrupt, and one is a serial port interrupt as shown below.

PCA interrupt enable

Timer 2 interrupt enable

Serial port interrupt enable

Timer 1 interrupt enable

External interrupt 1 enable

Timer 0 interrupt enable

External interrupt 0 enable

RESET

The reset input is the RST pin. A reset is accomplished by holding the RST pin high for a minimum of 4 clock periods while the clock is running. The CPU generates an internal reset from the external signal. The port pins are driven to the reset state 2 oscillator periods after a valid 1 is detected on the RST pin.

While RST is high, PSENn is pulled high, ALE is pulled low, and the port pins are pulled weakly high. All SFRs are reset to their reset values. The internal Data Memory content is not affected by reset. In addition, if the HT51 is in Idle or Power Down mode prior to activation of RST, the HT51 will be taken out of Idle or Power Down mode by the reset.

The processor will begin operation on the second machine cycle after the RST line is brought low. A memory access will be made immediately after the RST line is brought low, but the data is not brought into the processor. The memory access will be repeated on the next machine cycle and actual processing will begin at that time.

INSTRUCTION SET

The instruction set for the HT51 is compatible to the Intel MCS-51 instruction set used on the 8XC51FC.

AC CHARACTERISTICS

The AC characteristics for the HT51 are shown in the following tables. Each of the timing symbols has 5 characters. The first character is always a 'T' (Time). The other characters, depending on their positions, stand for the logical name of a signal or the logical status of that signal. The following is a list of the characters and what they stand for:

A: Address

Q: Output Data

C: Clock

R: RDn Signal

D: Data

T: Time

H: Logic Level HIGH

V: Valid

I: Instruction (program memory contents)

W: WRn Signal

L: Logic level LOW, or ALE level

X: No longer a valid logic

P: PSENn

Z: Float

For example, TAVLL = Time from address valid to ALE low. The characteristics given are over the operating conditions T_A=-55ºC to +225ºC, V_{DD}=5V±10%, V_{SS} = 0V. The load capacitance on Port 0, ALE and PSENn=100 pF. Load capacitance for all other outpus =50 pF. Inputs during AC testing are to be driven at V_{DD} – 0.5V for logic 1 and 0.45 V for logic 0. Timing measurements are to be made at V_{IH} min for logic 1 and V_{IL} max for logic 0. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OL}/V_{OH} level occurs. Timing diagrams are shown to illustrate the signal relationships depicted in the tables.

HT83C51

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Conditions [3]
VIL	Input Low Voltage	VSS-0.3	0.8		
VIH	Input High Voltage (except XTAL1, RST)	2.0	VDD+0.5	V	
VIH1	Input High Voltage (XTAL1, RST)	3.85	VDD+0.5	V	
VOL	Output Low Voltage [1,2] (Ports 1,2, and 3)		0.3	V	IOL=100µA
			0.45	V	IOL=1.6µA
			1.0	V	IOL=3.5µA
VOL1	Output Low Voltage [1,2] (Ports 0, ALE, PSENn)		0.3	V	IOL=200 µA
			0.45	V	IOL=3.2µA
			1.0	V	IOL=7.0µA
VOH	Output High Voltage (Ports 1,2, and 3, ALE, PSENn)	4.2		V	IOH=-10 µA
		3.8		V	IOH=-30 µA
		3.0		V	IOH=-60 µA
VOH1	Output High Voltage (Ports 0)	4.2		V	IOH=-200 µA
		3.8		V	IOH=-3.2 µA
		3.0		V	IOH=-7.0 µA
IIL	Logical 0 Input Current (Ports 1,2, and 3)		-50	µA	VIN = 0.45 V
ILI	Input Leakage Current (Port 0)		±10	µA	0.45 V < Vin < VDD
ITL	Logical 1 to 0 Transition Current (Ports 1,2, and 3)		-650	µA	VIN = 2V
RRST	RST Pulldown Resistor	10	225	KW	
CIO	Pin Capacintance		10 typical	pF	@1 MHz, 25ºC
IDD	Power Supply Current: Operating		70	mA	16 MHz
	Idle		15	mA	16MHz

(1) Under steady state (non-transient conditions, IOL must be limited externally as follows:

    Maximum IOL per port pin   10mA

    Maximum IOL per 8-bit port

       -port 0   26mA

       -port 1,2,3   15mA

    Maximum total IOL for all output pins   71mA

(2) If OIL exceeds the test conditions, VOL may exceed the related specifications.

(3) Pins are not guaranteed to sink current greater than the listed test conditions.

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage, V_{DD} to V_{SS} .... -0.5 to 7.0 V

Voltage On Any Pin to V_{SS} .... -.05 V to VDD + 0.3V

Power Dissipation .... 750 mW

Storage Temperature .... -65 to +325ºC

IOL per Output Pin .... 15 mA

EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

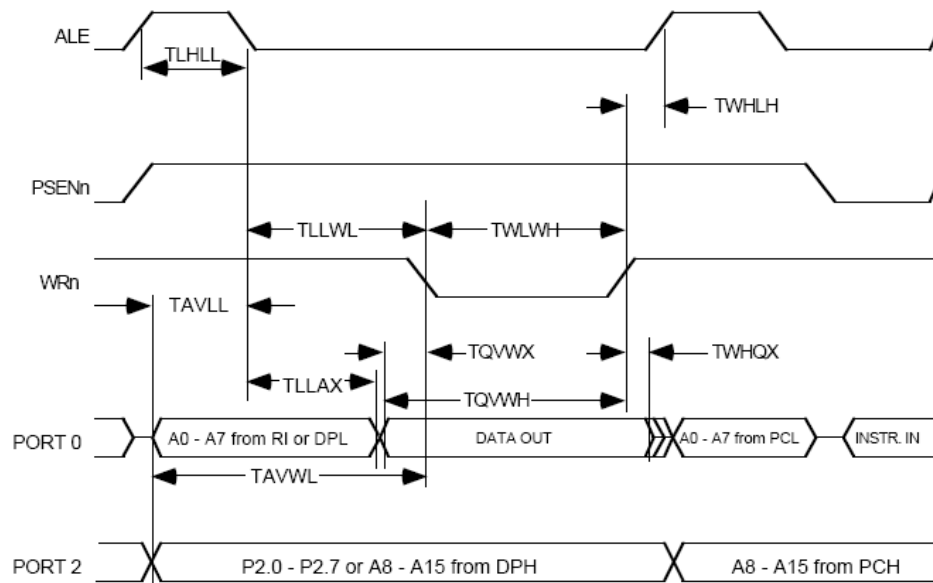| Symbol	Parameter	Min	Max	Unit
TCLCL	Clock Period	62.5		ns
1/TCLCL	Oscillator Frequency		16	MHz
TLHLL	ALE Pulse Width	2 TCLCL-40		ns
TAVLL	Address Valid to ALE Low	TCLCL-40		ns
TLLAX	Address hold after ALE Low	TCLCL-30		ns
TLLIV	ALE low to Valid Instruction In		4 TCLCL-100	ns
TLLPL	ALE Low to PSENn Low	TCLCL-30		ns
TPLPH	PSENn Pulse Width	3 TCLCL-45		ns
TPLIV	PSENn low to Valid Instruction In		3 TCLCL-105	ns
TPXIX	Input Instruction hold after PSENn	0		ns
TPXIZ	Input Instruction Float After PSENn		TCLCL-25	ns
TPVIV	Address to Valid Instruction In		5 TCLCL-105	ns
TPLAZ	PSENn Low to Address Float		10	ns
TRLRH	RDn Pulse Width	6 TCLCL-100		ns
TWLWH	WRn Pulse Width	6 TCLCL-100		ns
TRLDV	RDn Low to Valid Data In		5 TCLCL-165	ns
TRHDX	Data Hold After RDn	0		ns
TRHDZ	Data Float After RDn		2 TCLCL-60	ns
TLLDV	ALE Low to Valid Data In		8 TCLCL-150	ns
TAVDV	Address to Valid Data In		9 TCLCL-165	ns
TLLWL	ALE Low to RDn or WRn Low	3 TCLCL-50	3 TCLCL+50	ns
TAVWL	Address Valid to WRn Low	4 TCLCL-130		ns
TQVWX	Data Valid Before WRn	TCLCL-50		ns
TWHQX	Data Hold After WRn	TCLCL-50		ns
TQVWH	Data Valid to WRn High	7 TCLCL-150		ns
TRLAZ	RDn Low to Address Float		0	ns
TWHLH	RDn or WRn High to ALE High	TCLCL-40	TCLCL+40	ns

HT83C51

EXTERNAL PROGRAM MEMORY READ CYCLE
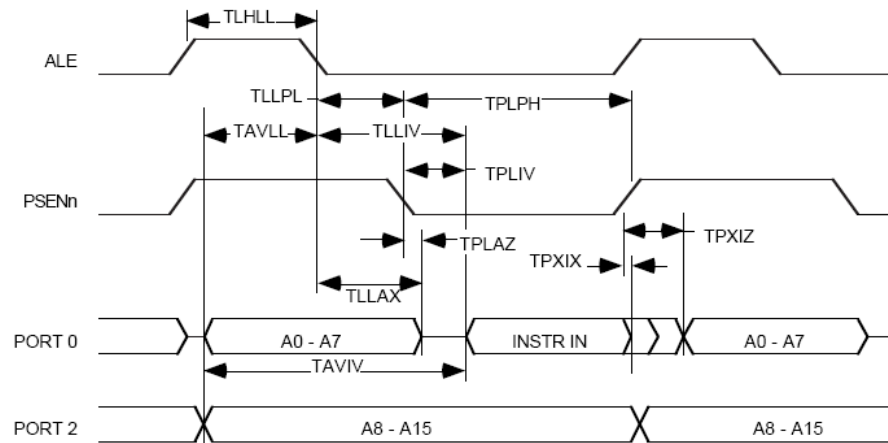

EXTERNAL DATA MEMORY READ CYCLE
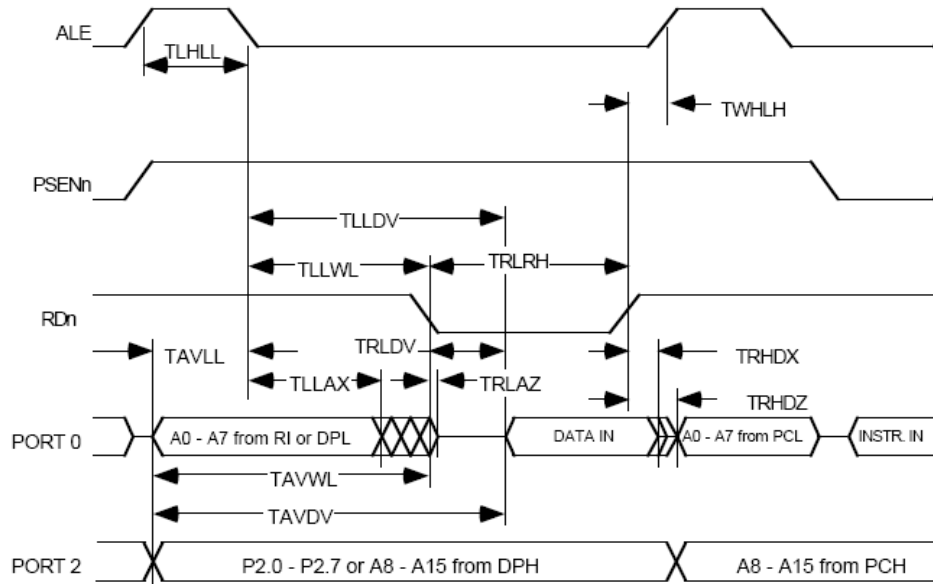

EXTERNAL DATA MEMORY WRITE CYCLE

HT83C51

SERIAL PORT TIMING CHARACTERISTICS – SHIFT REGISTER MODE (MODE 0)

| Symbol	Parameter	16 MHz Oscillator		Variable Oscillator		Unit
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Period	750		12 TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	492		10 TCLCL-133		ns
TXHQX	Output Data Hold after Clock Rising Edge	8		2 TCLCL-117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		492		10 TCLCL-133	ns

SERIAL PORT TIMING WAVEFORMS
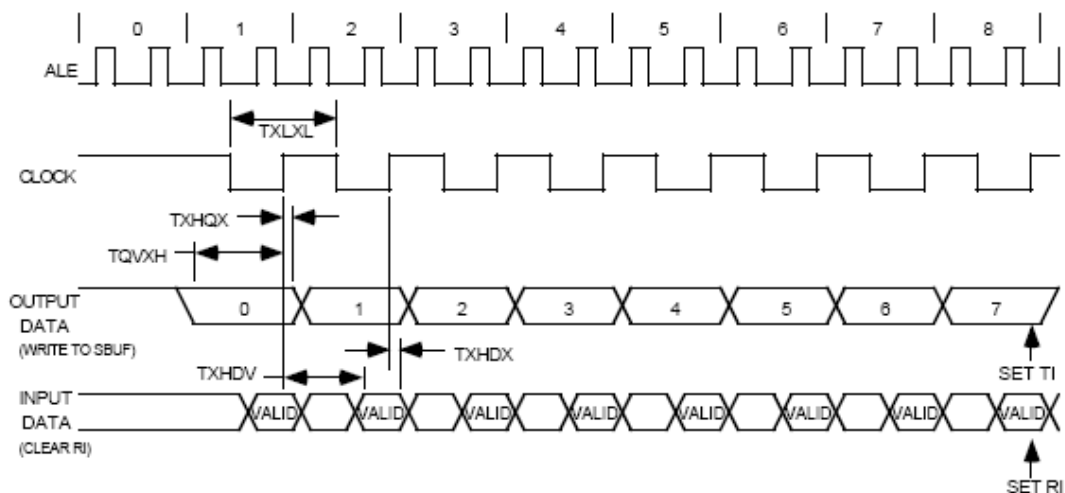
PERFORMANCE CURVES OVER TEMPERATURE
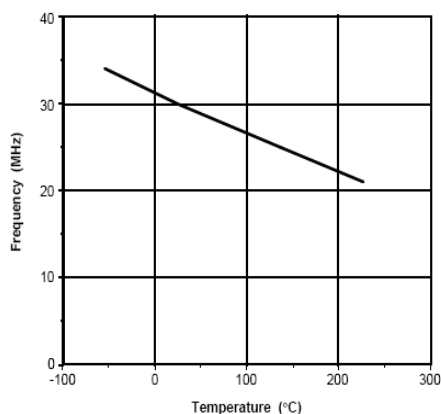
Maximum frequency vs. temperature
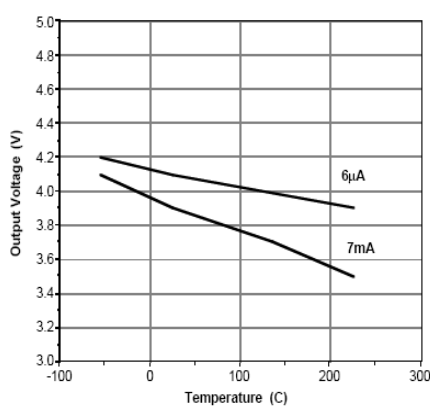
Output drive vs. temperature
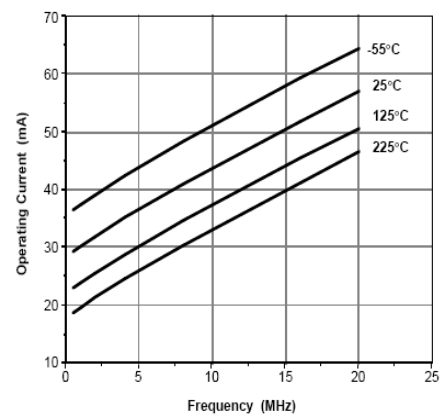
Operating current vs. frequency vs. temperature

HT83C51

DIFFERENCE BETWEEN INTEL 8XC51FC AND HT83C51

There are a few areas in which the HT51 differs from the 8XC51FC. These differences will be covered in this appendix. In this discussion, 8XC51FC will be used generically to refer to all speed grades of the Intel 8XC51FC family, including the 16MHz 8XC51FC-1.

1. Reset

The 8XC51FC requires the RST input to be held high for at least 24 oscillator periods to guarantee the reset is completed in the chip. Also, the port pins are reset asynchronously as soon as the RST pins is pulled high. On the HT51, all portions of the chip are reset synchronously when the RST pin has been high during 2 rising edges of the input clock.

When coming out of reset, the 8XC51FC takes 1 to 2 machine cycles to begin driving ALE and PSENn. The HT51 will begin driving ALE and PSENn2 oscillator periods after the RST is removed but the access during the first machine cycle after reset is ignored by the processor. The second cycle will repeat the access and processing will begin.

2. Power Off Flag

The Power Off Flag in the PCON register has not been implemented in the HT51.

3. On Circuit Emulation

The On Circuit Emulation mode of operation in the 8XC51FC has not been implemented in the HT51.

4. Operating Conditions

The operating voltage range for the 8XC51FC is 5V ± 20%. The operating temperature range is 0º to 70ºC. On the HT51, the operating voltage range is 5V ± 10%. The full speed operating temperature rnage is -55ºC to +225ºC; typically, parts will operate up to +300ºC for a year, with derated performance.

5. DC Characteristics

VIL min for the 8XC51FC is -0.5V for all inputs except EAn which has a VIL min of 0V. The HT51 has a VIL min for all inputs of Vss-0.3V.
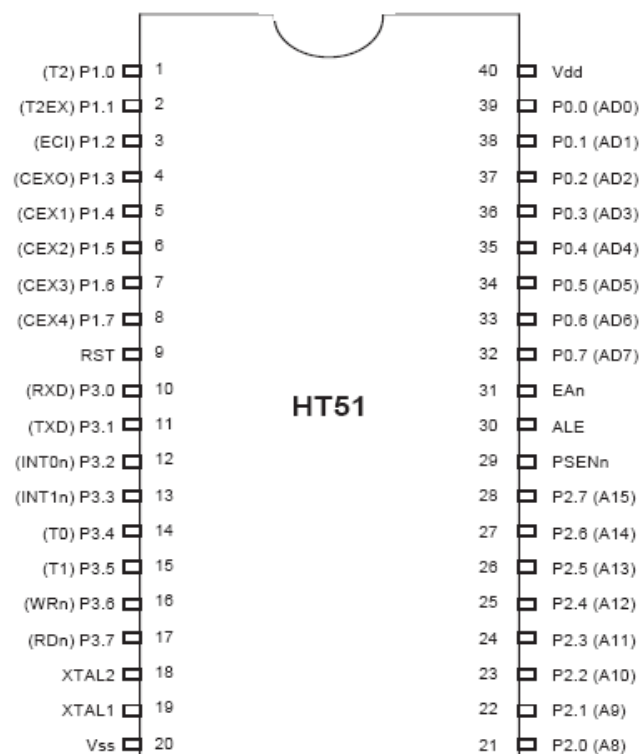
6. Internal Program Memory

The 8XC51FC contains 32 Kbytes of internal program ROM (8XC51FC) or EPROM (87C51FC). The HT51 contains 8 Kbytes of internal program ROM.

7. Serial Communications

There is a chance the part will miss hardware interrupts when performing full-duplex (simultaneous send and receive) communication or when using the capture or compare modes in the Programmable Counter Array (PCA).
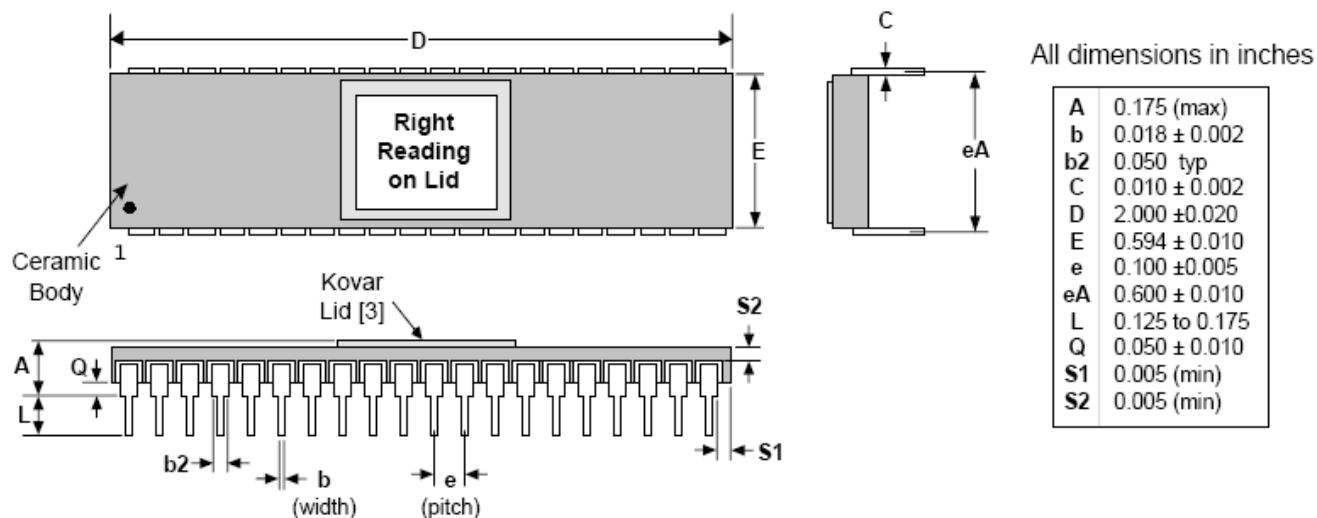
As a result, the HT83C51 supports half-duplex operation. Full duplex operation is not supported without additional external hardware. Several acceptable work-around procedures have been identified for the problem associated with the PCA.

PINOUT DIAGRAM
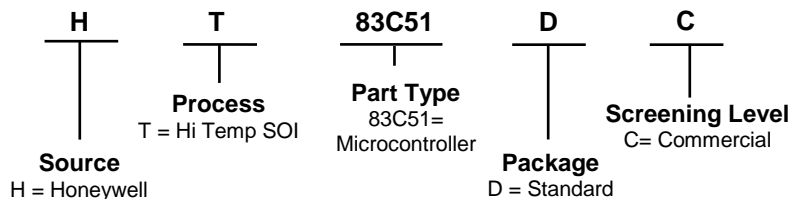
HT83C51

40-LEAD PACKAGE DETAIL

All dimensions in inches

A	0.175 (max)
b	0.018 ± 0.002
b2	0.050 typ
C	0.010 ± 0.002
D	2.000 ±0.020
E	0.594 ± 0.010
e	0.100 ±0.005
eA	0.600 ± 0.010
L	0.125 to 0.175
Q	0.050 ± 0.010
S1	0.005 (min)
S2	0.005 (min)

THERMAL CHARACTERISTICS
Assumes Static Air Convection
Θjc..................0.9ºC/W
Θjc..................32.8ºC/W

ORDERING INFORMATION

H   T   83C51   D   C

Source
H = Honeywell

Process
T = Hi Temp SOI

Part Type
83C51=
Microcontroller

Package
D = Standard

Screening Level
C= Commercial

Find out more

For more information on Honeywell's High Temperature Electronics visit us online at www.hightempsolutions.com or contact us at 1-800-323-8295. Customer Service Email: ps.customer.support@honeywell.com.

Honeywell