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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg330f1024-qfn64

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32GG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32GG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32GG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32GG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Universal Serial Bus Controller (USB)

The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated

available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.26 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32GG330 to keep track of time and retain data, even if the main power source should drain out.

2.1.27 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.28 General Purpose Input/Output (GPIO)

In the EFM32GG330, there are 52 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

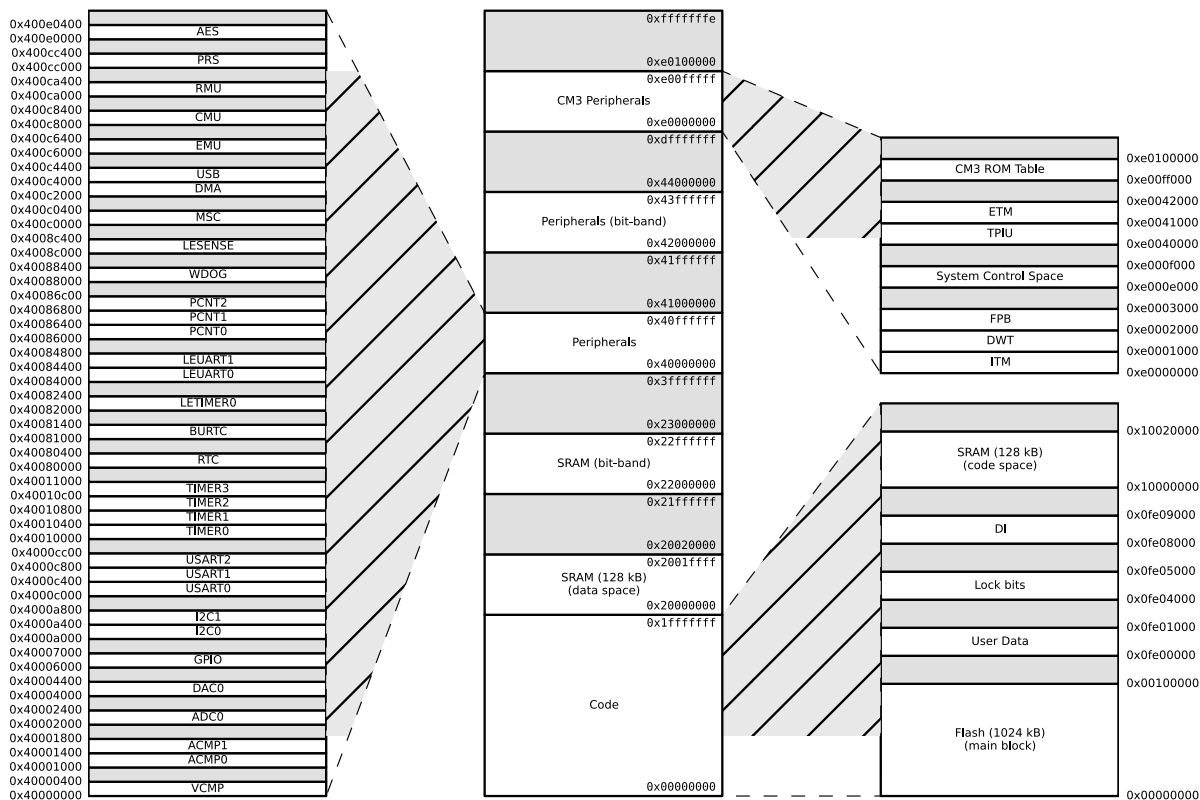
2.2 Configuration Summary

The features of the EFM32GG330 is a subset of the feature set described in the EFM32GG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID

Figure 2.2. EFM32GG330 Memory Map with largest RAM and Flash sizes

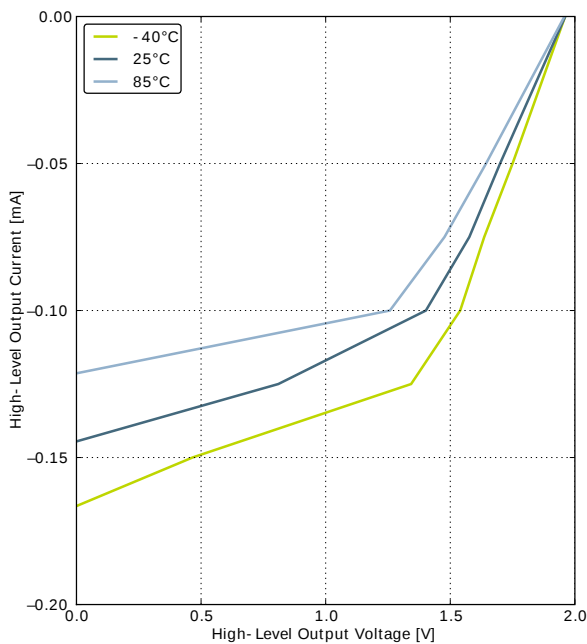


3.4 Current Consumption

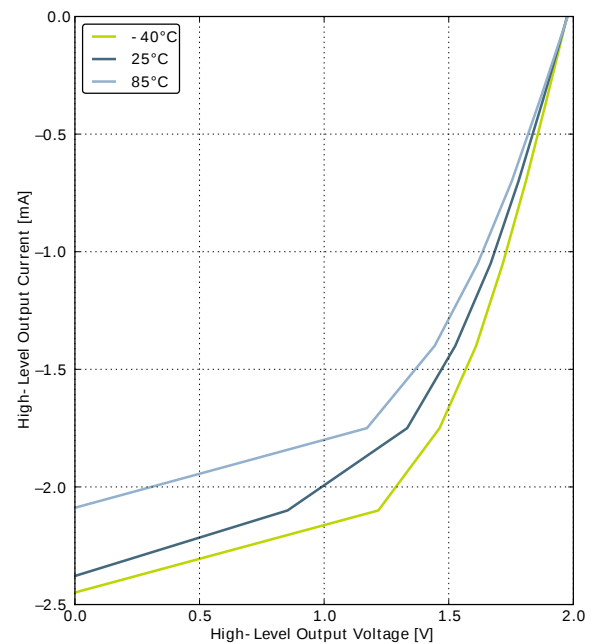
Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from flash. (Production test condition = 14MHz)	48 MHz HFXO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		219	240	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		205	225	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		206	229	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		209	232	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		211	234	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		215	242	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		243	327	$\mu\text{A}/\text{MHz}$
I_{EM1}	EM1 current (Production test condition = 14MHz)	48 MHz HFXO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		80	90	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		80	90	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		81	91	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		83	99	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		85	100	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		90	102	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$		122	152	$\mu\text{A}/\text{MHz}$
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}= 3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		1.1 ¹	1.9 ¹	μA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}= 3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		8.8 ¹	21.5 ¹	μA
I_{EM3}	EM3 current	$V_{DD}= 3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.8 ¹	1.5 ¹	μA
		$V_{DD}= 3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		8.2 ¹	20.3 ¹	μA
I_{EM4}	EM4 current	$V_{DD}= 3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.02	0.08	μA
		$V_{DD}= 3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		0.5	2.5	μA

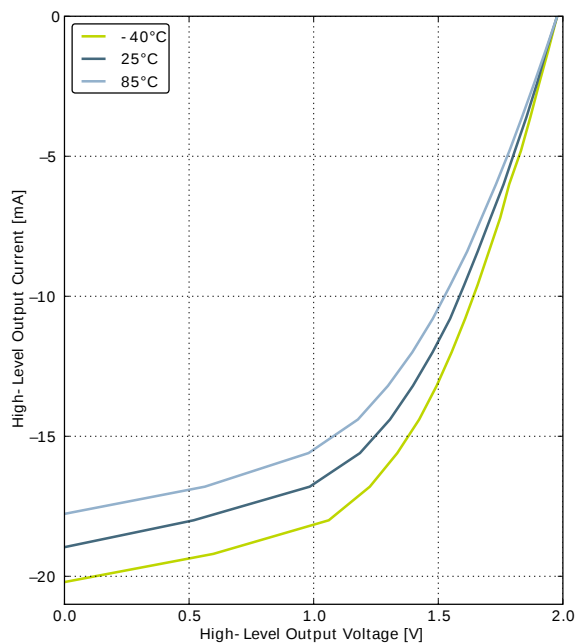
¹ Only one RAM block enabled. The RAM block size is 32 kB.

Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage

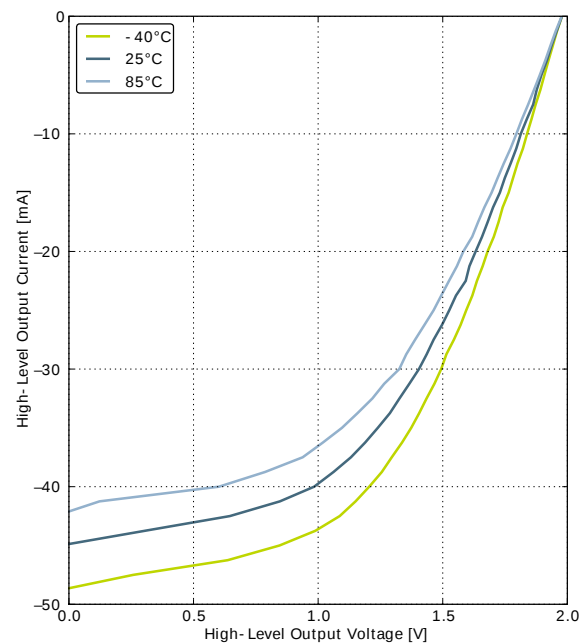
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{HFRCO}	Current consumption (Production test condition = 14MHz)	$f_{\text{HFRCO}} = 28 \text{ MHz}$		165	190	μA
		$f_{\text{HFRCO}} = 21 \text{ MHz}$		134	155	μA
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		106	120	μA
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		94	110	μA
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		77	90	μA
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		25	32	μA
$\text{TUNESTEP}_{\text{HFRCO}}$	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

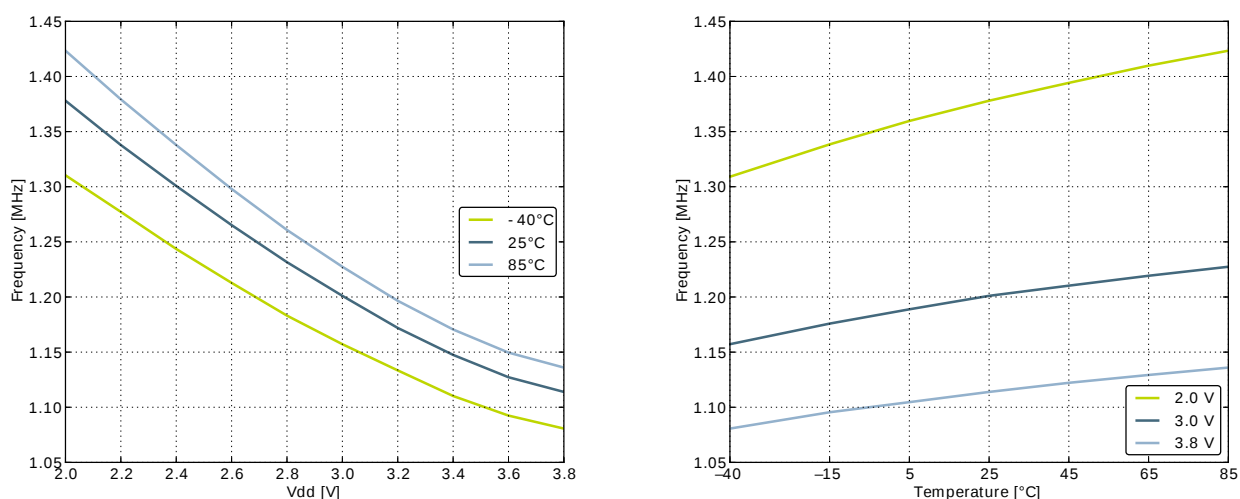


Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

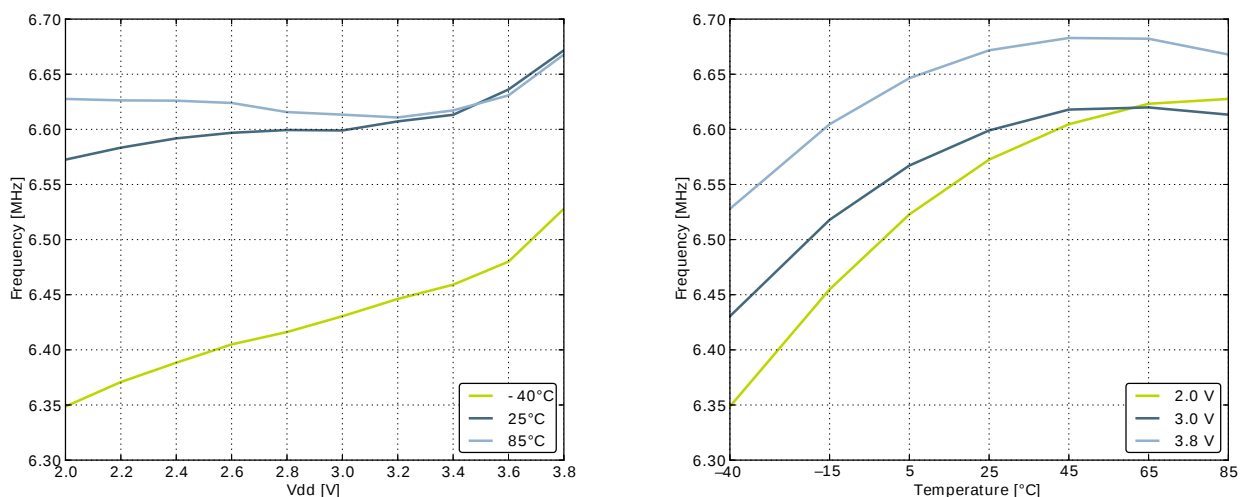


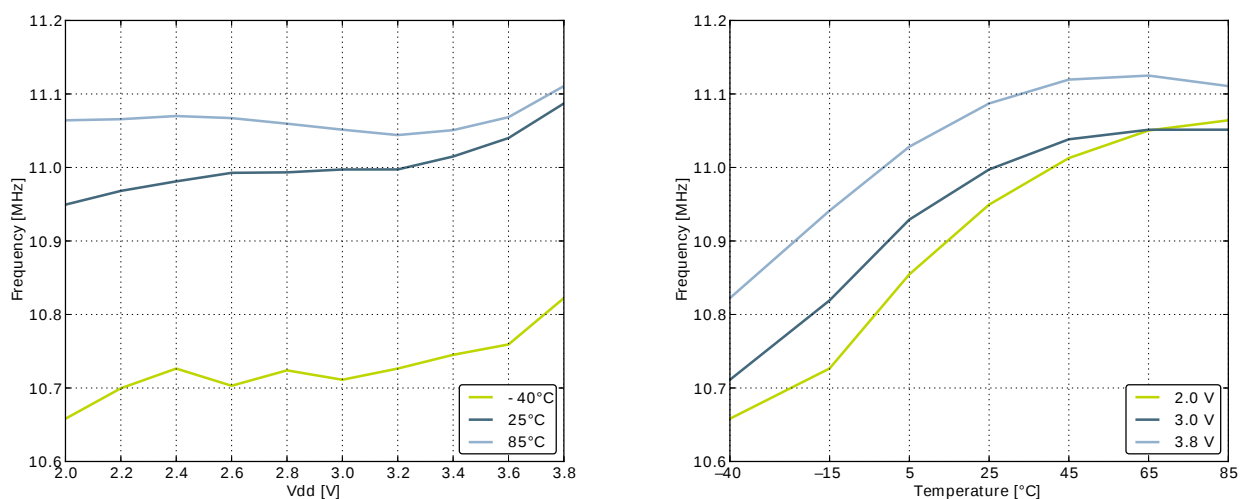
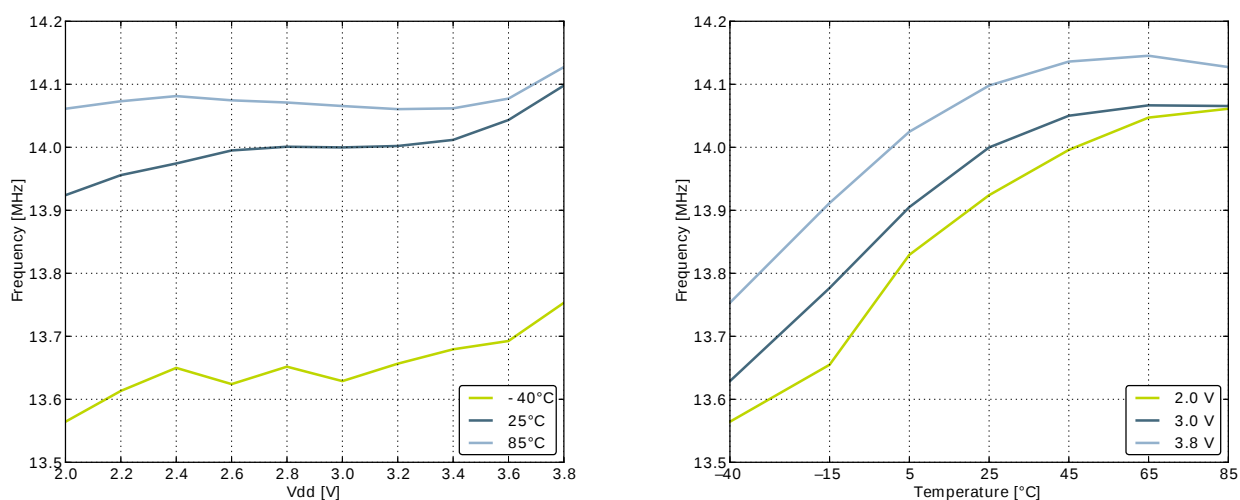
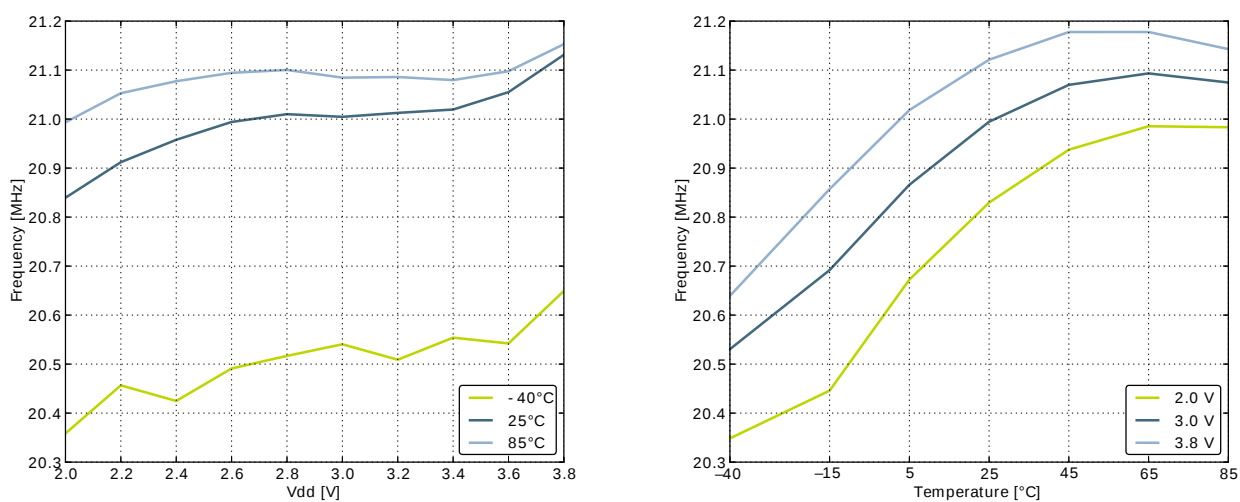
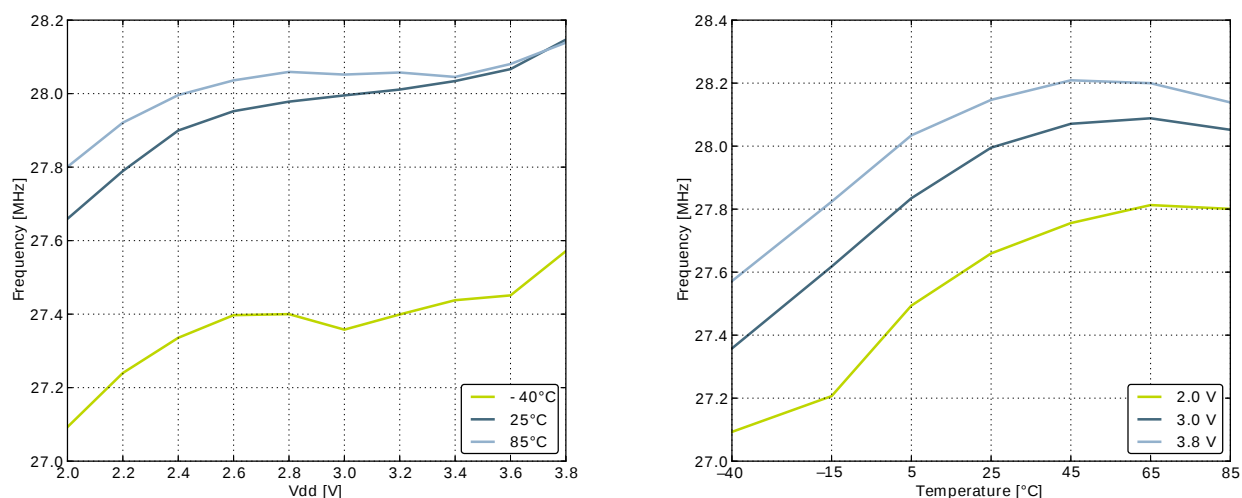
Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature**

Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature

3.9.5 AUXHFRCO

Table 3.12. AUXHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{AUXHFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48 ¹	6.60 ¹	6.72 ¹	MHz
		1 MHz frequency band	1.15 ²	1.20 ²	1.25 ²	MHz
$t_{\text{AUXHFRCO_settling}}$	Settling time after start-up	$f_{\text{AUXHFRCO}} = 14 \text{ MHz}$		0.6		Cycles
$\text{DC}_{\text{AUXHFRCO}}$	Duty cycle	$f_{\text{AUXHFRCO}} = 14 \text{ MHz}$	48.5	50	51	%
$\text{TUNESTEP}_{\text{AUXHFRCO}}$	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
GAIN _{ED}	Gain error drift	1.25V reference		0.01 ²	0.033 ³	%/°C
		2.5V reference		0.01 ²	0.03 ³	%/°C
OFFSET _{ED}	Offset error drift	1.25V reference		0.2 ²	0.7 ³	LSB/°C
		2.5V reference		0.2 ²	0.62 ³	LSB/°C

¹On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.

³Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 32) and Figure 3.18 (p. 33), respectively.

Figure 3.17. Integral Non-Linearity (INL)

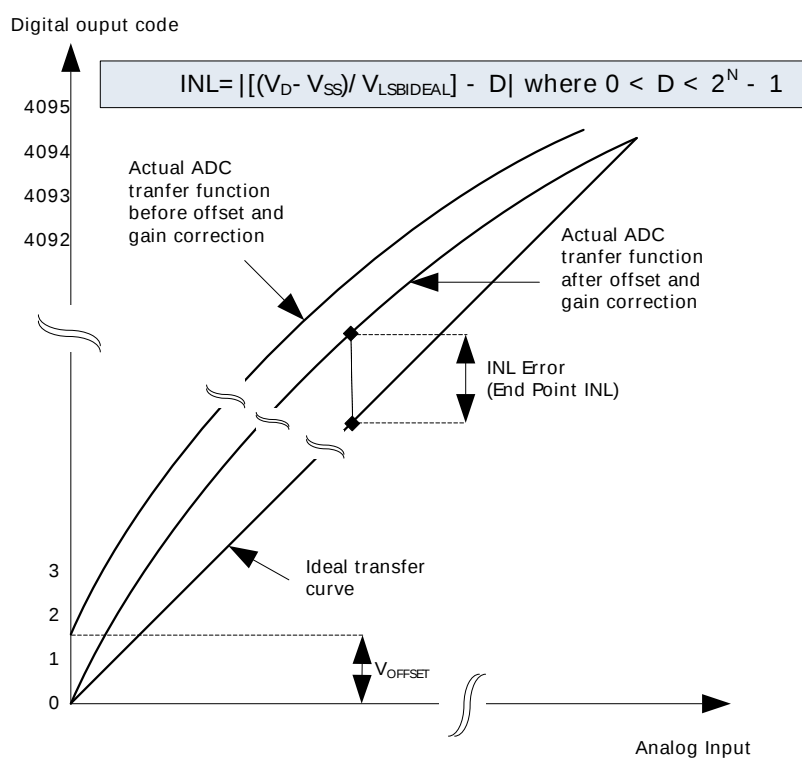


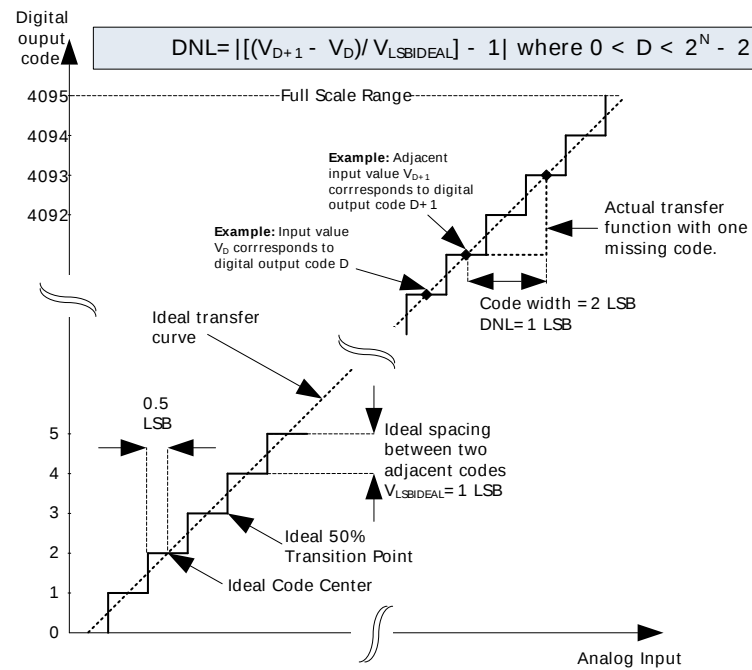
Figure 3.18. Differential Non-Linearity (DNL)

Figure 3.22. ADC Absolute Offset, Common Mode = Vdd /2

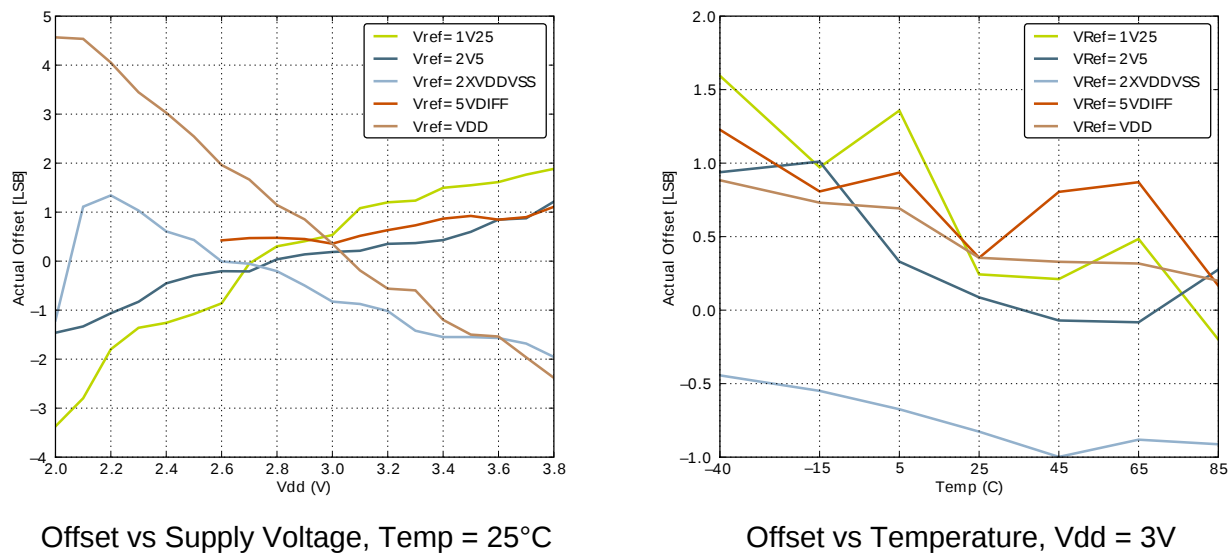
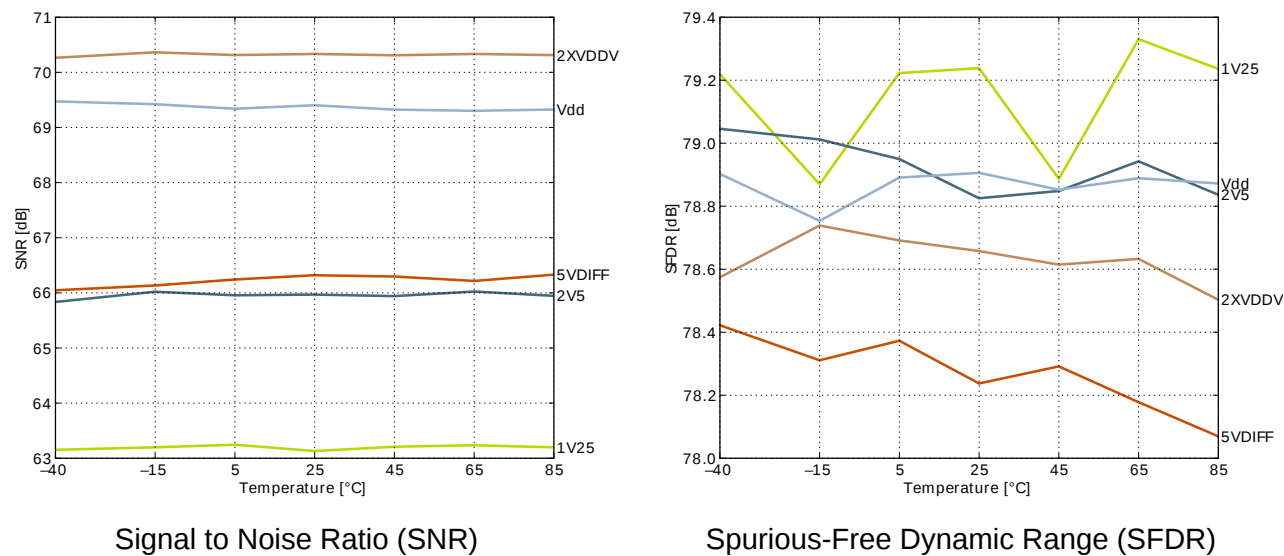


Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



3.13 Analog Comparator (ACMP)

Table 3.17. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.6	μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	12	μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		250	520	μA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		μA
		Internal voltage reference		5		μA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		43		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		78		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		111		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		145		kOhm
$t_{ACMPSTART}$	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 43) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

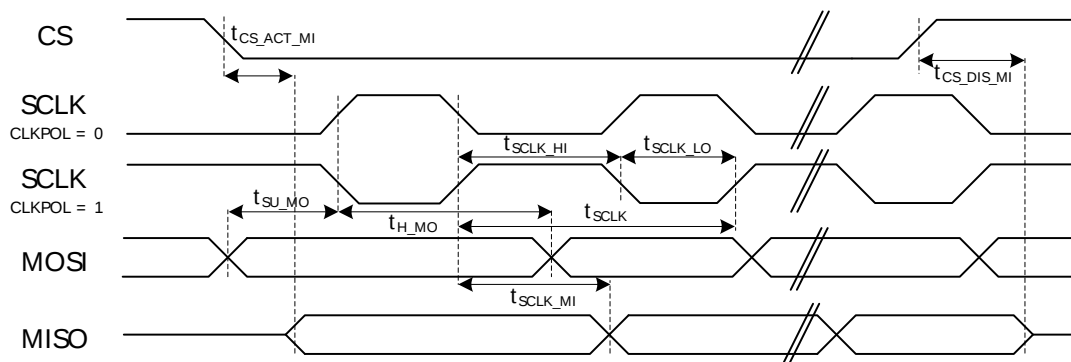
$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

Table 3.22. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{SCLK}}^{1,2}$	SCLK period		$2 * t_{\text{HFER-CLK}}$			ns
$t_{\text{CS_MO}}^{1,2}$	CS to MOSI		-2.00		1.00	ns
$t_{\text{SCLK_MO}}^{1,2}$	SCLK to MOSI		-4.00		3.00	ns
$t_{\text{SU_MI}}^{1,2}$	MISO setup time	IOVDD = 1.98 V	36.00			ns
		IOVDD = 3.0 V	29.00			ns
$t_{\text{H_MI}}^{1,2}$	MISO hold time		-4.00			ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Figure 3.32. SPI Slave Timing**Table 3.23. SPI Slave Timing**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{SCLK_sl}}^{1,2}$	SCKL period	$2 * t_{\text{HFER-CLK}}$			ns
$t_{\text{SCLK_hi}}^{1,2}$	SCLK high period	$3 * t_{\text{HFER-CLK}}$			ns
$t_{\text{SCLK_lo}}^{1,2}$	SCLK low period	$3 * t_{\text{HFER-CLK}}$			ns
$t_{\text{CS_ACT_MI}}^{1,2}$	CS active to MISO	4.00		30.00	ns
$t_{\text{CS_DIS_MI}}^{1,2}$	CS disable to MISO	4.00		30.00	ns
$t_{\text{SU_MO}}^{1,2}$	MOSI setup time	4.00			ns
$t_{\text{H_MO}}^{1,2}$	MOSI hold time	$2 + 2 * t_{\text{HFER-CLK}}$			ns
$t_{\text{SCLK_MI}}^{1,2}$	SCLK to MISO	$9 + t_{\text{HFER-CLK}}$		$36 + 2 * t_{\text{HFER-CLK}}$	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

3.17 USB

The USB hardware in the EFM32GG330 passes all tests for USB 2.0 Full Speed certification. See the test-report distributed with application note "AN0046 - USB Hardware Design Guide".

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32GG330.

4.1 Pinout

The EFM32GG330 pinout is shown in Figure 4.1 (p. 49) and Table 4.1 (p. 49). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32GG330 Pinout (top view, not to scale)

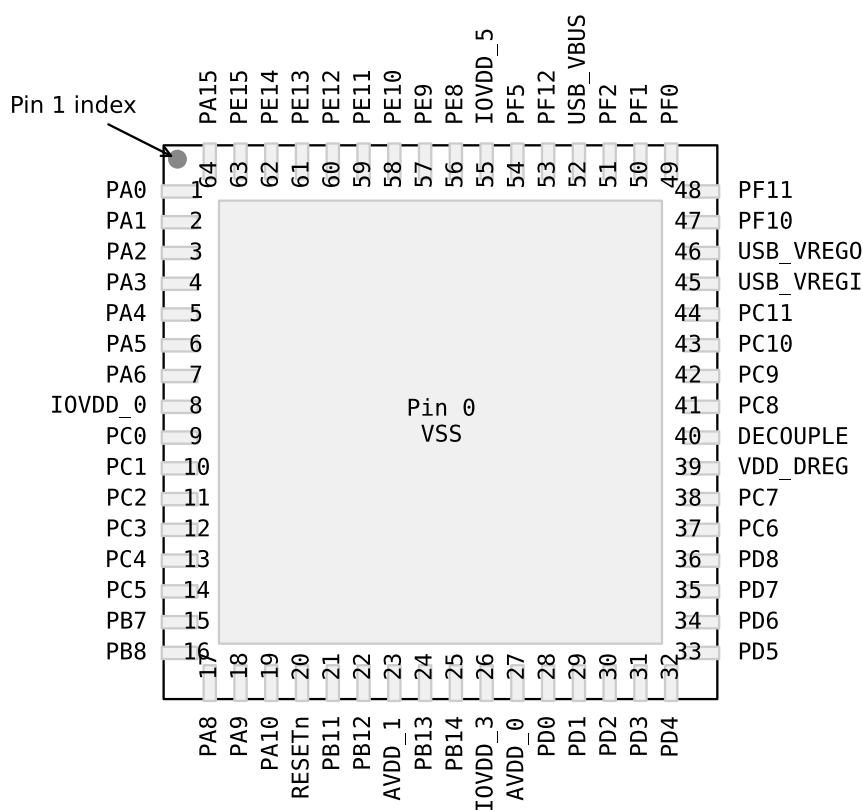
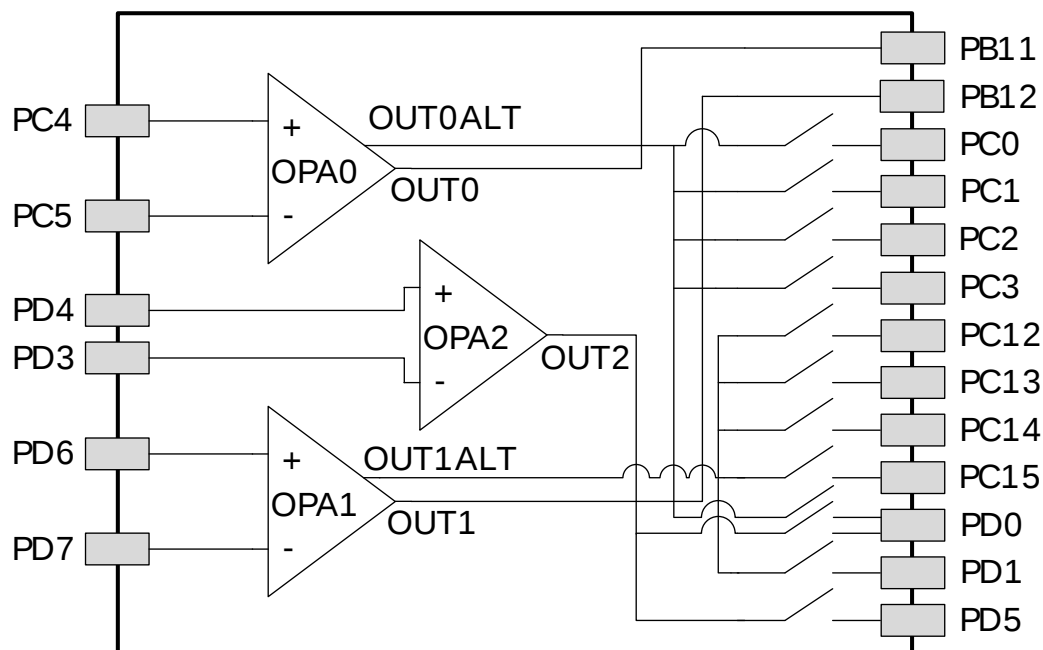


Table 4.1. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	I2C0_SDA #0 LEU0_RX #4	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

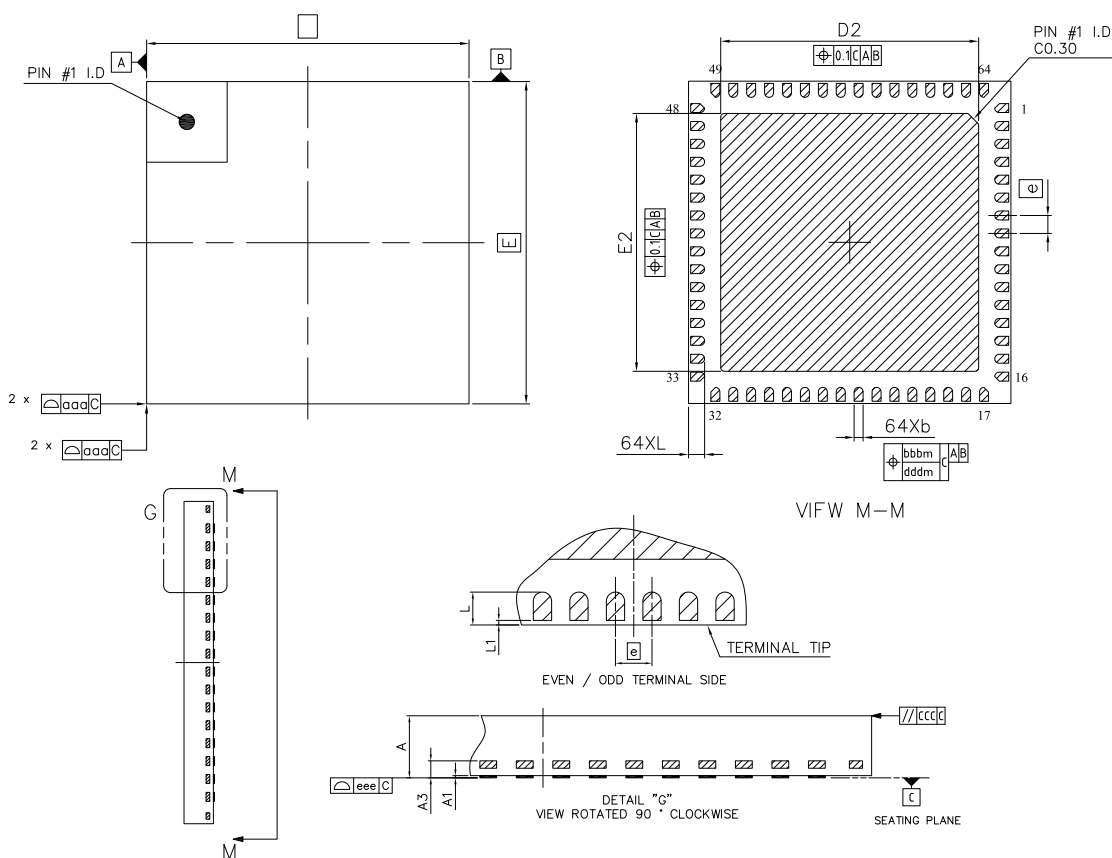
QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
4	PA3		TIM0_CDTI0 #0		LES_ALTEX2 #0 ETM_TD1 #3
5	PA4		TIM0_CDTI1 #0		LES_ALTEX3 #0 ETM_TD2 #3
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	PA6			LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
8	IOVDD_0	Digital IO power supply 0.			
9	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
10	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
11	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
12	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
13	PC4	ACMP0_CH4 OPAMP_P0	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
14	PC5	ACMP0_CH5 OPAMP_N0	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
15	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
16	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0 / OPAMP_OUT0	LETIM0_OUT0 #1 TIM1_CC2 #3	I2C1_SDA #1	
22	PB12	DAC0_OUT1 / OPAMP_OUT1	LETIM0_OUT1 #1	I2C1_SCL #1	
23	AVDD_1	Analog power supply 1.			
24	PB13	HFX TAL_P		US0_CLK #4/5 LEU0_TX #1	
25	PB14	HFX TAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	

Figure 4.2. Opamp Pinout



4.5 QFN64 Package

Figure 4.3. QFN64



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Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.

7 Revision History

7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with $FULLBIAS=1$ and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

7.5 Revision 1.10

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.7 Revision 0.98

May 25th, 2012

Corrected EM3 current consumption in the Electrical Characteristics section.

7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected QFN64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected QFN64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

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