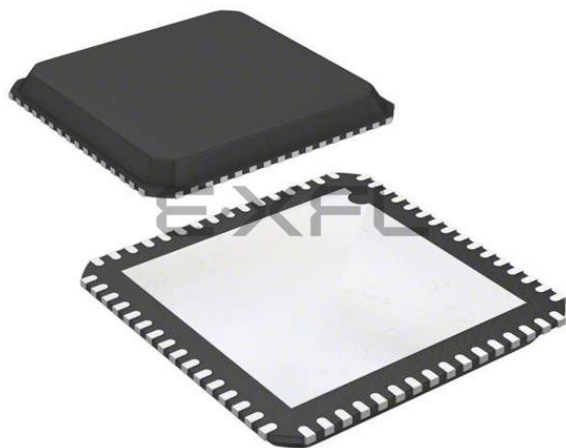




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg330f512-qfn64t

Table 3.5. Power Management

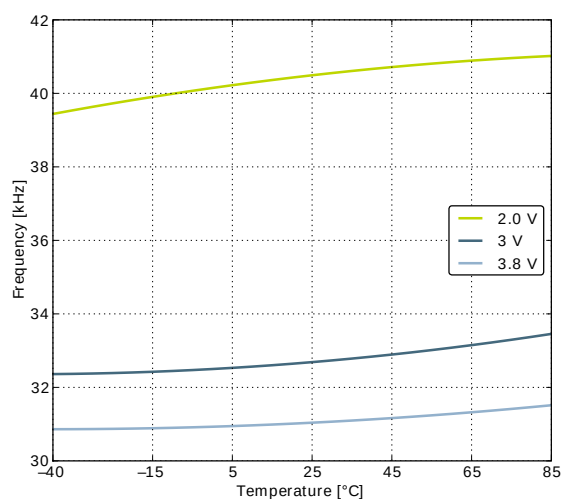
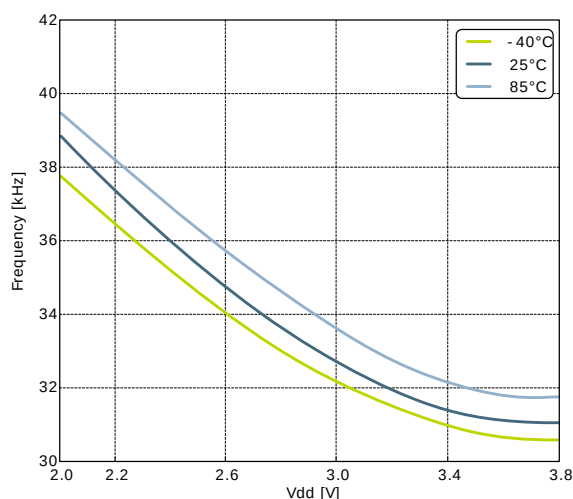
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.74		1.98	V
V _{BODintthr-}	BOD threshold on falling internally regulated supply voltage		1.57		1.70	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85	1.98	V
V _{PORthr+}	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF
C _{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		μF
C _{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		μF

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$		31.29	32.768	34.28	kHz
t_{LFRCO}	Startup time not including software calibration			150		μs
I_{LFRCO}	Current consumption			300	900	nA
$\text{TUNESTEP}_{\text{LFRCO}}$	Frequency step for LSB change in TUNING value			1.5		%

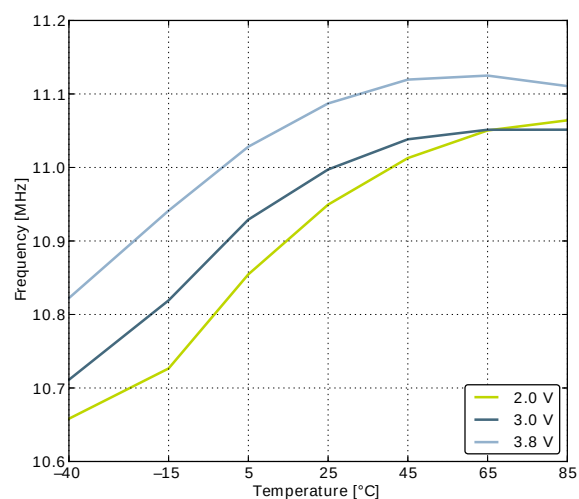
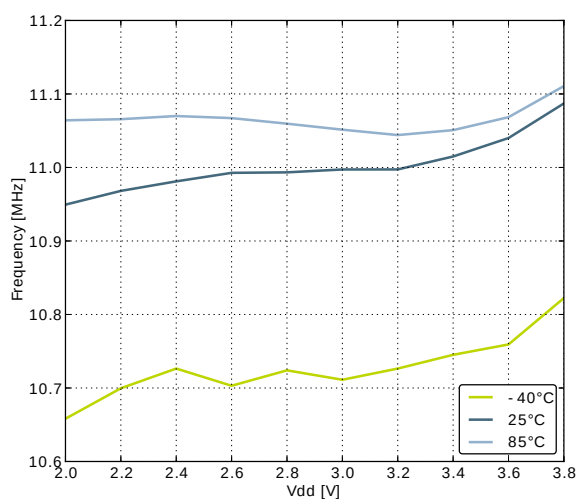
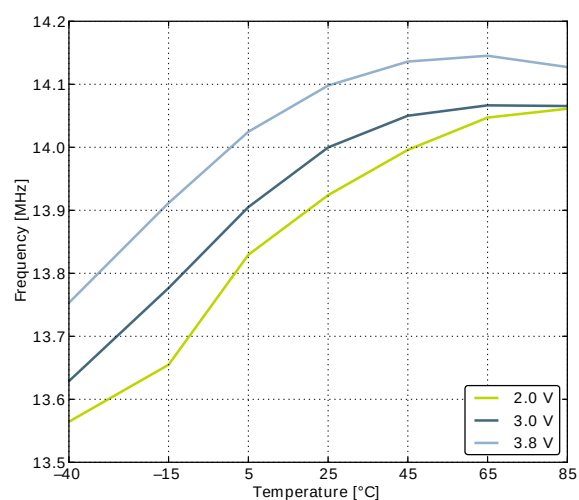
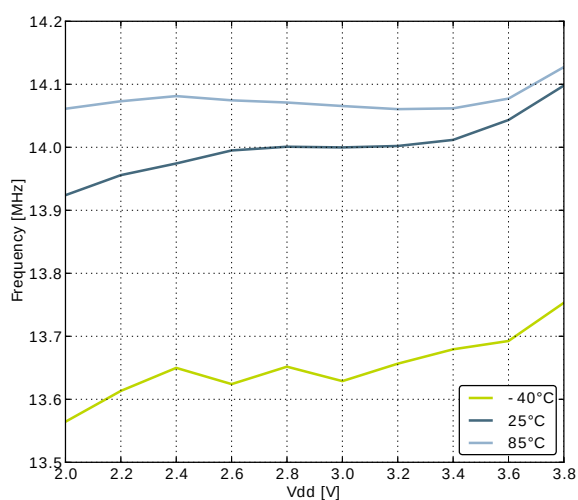
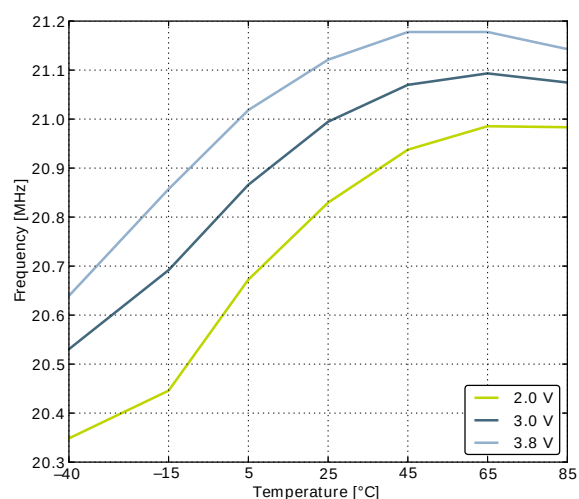
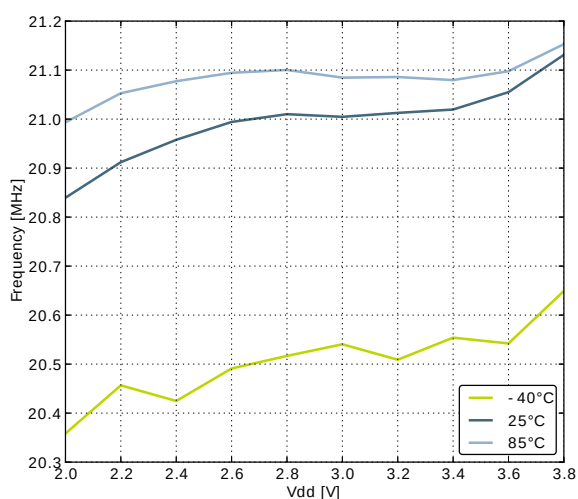
Figure 3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.4 HFRCO

Table 3.11. HFRCO

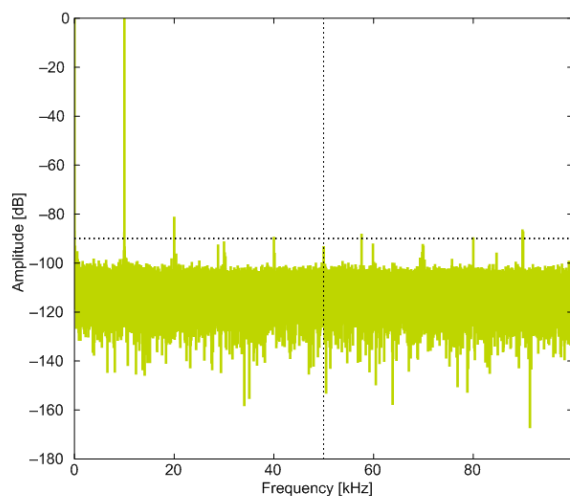
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48 ¹	6.60 ¹	6.72 ¹	MHz
		1 MHz frequency band	1.15 ²	1.20 ²	1.25 ²	MHz
$t_{\text{HFRCO_settling}}$	Settling time after start-up	$f_{\text{HFRCO}} = 14 \text{ MHz}$		0.6		Cycles
	Settling time after band switch			25		Cycles

Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature**

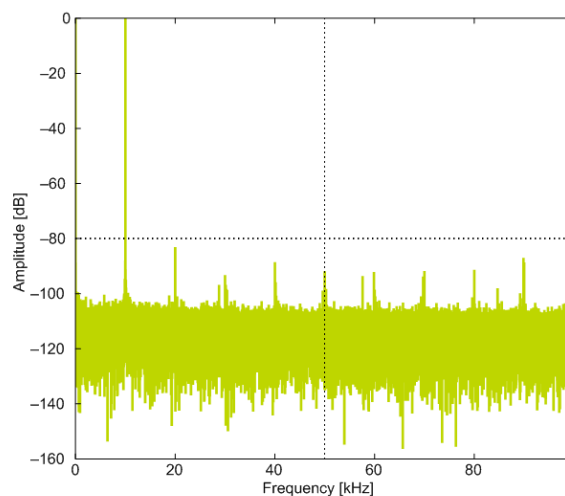
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		79		dBc
V _{ADCOFFSET}	Offset voltage	After calibration, single ended		0.3		mV
		After calibration, differential	-3	0.3	3	mV
TGRAD _{ADCTH}	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL _{ADC}	Differential non-linearity (DNL)	$V_{DD} = 3.0$ V, external 2.5V reference	-1	±0.7	4	LSB
INL _{ADC}	Integral non-linearity (INL), End point method			±1.2	±3.0	LSB
MC _{ADC}	No missing codes		11.999 ¹	12		bits

3.10.1 Typical performance

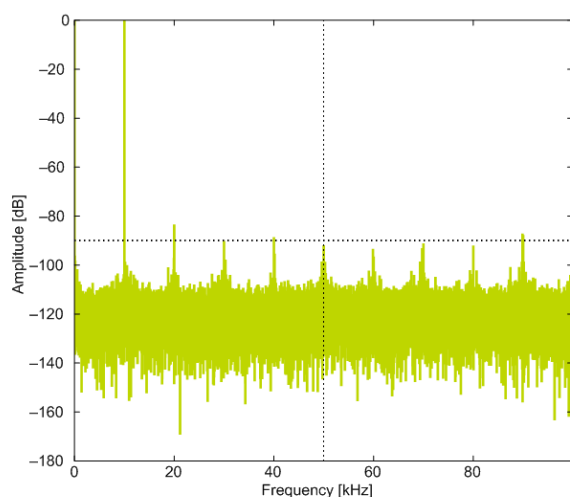
Figure 3.19. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



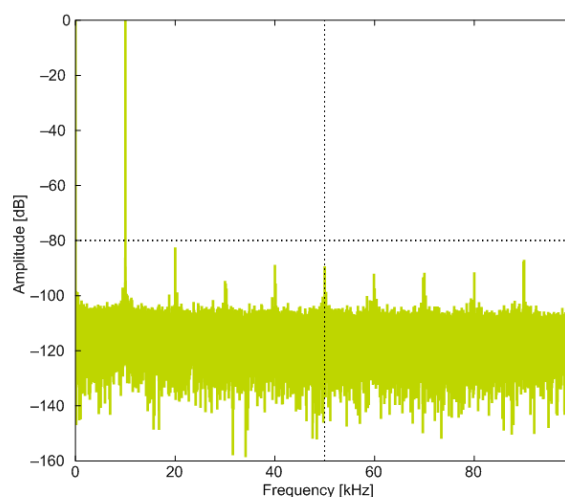
1.25V Reference



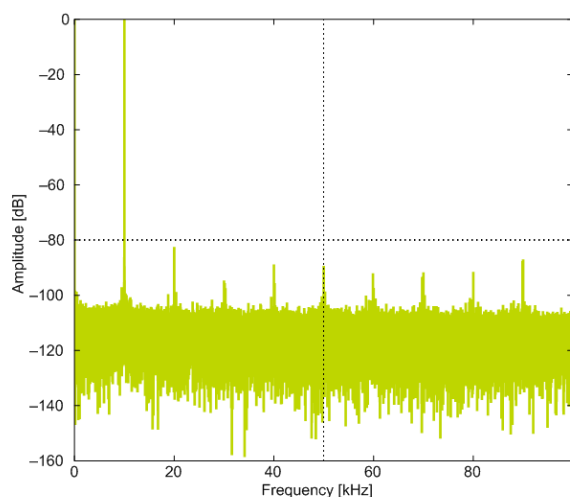
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

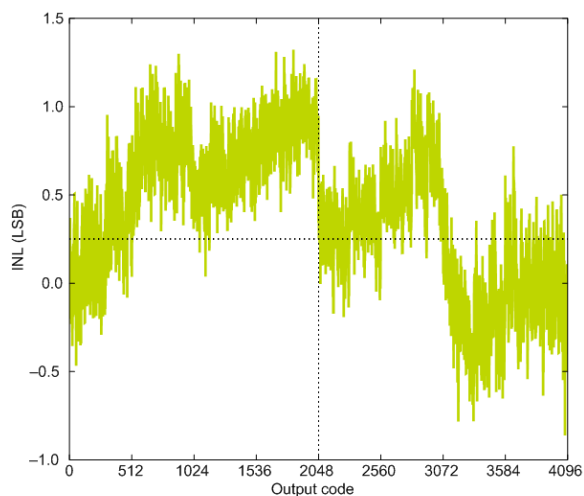
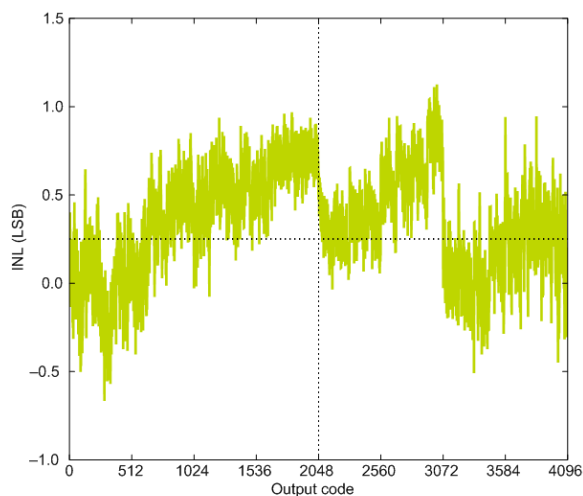
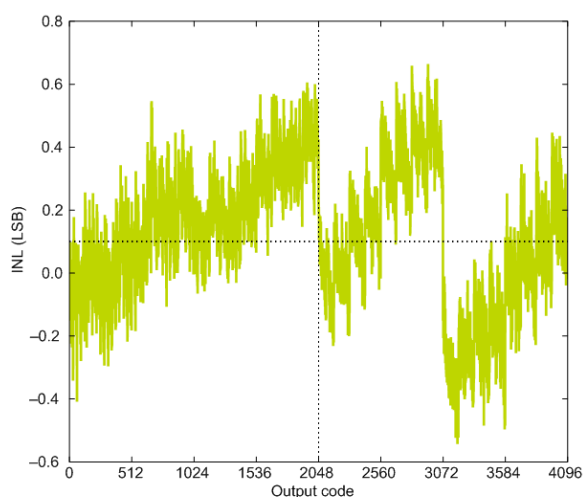
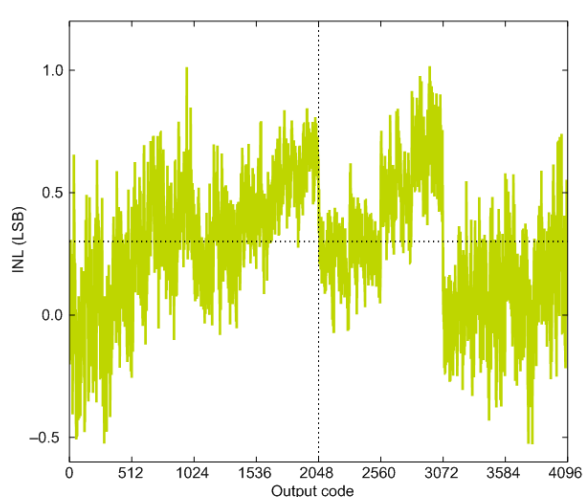
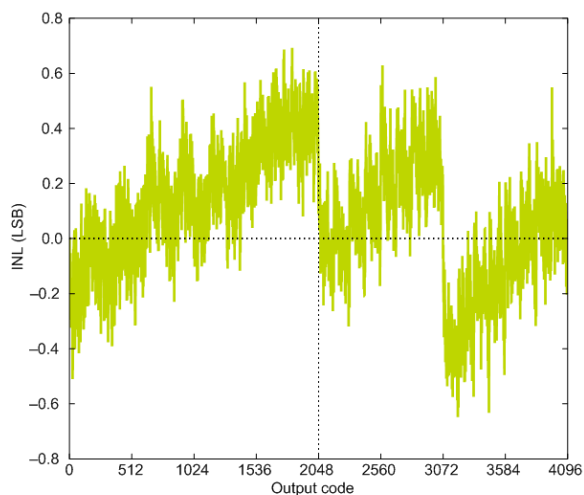
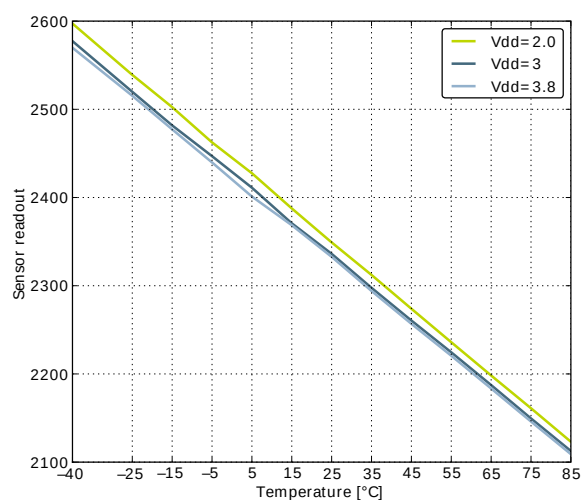
Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.24. ADC Temperature sensor readout

3.11 Digital Analog Converter (DAC)

Table 3.15. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12 bit		400 ¹	600 ¹	μA
		100 kSamples/s, 12 bit		200 ¹	260 ¹	μA
		1 kSamples/s 12 bit NORMAL		17 ¹	25 ¹	μA
SR_{DAC}	Sample rate				500	ksamples/s
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cycles per conversion			2		
$t_{DACCONV}$	Conversion time		2			μs
$t_{DACSETTLE}$	Settling time			5		μs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		58		dB

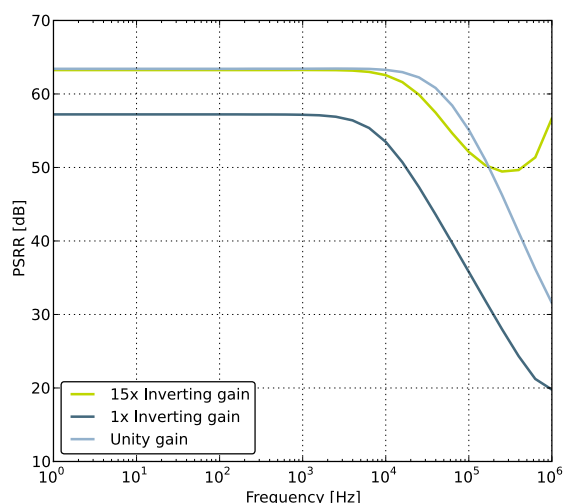
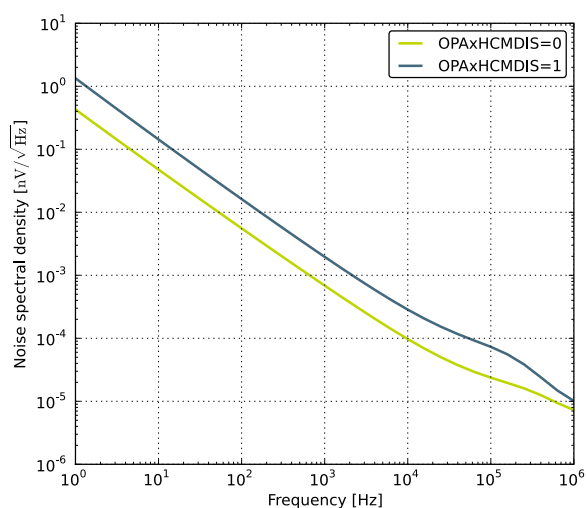
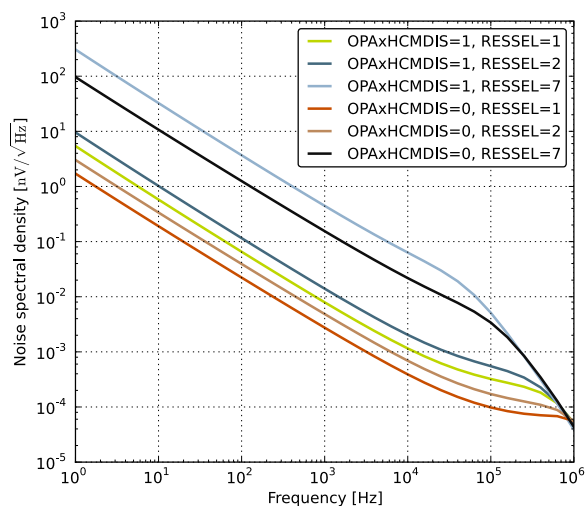
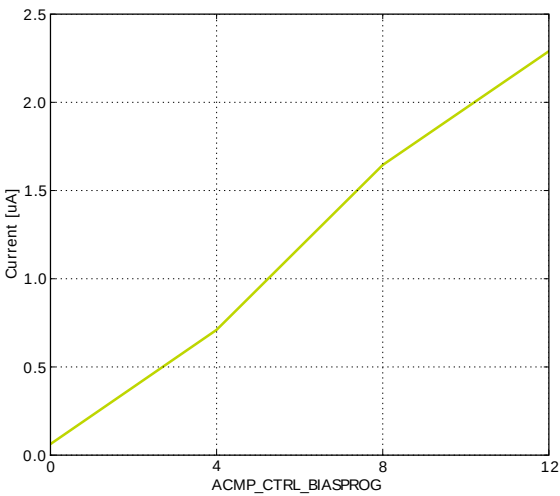
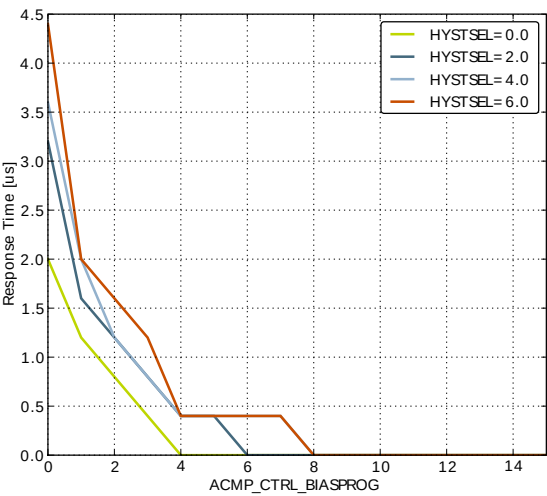
Figure 3.27. OPAMP Negative Power Supply Rejection Ratio**Figure 3.28. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}=1V$** **Figure 3.29. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)**

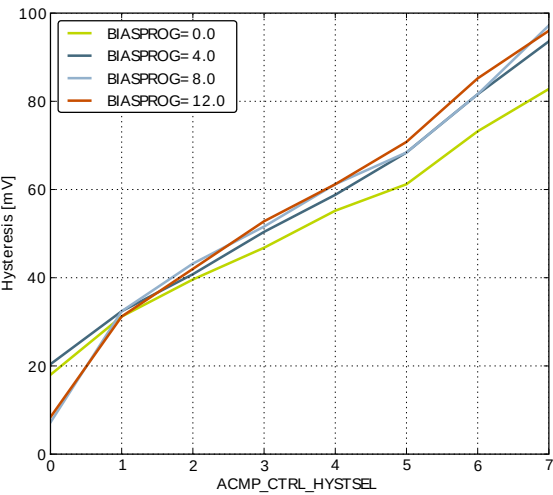
Figure 3.30. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time



Hysteresis

3.14 Voltage Comparator (VCMP)

Table 3.18. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMPCM}	VCMP Common Mode voltage range			V _{DD}		V
I _{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	30	μA
t _{VCMPREF}	Startup time reference generator	NORMAL		10		μs
V _{VCMPOFFSET}	Offset voltage	Single ended	-230	-40	190	mV
		Differential		10		mV
V _{VCMPHYST}	VCMP hysteresis			40		mV
t _{VCMPSTART}	Startup time				10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL} \quad (3.2)$$

3.15 I2C

Table 3.19. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and START condition	4.7			μs

¹For the minimum HPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32GG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10⁻⁹ [s] * f_{HPERCLK} [Hz]) - 4).

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32GG330.

4.1 Pinout

The EFM32GG330 pinout is shown in Figure 4.1 (p. 49) and Table 4.1 (p. 49). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32GG330 Pinout (top view, not to scale)

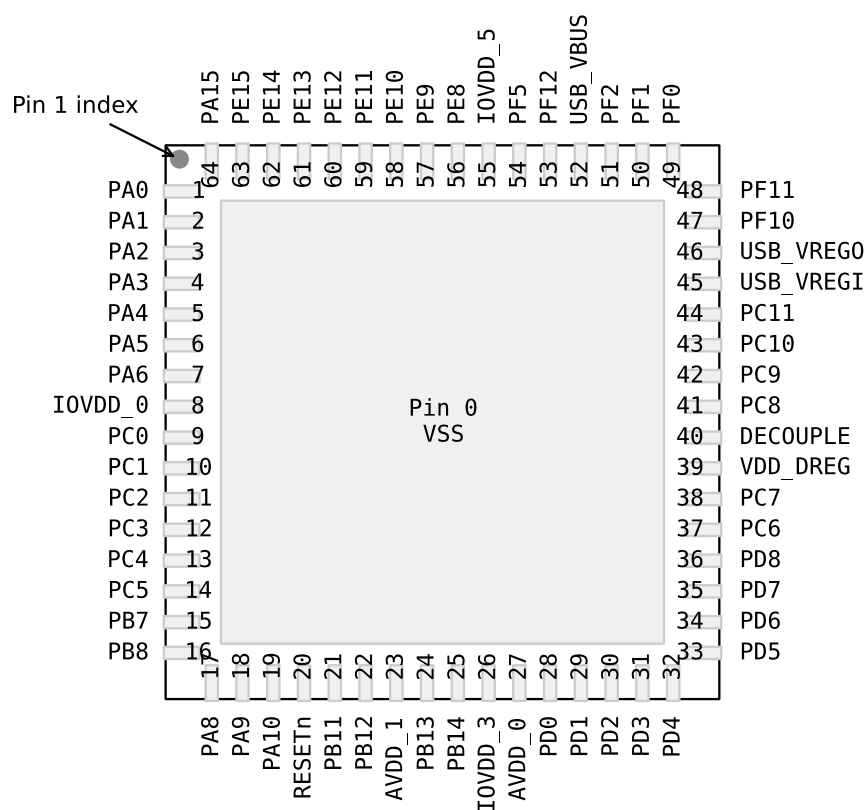


Table 4.1. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	I2C0_SDA #0 LEU0_RX #4	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
4	PA3		TIM0_CDTI0 #0		LES_ALTEX2 #0 ETM_TD1 #3
5	PA4		TIM0_CDTI1 #0		LES_ALTEX3 #0 ETM_TD2 #3
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	PA6			LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
8	IOVDD_0	Digital IO power supply 0.			
9	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
10	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
11	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
12	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
13	PC4	ACMP0_CH4 OPAMP_P0	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
14	PC5	ACMP0_CH5 OPAMP_N0	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
15	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
16	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0 / OPAMP_OUT0	LETIM0_OUT0 #1 TIM1_CC2 #3	I2C1_SDA #1	
22	PB12	DAC0_OUT1 / OPAMP_OUT1	LETIM0_OUT1 #1	I2C1_SCL #1	
23	AVDD_1	Analog power supply 1.			
24	PB13	HFX TAL_P		US0_CLK #4/5 LEU0_TX #1	
25	PB14	HFX TAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	

3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Table 4.4. QFN64 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.20	9.00 BSC	9.00 BSC	7.10	7.10	0.50 BSC	0.40	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	-		0.25			7.20	7.20		0.45						
Max	0.90	0.05		0.30			7.30	7.30		0.50	0.10					

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
<http://www.silabs.com/support/quality/pages/default.aspx>

Figure 5.2. QFN64 PCB Solder Mask

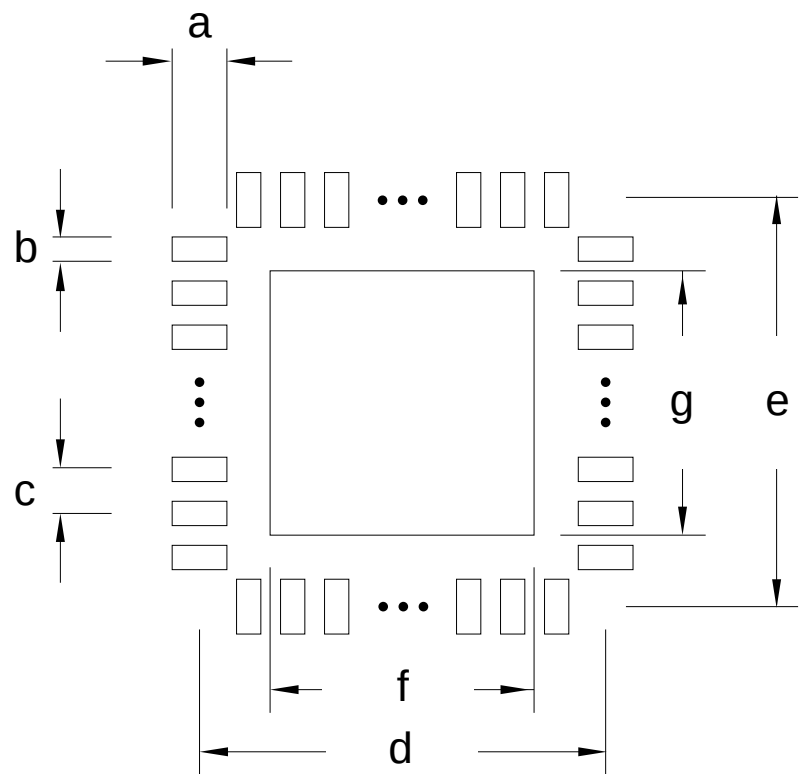
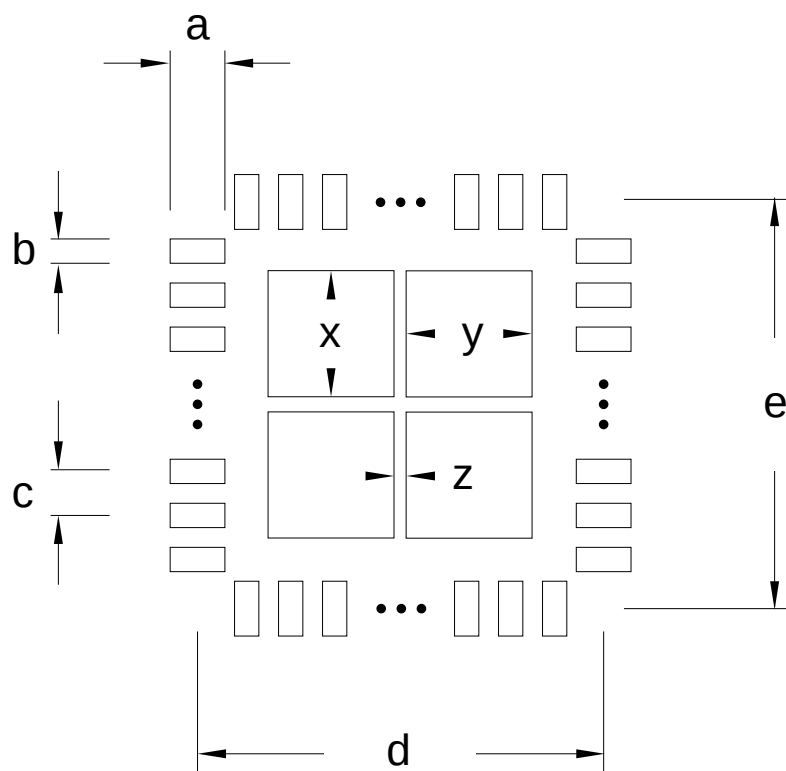


Table 5.2. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.97	e	8.90
b	0.42	f	7.32
c	0.50	g	7.32
d	8.90	-	-

Figure 5.3. QFN64 PCB Stencil Design**Table 5.3. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.75	e	8.90
b	0.22	x	2.70
c	0.50	y	2.70
d	8.90	z	0.80

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 57) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

7 Revision History

7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with $FULLBIAS=1$ and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

Updated GPIO information.

Updated LFRCO information.

Updated HFRCO information.

Updated ULFRCO information.

Updated ADC information.

Updated DAC information.

Updated OPAMP information.

Updated ACMP information.

Updated VCMP information.

Added AUXHFRCO information.

7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

7.4 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Added SPI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Added the USB bootloader information.

Updated that the EM2 current consumption test was carried out with only one RAM block enabled.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Removed UART mentioned incorrectly in the QFN64 parts.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

B Contact Information

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Please visit the Silicon Labs Technical Support web page:

<http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.

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