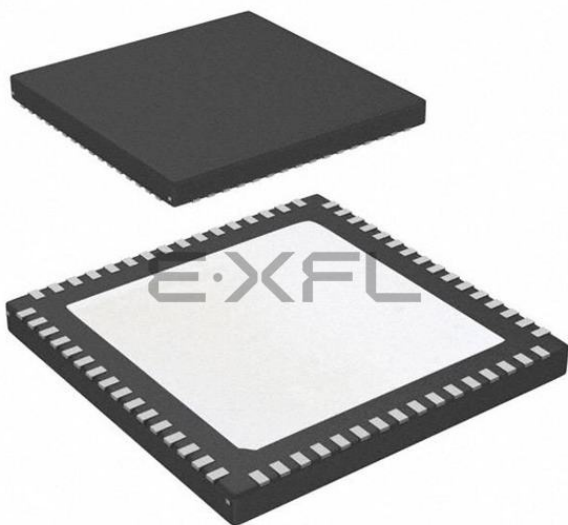




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg330f512g-e-qfn64

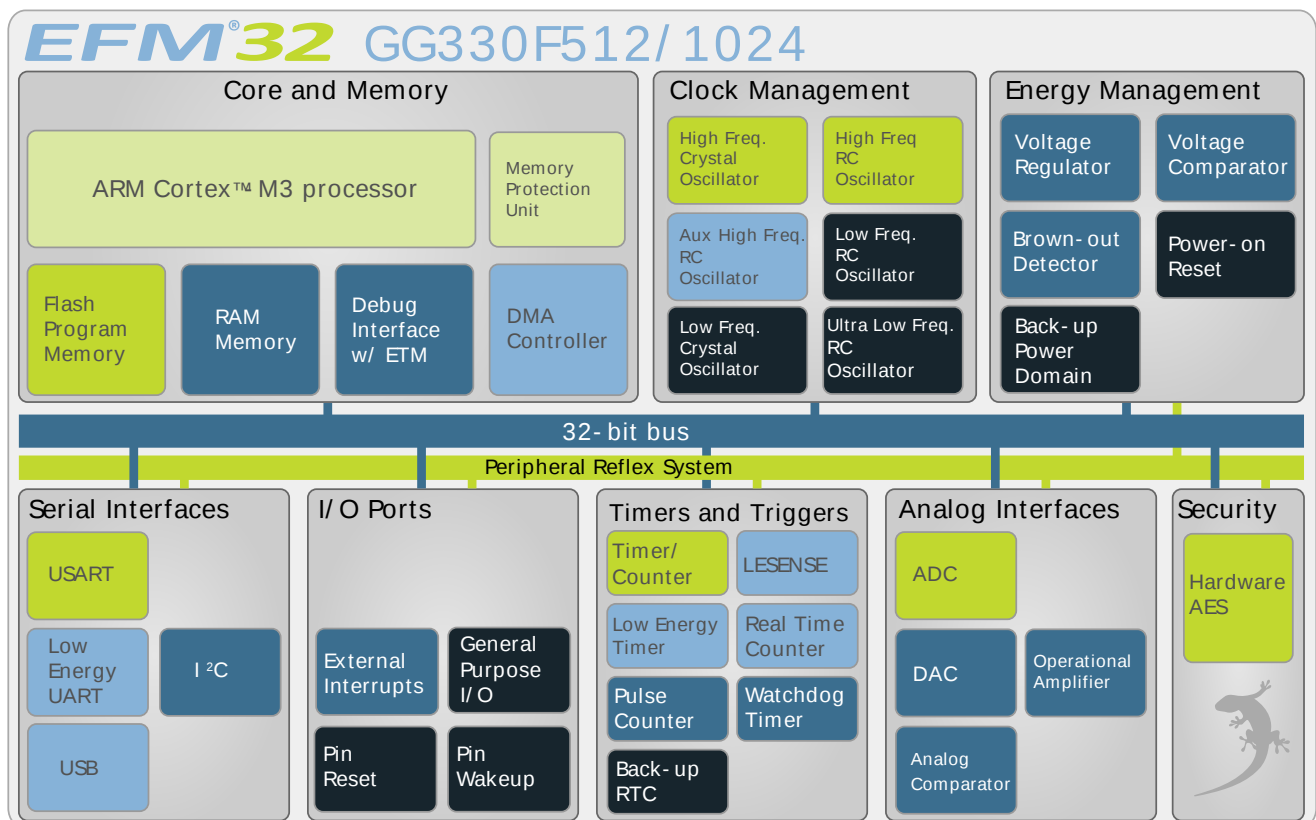
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32GG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32GG330 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32GG Reference Manual*.

A block diagram of the EFM32GG330 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

Figure 2.2. EFM32GG330 Memory Map with largest RAM and Flash sizes

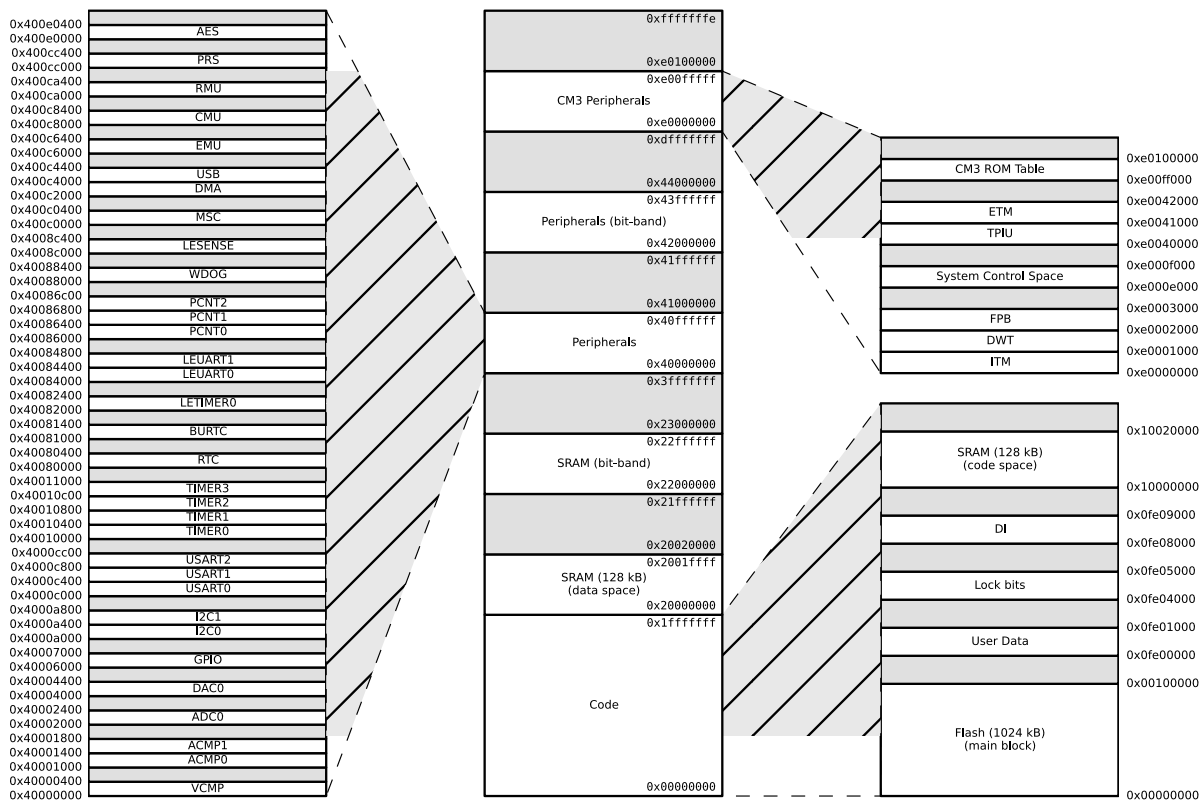
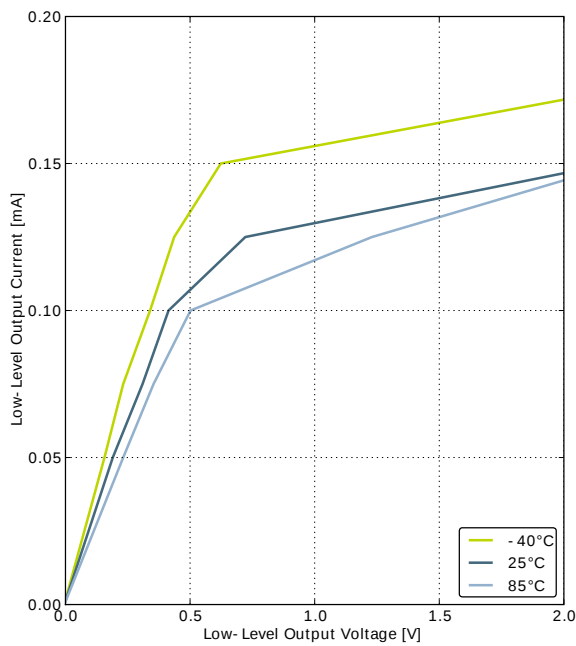
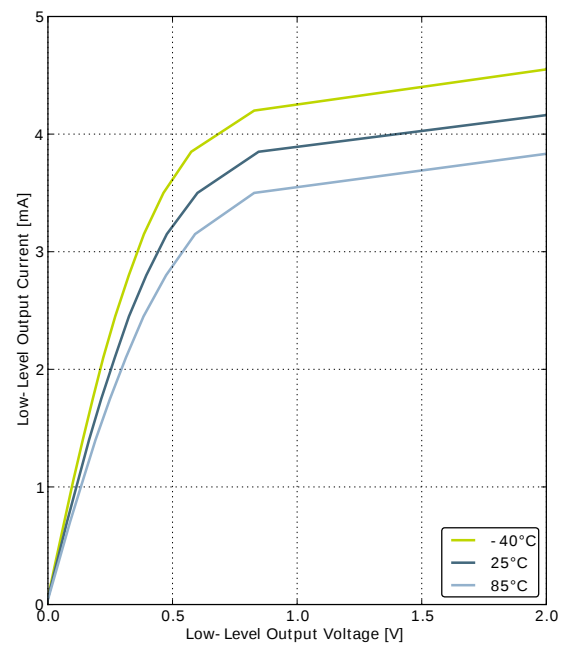


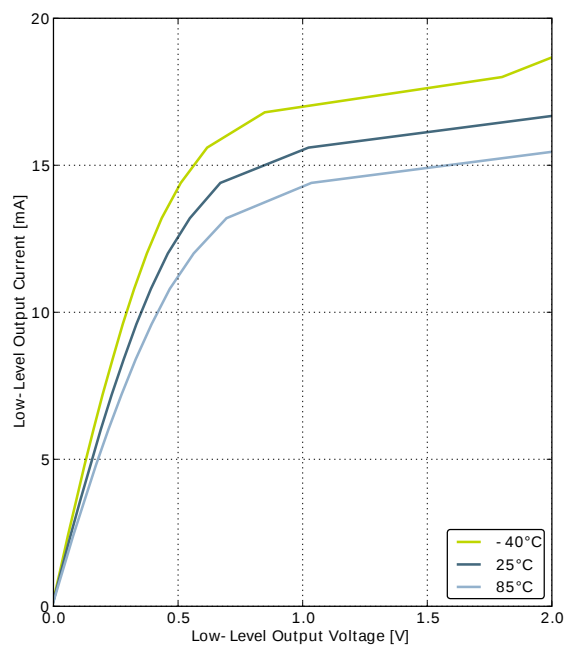
Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage



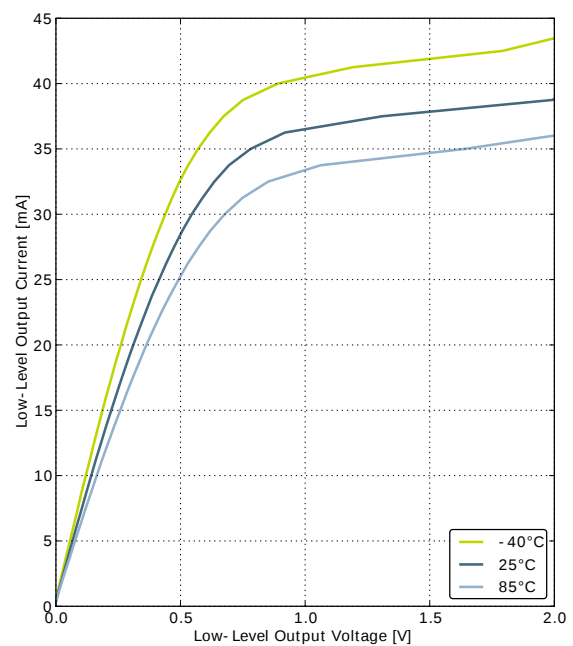
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

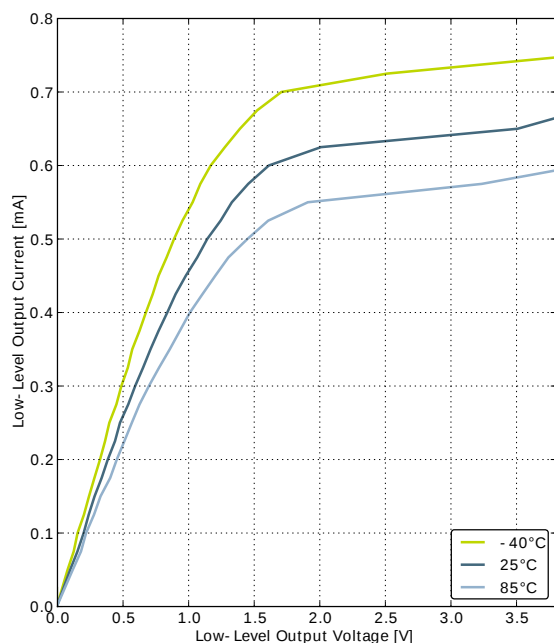


GPIO_Px_CTRL DRIVEMODE = STANDARD

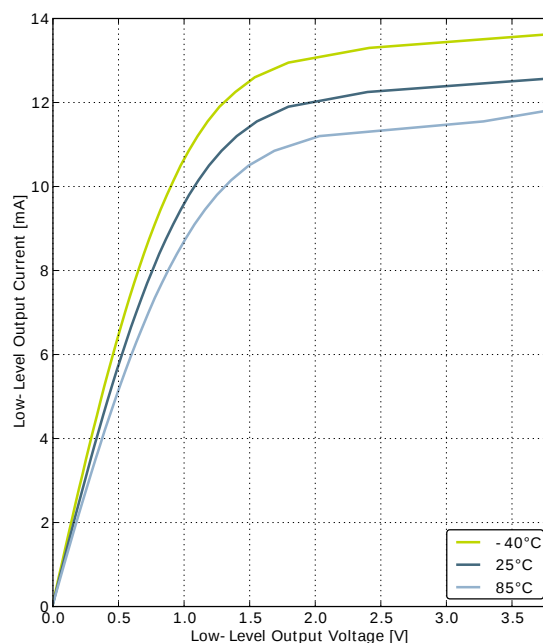


GPIO_Px_CTRL DRIVEMODE = HIGH

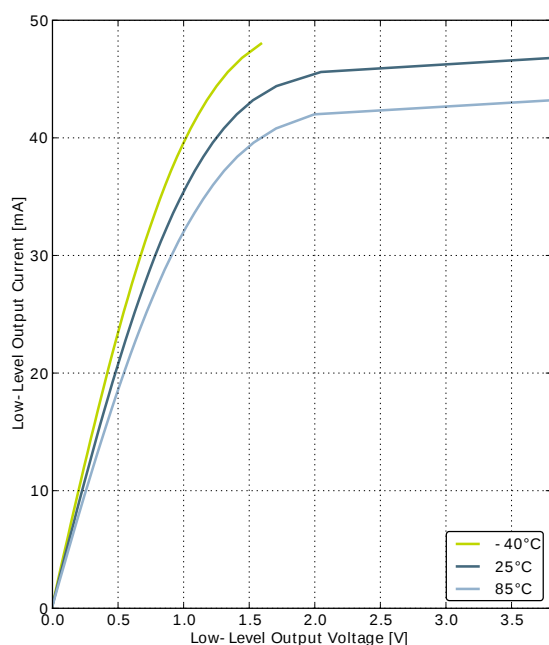
Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



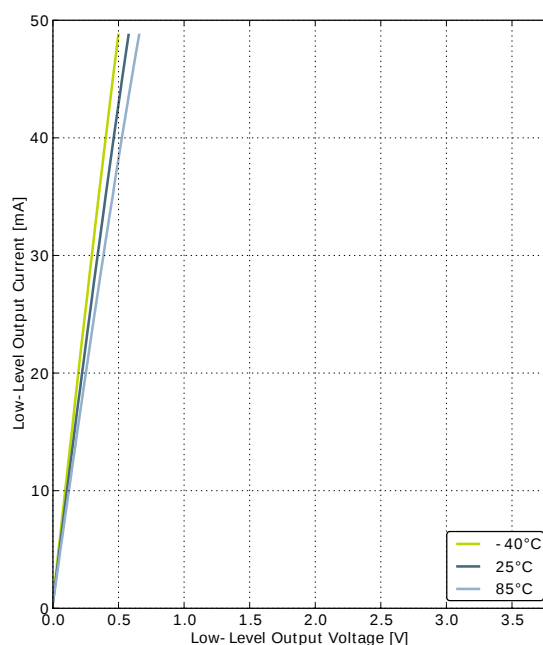
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	63	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		70		dB
SINAD _{ADC}	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	65		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
GAIN _{ED}	Gain error drift	1.25V reference		0.01 ²	0.033 ³	%/°C
		2.5V reference		0.01 ²	0.03 ³	%/°C
OFFSET _{ED}	Offset error drift	1.25V reference		0.2 ²	0.7 ³	LSB/°C
		2.5V reference		0.2 ²	0.62 ³	LSB/°C

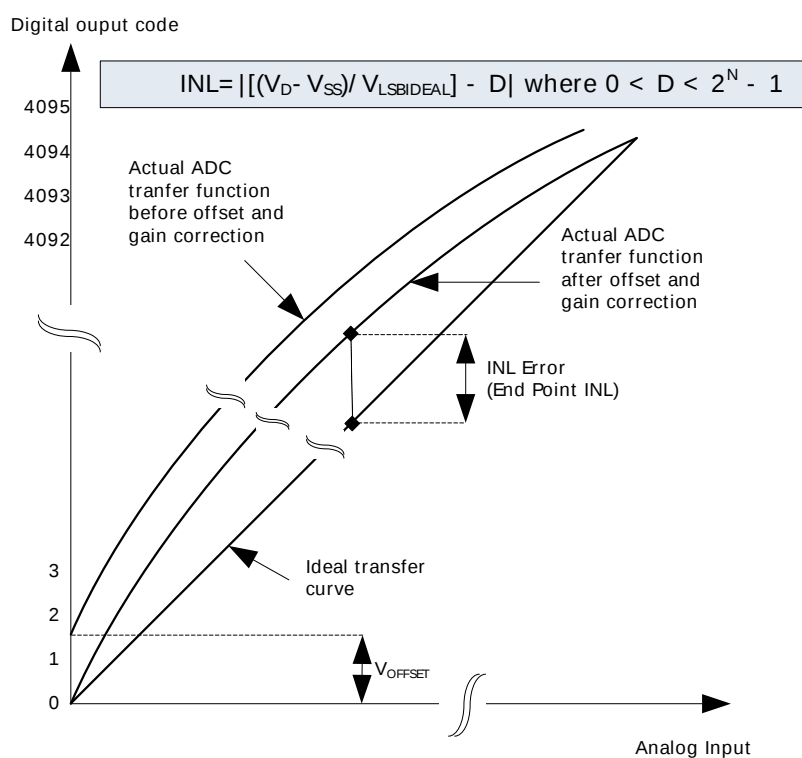
¹On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.

³Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

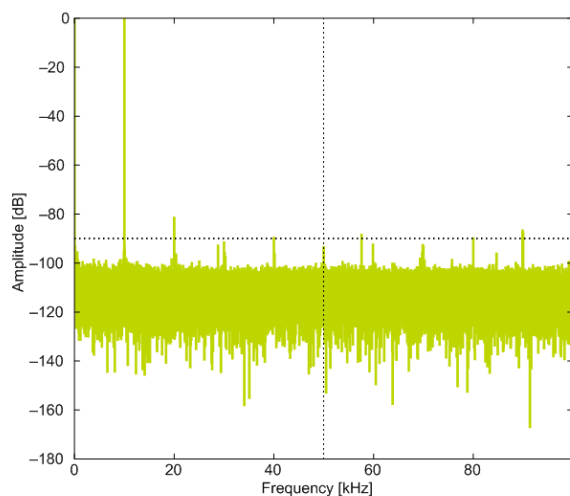
The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 32) and Figure 3.18 (p. 33) , respectively.

Figure 3.17. Integral Non-Linearity (INL)

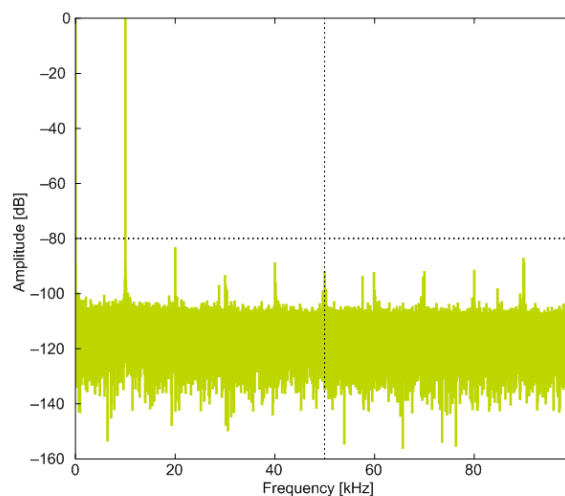


3.10.1 Typical performance

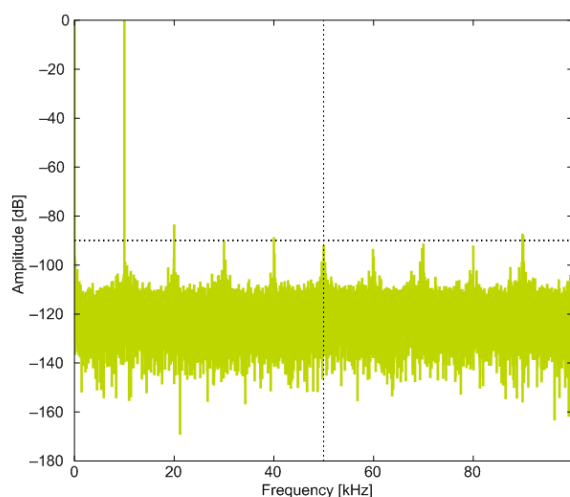
Figure 3.19. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



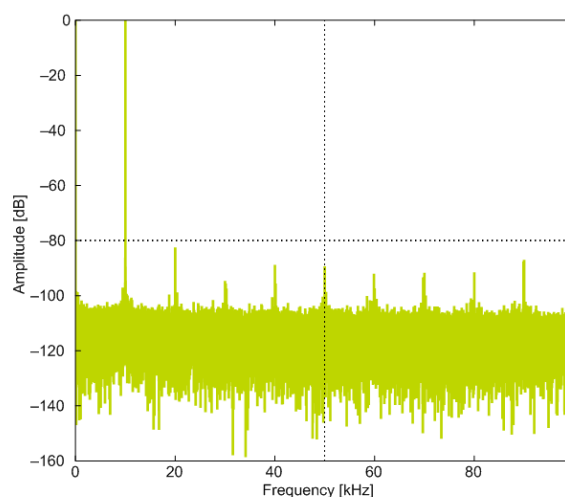
1.25V Reference



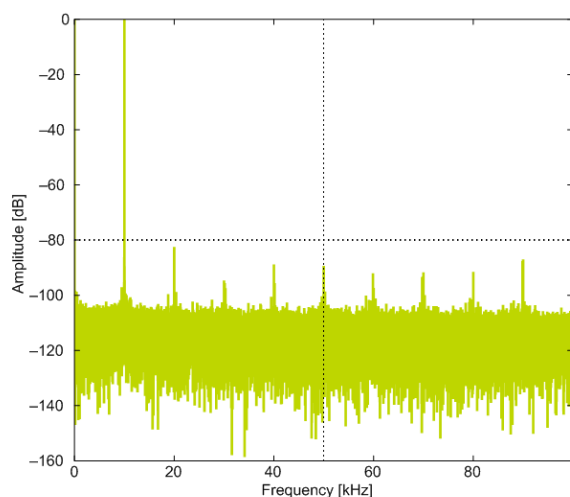
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

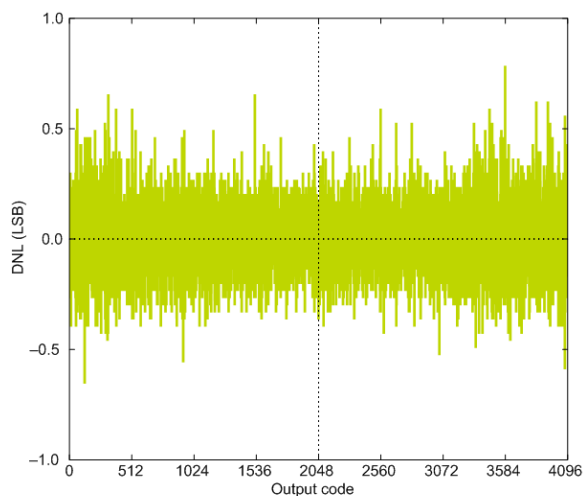
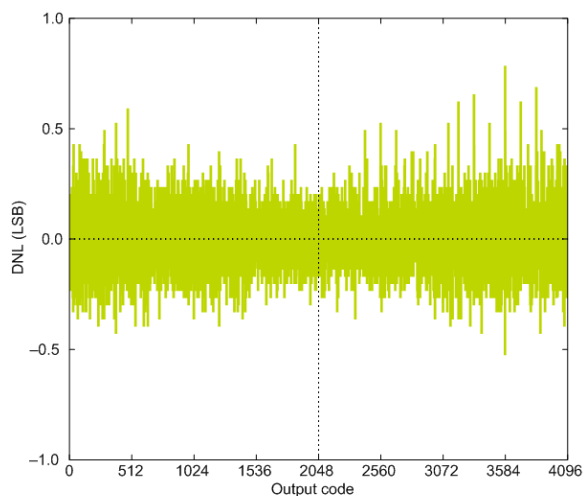
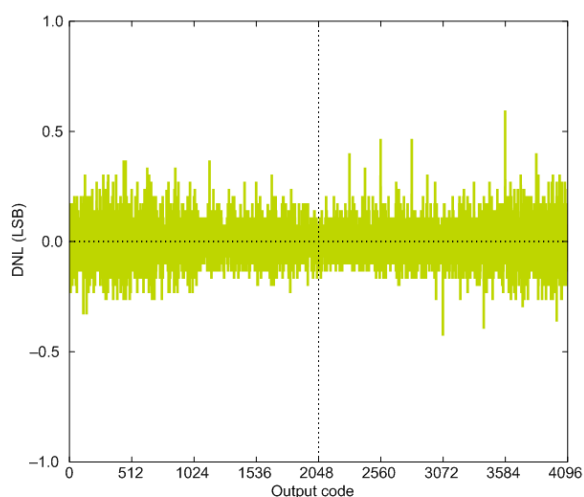
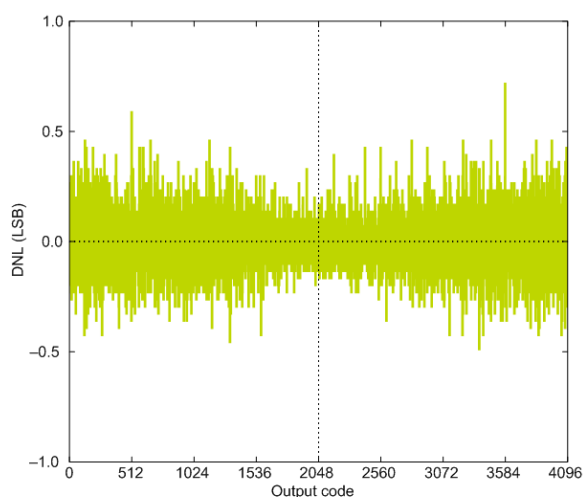
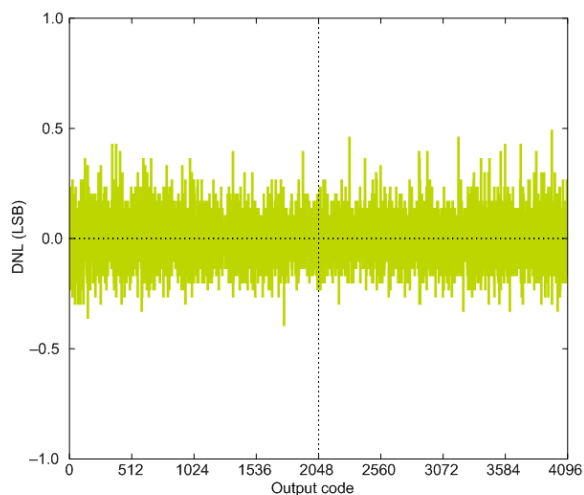
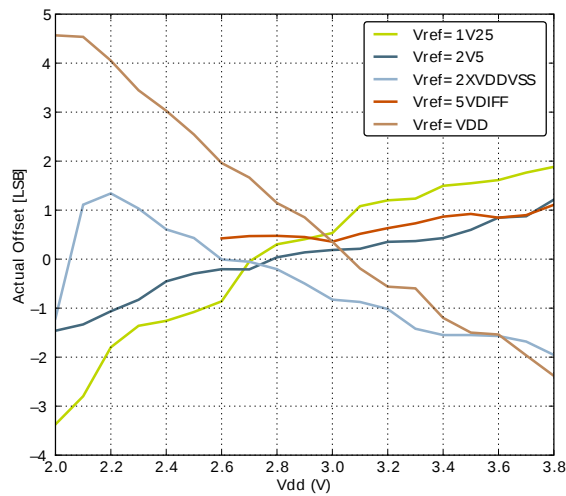
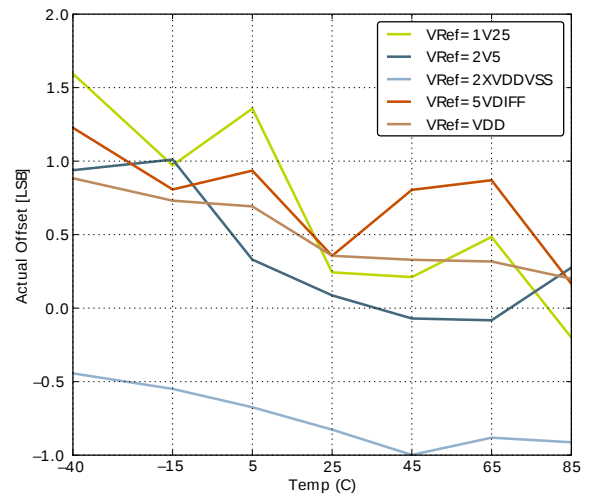
Figure 3.21. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.22. ADC Absolute Offset, Common Mode = $V_{dd}/2$

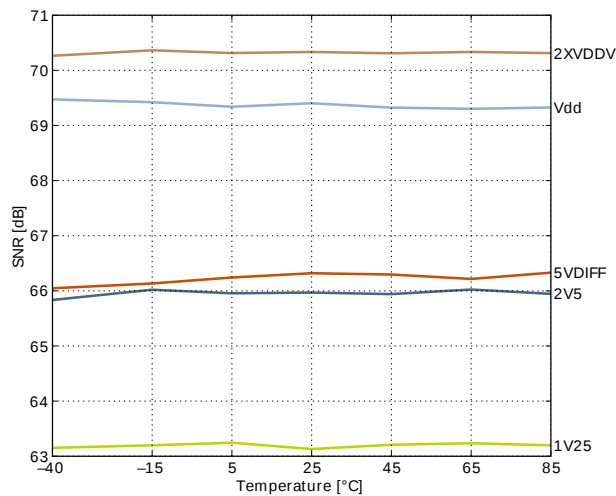


Offset vs Supply Voltage, Temp = 25°C

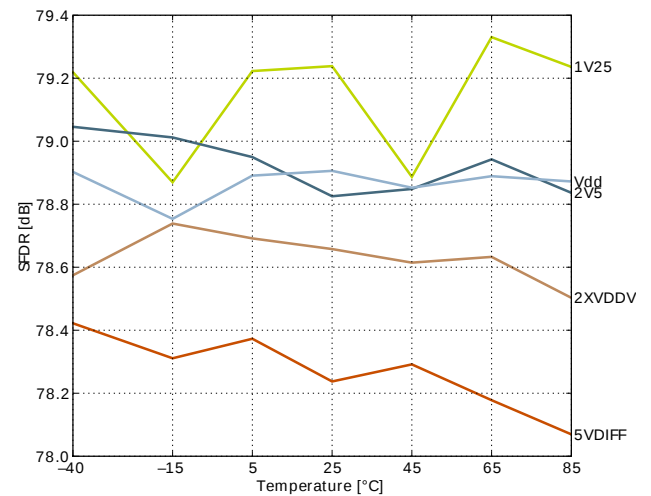


Offset vs Temperature, $V_{dd} = 3V$

Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, $V_{dd} = 3V$



Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		196		μV_{RMS}
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		229		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=0		1230		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=1		2130		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		1630		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		2590		μV_{RMS}

Figure 3.25. OPAMP Common Mode Rejection Ratio

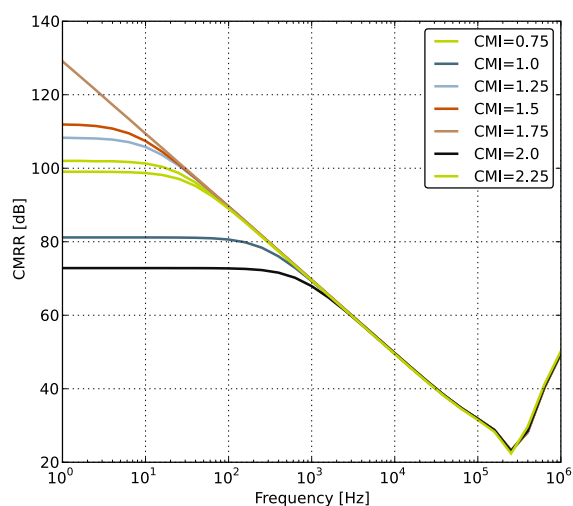
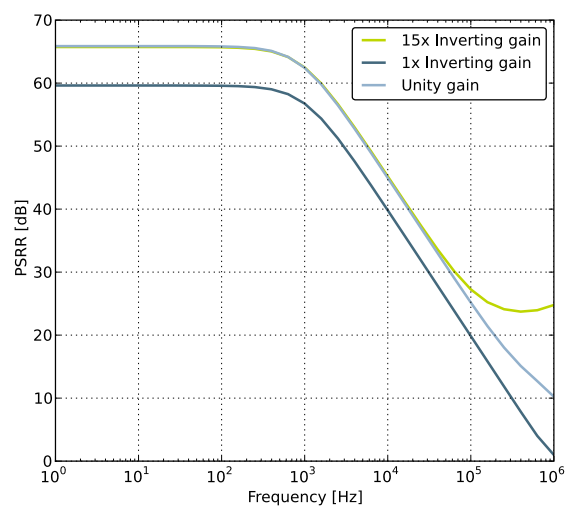


Figure 3.26. OPAMP Positive Power Supply Rejection Ratio



3.13 Analog Comparator (ACMP)

Table 3.17. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.6	μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	12	μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		250	520	μA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		μA
		Internal voltage reference		5		μA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		43		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		78		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		111		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		145		kOhm
$t_{ACMPSTART}$	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 43) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

Table 3.20. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32GG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((900 \cdot 10^{-9} [s] \cdot f_{HPERCLK} [Hz]) - 4)$.

Table 3.21. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		1000 ¹	kHz
t _{LOW}	SCL clock low time	0.5			μs
t _{HIGH}	SCL clock high time	0.26			μs
t _{SU,DAT}	SDA set-up time	50			ns
t _{HD,DAT}	SDA hold time	8			ns
t _{SU,STA}	Repeated START condition set-up time	0.26			μs
t _{HD,STA}	(Repeated) START condition hold time	0.26			μs
t _{SU,STO}	STOP condition set-up time	0.26			μs
t _{BUF}	Bus free time between a STOP and START condition	0.5			μs

¹For the minimum HPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32GG Reference Manual.

3.16 USART SPI

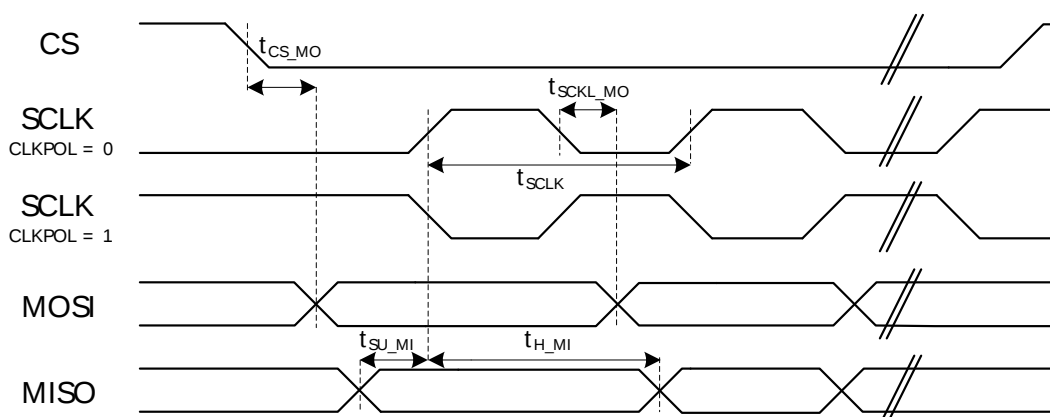
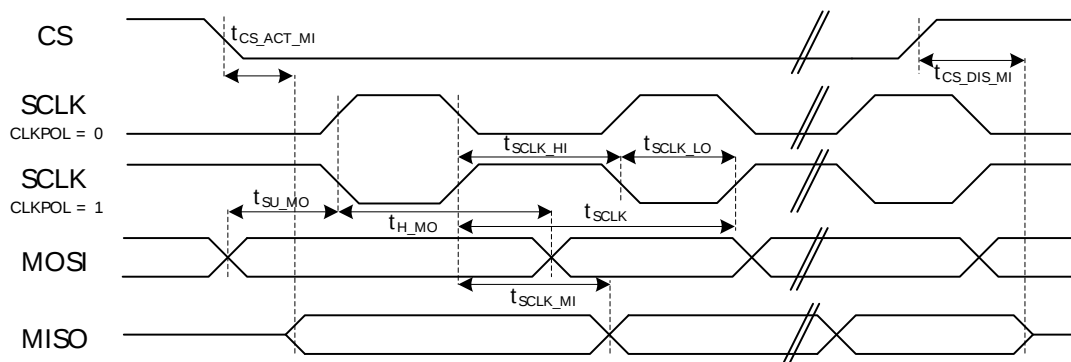
Figure 3.31. SPI Master Timing

Table 3.22. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{SCLK}}^{1,2}$	SCLK period		$2 * t_{\text{HFER-CLK}}$			ns
$t_{\text{CS_MO}}^{1,2}$	CS to MOSI		-2.00		1.00	ns
$t_{\text{SCLK_MO}}^{1,2}$	SCLK to MOSI		-4.00		3.00	ns
$t_{\text{SU_MI}}^{1,2}$	MISO setup time	IOVDD = 1.98 V	36.00			ns
		IOVDD = 3.0 V	29.00			ns
$t_{\text{H_MI}}^{1,2}$	MISO hold time		-4.00			ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Figure 3.32. SPI Slave Timing**Table 3.23. SPI Slave Timing**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{SCLK_sl}}^{1,2}$	SCKL period	$2 * t_{\text{HFER-CLK}}$			ns
$t_{\text{SCLK_hi}}^{1,2}$	SCLK high period	$3 * t_{\text{HFER-CLK}}$			ns
$t_{\text{SCLK_lo}}^{1,2}$	SCLK low period	$3 * t_{\text{HFER-CLK}}$			ns
$t_{\text{CS_ACT_MI}}^{1,2}$	CS active to MISO	4.00		30.00	ns
$t_{\text{CS_DIS_MI}}^{1,2}$	CS disable to MISO	4.00		30.00	ns
$t_{\text{SU_MO}}^{1,2}$	MOSI setup time	4.00			ns
$t_{\text{H_MO}}^{1,2}$	MOSI hold time	$2 + 2 * t_{\text{HFER-CLK}}$			ns
$t_{\text{SCLK_MI}}^{1,2}$	SCLK to MISO	$9 + t_{\text{HFER-CLK}}$		$36 + 2 * t_{\text{HFER-CLK}}$	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

3.17 USB

The USB hardware in the EFM32GG330 passes all tests for USB 2.0 Full Speed certification. See the test-report distributed with application note "AN0046 - USB Hardware Design Guide".

3.18 Digital Peripherals

Table 3.24. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{USART}	USART current	USART idle current, clock enabled		4.9		μA/ MHz
I _{UART}	UART current	UART idle current, clock enabled		3.4		μA/ MHz
I _{LEUART}	LEUART current	LEUART idle current, clock enabled		140		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		6.1		μA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.9		μA/ MHz
I _{LETIMER}	LETIMER current	LETIMER idle current, clock enabled		119		nA
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		54		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		54		nA
I _{AES}	AES current	AES idle current, clock enabled		3.2		μA/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock enabled		3.7		μA/ MHz
I _{PRS}	PRS current	PRS idle current		3.5		μA/ MHz
I _{DMA}	DMA current	Clock enable		11.0		μA/ MHz

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
4	PA3		TIM0_CDTI0 #0		LES_ALTEX2 #0 ETM_TD1 #3
5	PA4		TIM0_CDTI1 #0		LES_ALTEX3 #0 ETM_TD2 #3
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	PA6			LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
8	IOVDD_0	Digital IO power supply 0.			
9	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
10	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
11	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
12	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
13	PC4	ACMP0_CH4 OPAMP_P0	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
14	PC5	ACMP0_CH5 OPAMP_N0	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
15	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
16	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0 / OPAMP_OUT0	LETIM0_OUT0 #1 TIM1_CC2 #3	I2C1_SDA #1	
22	PB12	DAC0_OUT1 / OPAMP_OUT1	LETIM0_OUT1 #1	I2C1_SCL #1	
23	AVDD_1	Analog power supply 1.			
24	PB13	HFX TAL_P		US0_CLK #4/5 LEU0_TX #1	
25	PB14	HFX TAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12						I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exit output 0.
LES_ALTEX1	PD7							LESENSE alternate exit output 1.
LES_ALTEX2	PA3							LESENSE alternate exit output 2.
LES_ALTEX3	PA4							LESENSE alternate exit output 3.
LES_ALTEX4	PA5							LESENSE alternate exit output 4.
LES_ALTEX5	PE11							LESENSE alternate exit output 5.
LES_ALTEX6	PE12							LESENSE alternate exit output 6.
LES_ALTEX7	PE13							LESENSE alternate exit output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN			PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4							Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5							Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.

Figure 5.2. QFN64 PCB Solder Mask

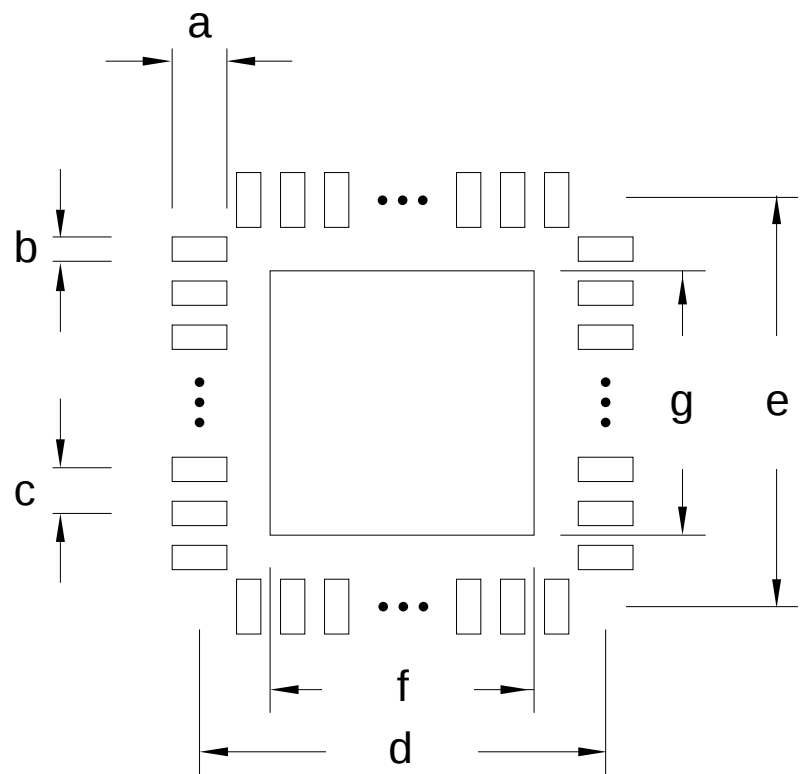


Table 5.2. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

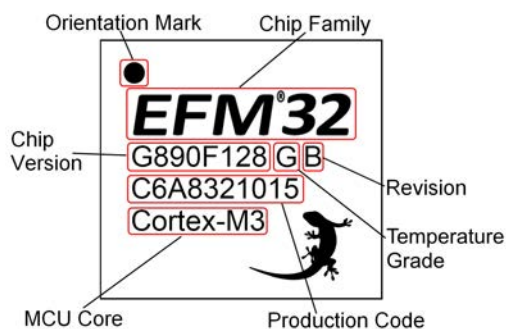
Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.97	e	8.90
b	0.42	f	7.32
c	0.50	g	7.32
d	8.90	-	-

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

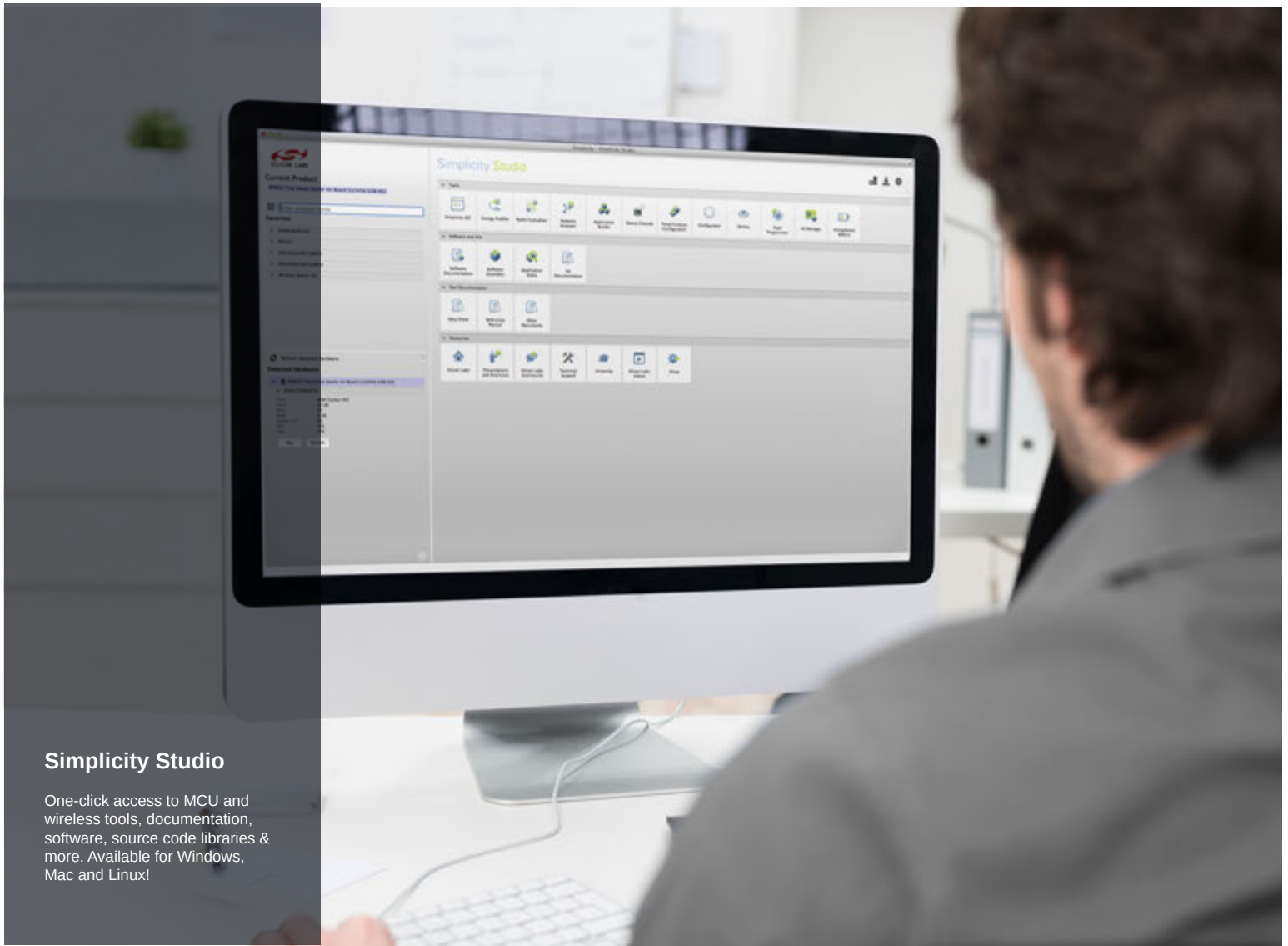
The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 62) .

6.3 Errata

Please see the errata document for EFM32GG330 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

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