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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	109
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFPGA
Supplier Device Package	132-UFPGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l471qei6

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L471xx microcontrollers.

This document should be read in conjunction with the STM32L4x1 reference manual (RM0392). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.



Table 2. STM32L471xx family device features and peripheral counts

Peripheral		STM32L471Zx		STM32L471Qx		STM32L471Vx		STM32L471Rx	
Flash memory		512KB	1MB	512KB	1MB	512KB	1MB	512KB	1MB
SRAM		128KB							
External memory controller for static memories		Yes		Yes		Yes ⁽¹⁾		No	
Quad SPI		Yes							
Timers	Advanced control	2 (16-bit)							
	General purpose	5 (16-bit) 2 (32-bit)							
	Basic	2 (16-bit)							
	Low -power	2 (16-bit)							
	SysTick timer	1							
	Watchdog timers (independent, window)	2							
Comm. interfaces	SPI	3							
	I ² C	3							
	USART UART LPUART	3 2 1							
	SAI	2							
	CAN	1							
	SDMMC	Yes							
	SWPMI	Yes							
Digital filters for sigma-delta modulators		Yes (4 filters)							
Number of channels		8							
RTC		Yes							
Tamper pins		3 2							
Random generator		Yes							
GPIOs		114		109		82		51	
Wakeup pins		5		5		5		4	
Nb of I/Os down to 1.08 V		14		14		0		0	
Capacitive sensing		24		24		21		12	
Number of channels									
12-bit ADCs		3		3		3		3	
Number of channels		24		19		16		16	
12-bit DAC channels		2							
Internal voltage reference buffer		Yes						No	
Analog comparator		2							
Operational amplifiers		2							
Max. CPU frequency		80 MHz							
Operating voltage		1.71 to 3.6 V							

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

STM32L471xx devices feature up to 128 Kbyte of embedded SRAM. This SRAM is split into two blocks:

- 96 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 32 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

This block is accessed through the ICode/DCode buses for maximum performance. These 32 Kbyte SRAM can also be retained in Standby mode.

The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
 - Code segment (located in Flash or SRAM1 if defined as executable protected area)
 - Non-volatile data segment (located in Flash)
 - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
 - code segment: up to 1024 Kbyte with granularity of 256 bytes
 - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
 - Volatile data segment: up to 96 Kbyte with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

Table 4. STM32L471 modes overview (continued)

Mode	Regulator ⁽¹⁾	CPU	Flash	SRAM	Clocks	DMA & Peripherals ⁽²⁾	Wakeup source	Consumption ⁽³⁾	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5) ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...3) ⁽⁷⁾ LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5) ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...3) ⁽⁷⁾ LPTIMx (x=1,2) SWPMI1 ⁽⁸⁾	6.6 μ A w/o RTC 6.9 μ A w RTC	4 μ s in SRAM 6 μ s in Flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3 ⁽⁷⁾ LPUART1 ⁽⁶⁾ LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3 ⁽⁷⁾ LPUART1 ⁽⁶⁾ LPTIM1	1.1 μ A w/o RTC 1.4 μ A w/RTC	5 μ s in SRAM 7 μ s in Flash

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see [Table 16](#)) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port E	PE0	-	-	-	-	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	-	-	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	-	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	-	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	-	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	-	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	-	-	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	QUADSPI_NCS	-	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	QUADSPI_BK1_IO0	-	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	QUADSPI_BK1_IO1	-	FMC_D10	-	-	EVENTOUT
	PE14	-	-	QUADSPI_BK1_IO2	-	FMC_D11	-	-	EVENTOUT
	PE15	-	-	QUADSPI_BK1_IO3	-	FMC_D12	-	-	EVENTOUT

Table 18. STM32L471xx memory map and peripheral register boundary addresses (continued)⁽¹⁾

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved
	0x4000 5C00 - 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 58: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 40: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

Table 63. ADC characteristics^{(1) (2)} (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	$f_{ADC} = 80 \text{ MHz}$	0.03125	-	8.00625	μs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	μs
t_{CONV}	Total conversion time (including sampling time)	$f_{ADC} = 80 \text{ MHz}$ Resolution = 12 bits	0.1875	-	8.1625	μs
		Resolution = 12 bits	$t_s + 12.5 \text{ cycles for successive approximation} = 15 \text{ to } 653$			$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the V_{DDA} supply	$f_s = 5 \text{ Msps}$	-	730	830	μA
		$f_s = 1 \text{ Msps}$	-	160	220	
		$f_s = 10 \text{ ksps}$	-	16	50	
$I_{DDV_S}(ADC)$	ADC consumption from the V_{REF+} single ended mode	$f_s = 5 \text{ Msps}$	-	130	160	μA
		$f_s = 1 \text{ Msps}$	-	30	40	
		$f_s = 10 \text{ ksps}$	-	0.6	2	
$I_{DDV_D}(ADC)$	ADC consumption from the V_{REF+} differential mode	$f_s = 5 \text{ Msps}$	-	260	310	μA
		$f_s = 1 \text{ Msps}$	-	60	70	
		$f_s = 10 \text{ ksps}$	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4 \text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4 \text{ V}$). It is disable when $V_{DDA} \geq 2.4 \text{ V}$.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA} , depending on the package. Refer to [Section 4: Pinouts and pin description](#) for further details.

Table 70. DAC accuracy⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain	Gain error ⁽⁵⁾	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL	-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL	-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz	-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz	-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	-79	-	
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2) V when buffer is ON.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 40. Synchronous multiplexed NOR/PSRAM read timings

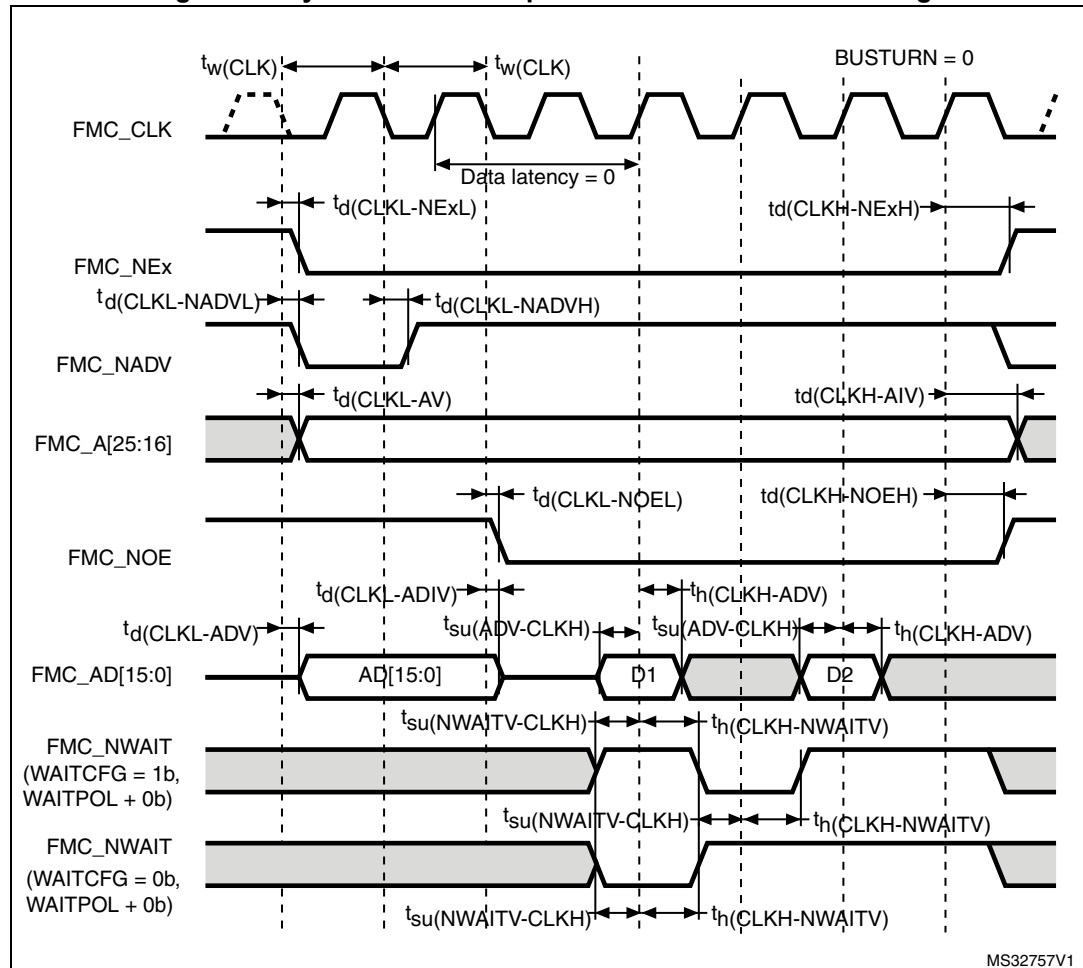


Figure 41. Synchronous multiplexed PSRAM write timings

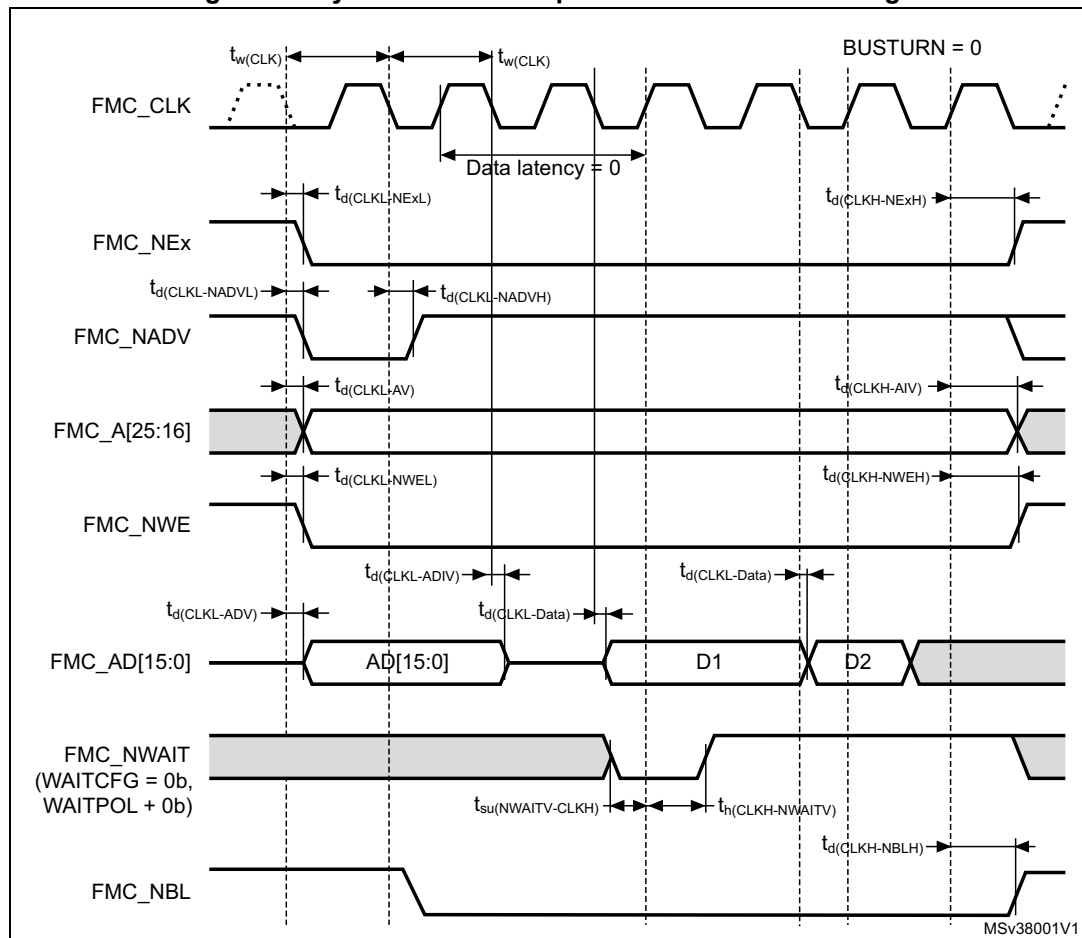


Figure 44. NAND controller waveforms for read access

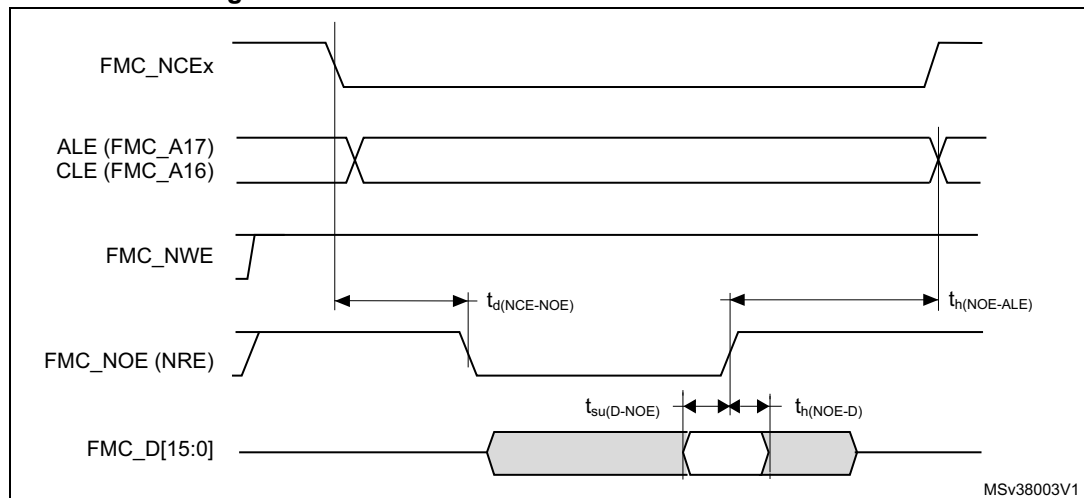


Figure 45. NAND controller waveforms for write access

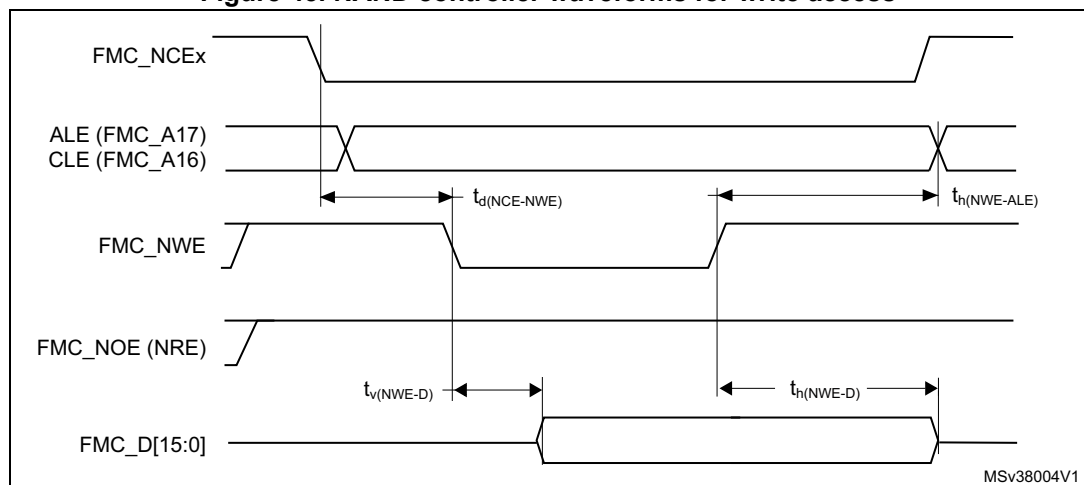


Figure 46. NAND controller waveforms for common memory read access

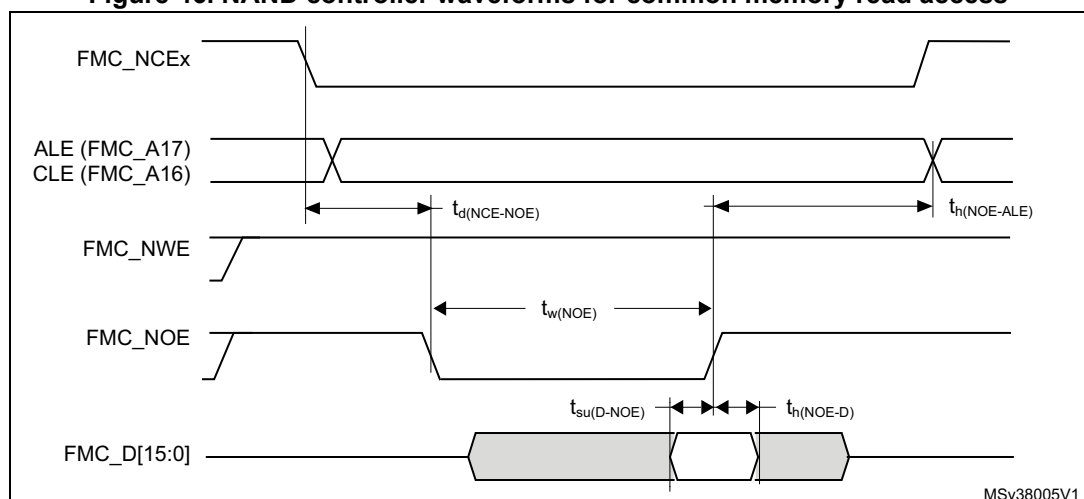
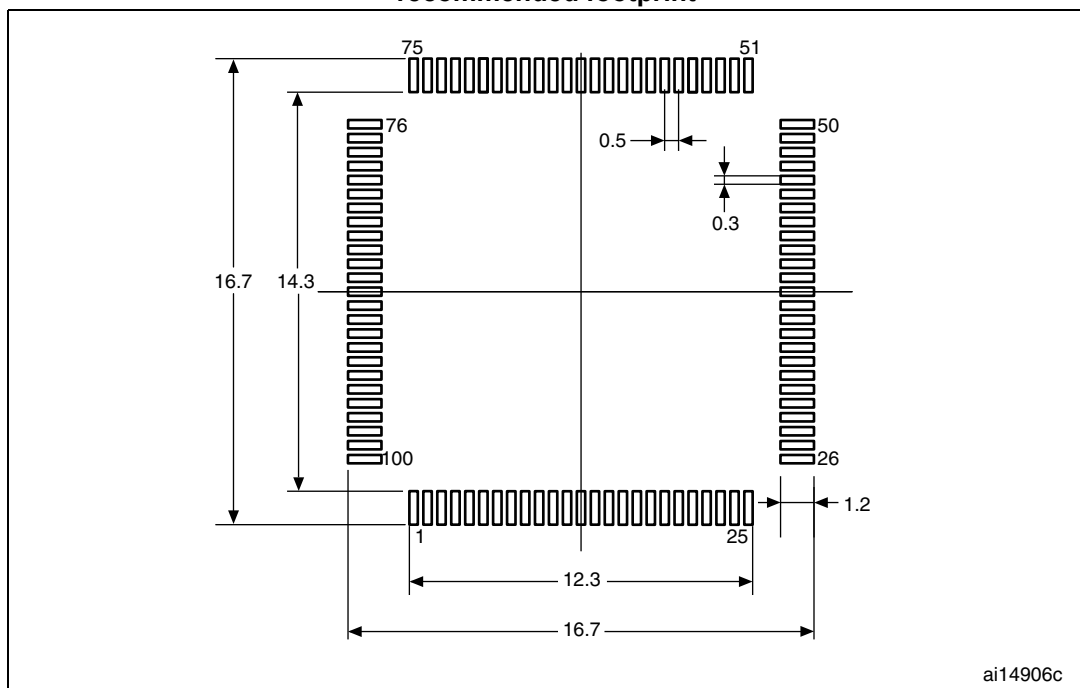


Table 105. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 55. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

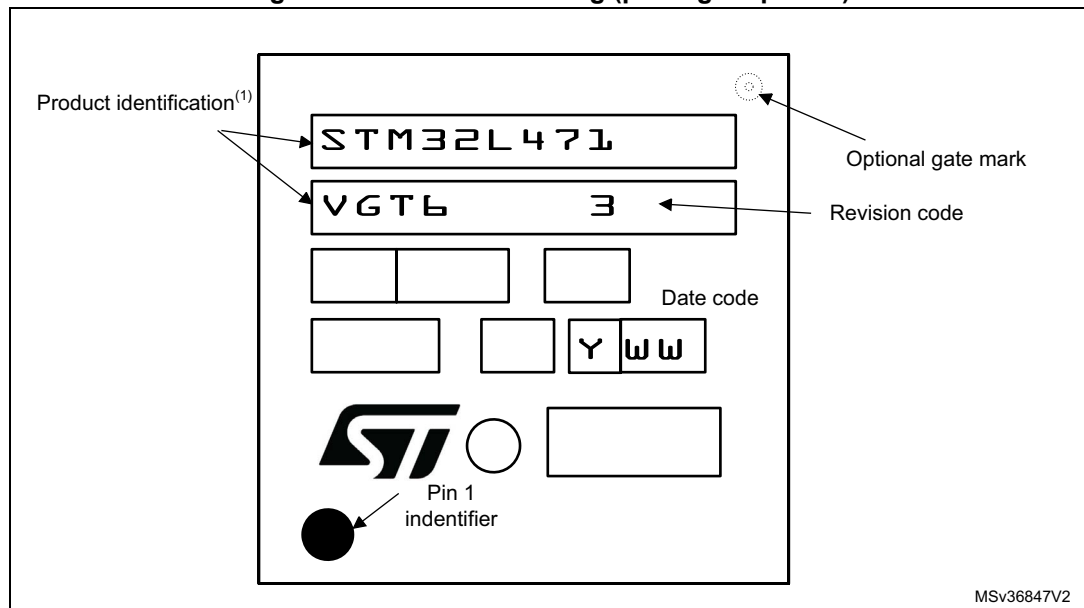


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

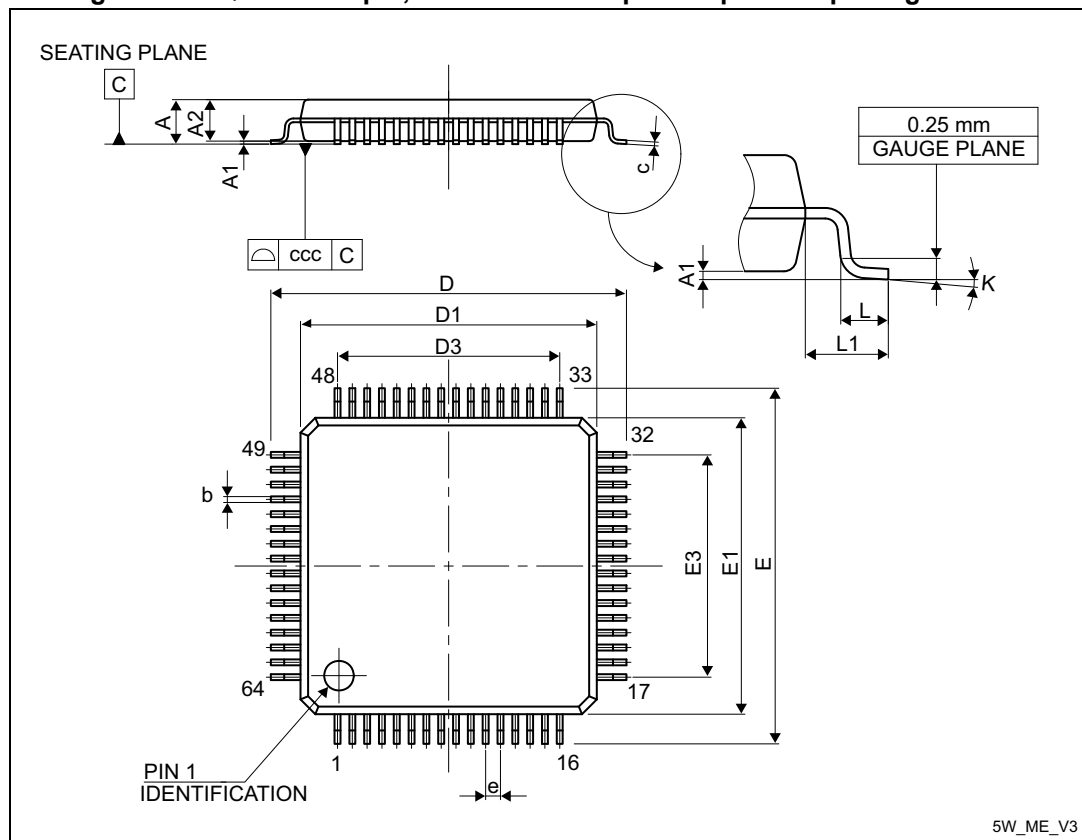
Figure 56. LQFP100 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP64 package information

Figure 57. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-