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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	109
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFPGA
Supplier Device Package	132-UFPGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l471qei7

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2 Description

The STM32L471xx devices are the ultra-low-power microcontrollers based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L471xx devices embed high-speed memories (Flash memory up to 1 Mbyte, up to 128 Kbyte of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L471xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer up to three fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM).

In addition, up to 24 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Three I2Cs
- Three SPIs
- Three USARTs, two UARTs and one Low-Power UART.
- Two SAIs (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One SWPMI (Single Wire Protocol Master Interface)

The STM32L471xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, and up to 14 I/Os can be supplied independently down to 1.08V. A VBAT input allows to backup the RTC and backup registers.

The STM32L471xx family offers four packages from 64-pin to 144-pin packages.

3.4 Embedded Flash memory

STM32L471xx devices feature up to 1 Mbyte of embedded Flash memory available for storing programs and data. The Flash memory is divided into two banks allowing read-while-write operations. This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
 - Level 0: no readout protection
 - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
 - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A ⁽¹⁾	No	No	N/A ⁽¹⁾
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes ⁽¹⁾	No	No	No ⁽¹⁾
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. One area per bank can be selected, with 64-bit granularity. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

Table 13. SAI implementation

SAI features ⁽¹⁾	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO Size	X (8 Word)	X (8 Word)
SPDIF	X	X

1. X: supported

3.30 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.31 Controller area network (CAN)

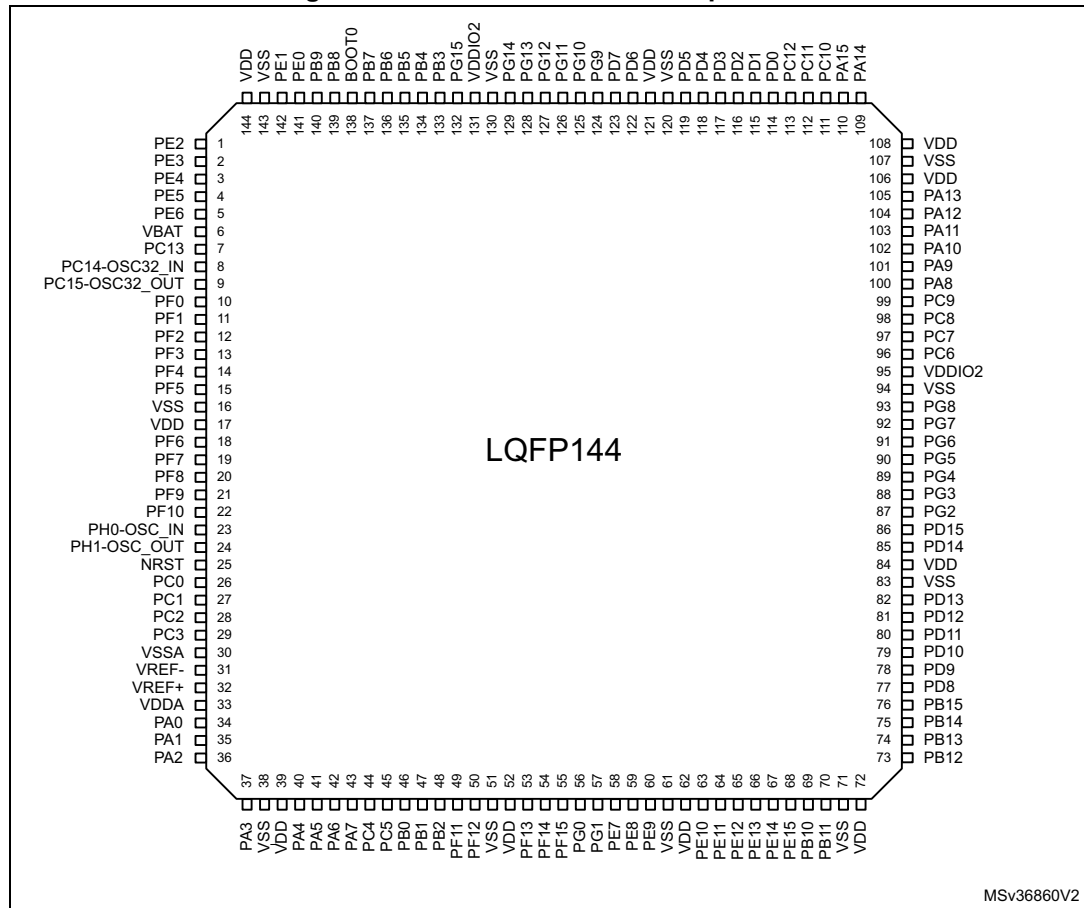
The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s

4 Pinouts and pin description

Figure 5. STM32L471Zx LQFP144 pinout⁽¹⁾



1. The above figure shows the package top view.

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see [Table 17](#)) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = V_{DDA} = 3\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

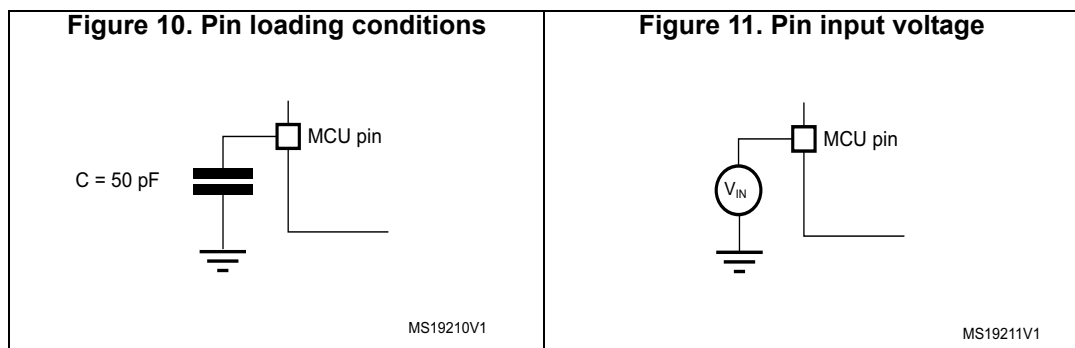
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 10](#).

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 11](#).



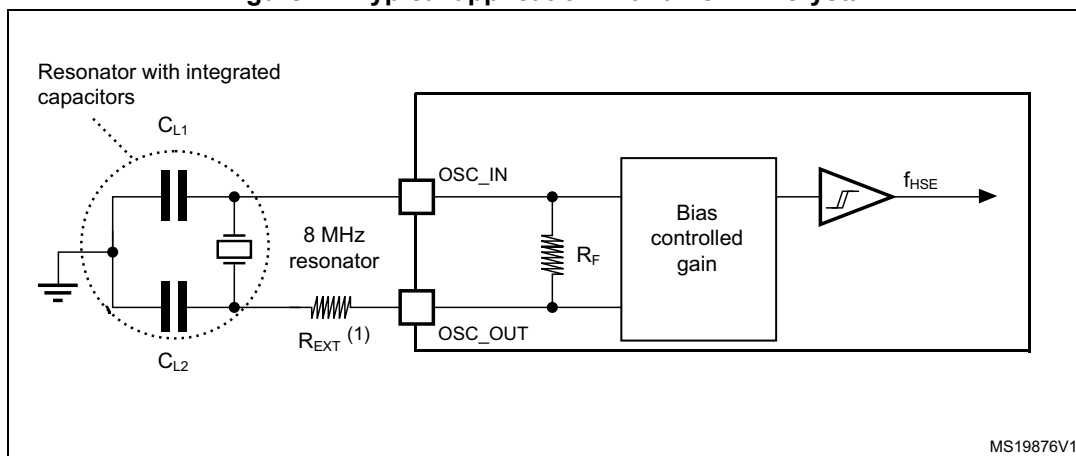
**Table 26. Current consumption in Run and Low-power run modes, code with data processing
running from Flash, ART enable (Cache ON Prefetch OFF)**

Symbol	Parameter	Conditions			TYP					MAX ⁽¹⁾					Unit
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I _{DD} (Run)	Supply current in Run mode	f _{HCLK} = f _{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.88	2.93	3.05	3.23	3.58	3.20	3.37	3.51	3.93	4.76	mA
				16 MHz	1.83	1.87	1.98	2.16	2.49	2.01	2.16	2.30	2.72	3.34	
				8 MHz	0.98	1.02	1.12	1.29	1.62	1.10	1.17	1.31	1.73	2.56	
				4 MHz	0.55	0.59	0.69	0.85	1.18	0.61	0.70	0.89	1.24	1.95	
				2 MHz	0.34	0.37	0.47	0.64	0.96	0.37	0.46	0.64	0.98	1.71	
				1 MHz	0.23	0.26	0.36	0.53	0.85	0.27	0.33	0.50	0.86	1.57	
				100 kHz	0.14	0.17	0.27	0.43	0.75	0.17	0.21	0.38	0.74	1.44	
			Range 1	80 MHz	10.2	10.3	10.5	10.7	11.1	11.22	11.8	12.1	12.5	13.3	
				72 MHz	9.24	9.31	9.47	9.69	10.1	10.16	10.7	11.0	11.4	12.2	
				64 MHz	8.25	8.32	8.46	8.68	9.09	9.08	9.6	9.9	10.3	11.1	
				48 MHz	6.28	6.35	6.5	6.72	7.11	6.91	7.3	7.6	8.0	8.8	
				32 MHz	4.24	4.30	4.44	4.65	5.04	4.66	4.97	5.26	5.67	6.51	
				24 MHz	3.21	3.27	3.4	3.61	3.98	3.53	3.76	4.05	4.46	5.30	
				16 MHz	2.19	2.24	2.36	2.56	2.94	2.41	2.66	2.95	3.16	3.99	
I _{DD} (LPRun)	Supply current in Low-power run mode	f _{HCLK} = f _{MSI} all peripherals disable		2 MHz	272	303	413	592	958	330	393	579	954	1704	μA
				1 MHz	154	184	293	473	835	195	265	457	822	1572	
				400 kHz	78	108	217	396	758	110	180	380	755	1505	
				100 kHz	42	73	182	360	723	75	138	331	706	1456	

1. Guaranteed by characterization results, unless otherwise specified.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

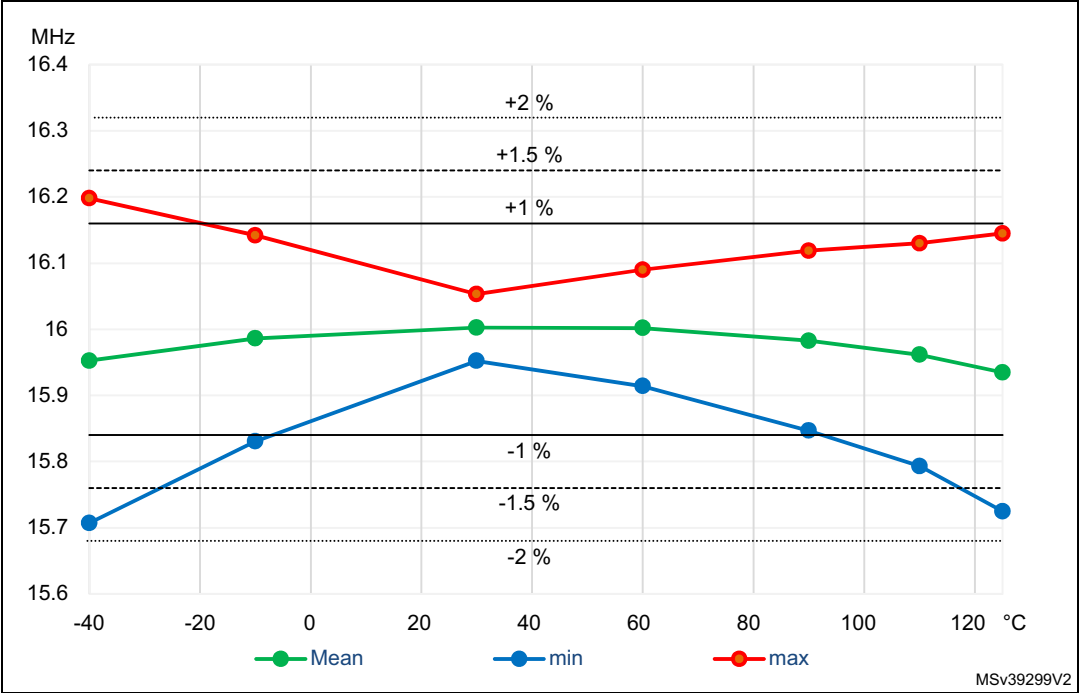
Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 46](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 46. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$G_{m_{critmax}}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	$\mu A/V$
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	s

Figure 19. HSI16 frequency versus temperature



6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 53](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 53. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 80\text{ MHz}$, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 80\text{ MHz}$, conforming to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 56. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A	II level A ⁽¹⁾

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$ range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 57](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

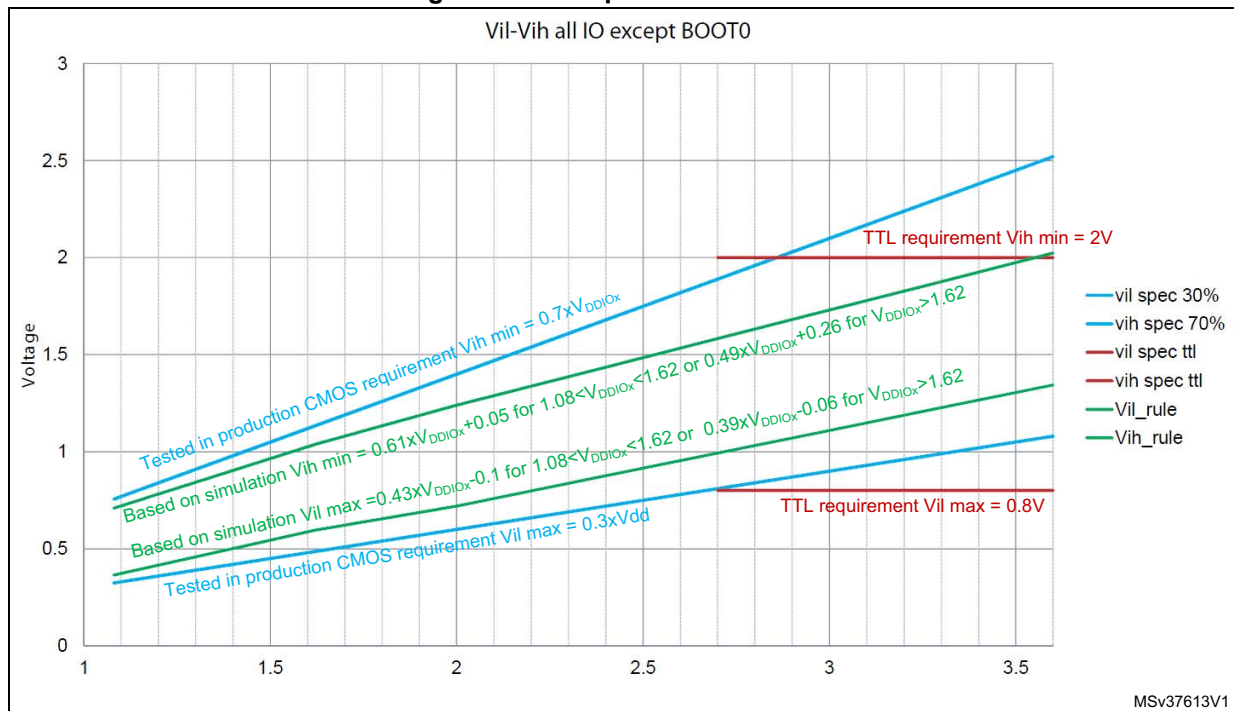
Table 57. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	-0	NA ⁽¹⁾	mA
	Injected current on pins except PA4, PA5, BOOT0	-5	NA ⁽¹⁾	
	Injected current on PA4, PA5 pins	-5	0	

1. NA: not applicable

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 21](#) for standard I/Os, and in [Figure 21](#) for 5 V tolerant I/Os.

Figure 21. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DDIOX} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 19: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 19: Voltage characteristics](#)).

1. Guaranteed by design, unless otherwise specified.
2. Refer to [Table 25: Embedded internal voltage reference](#).
3. Guaranteed by characterization results.

6.3.21 Operational amplifiers characteristics

Table 73. OPAMP characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage ⁽²⁾	-		1.8	-	3.6	V
CMIR	Common mode input range	-		0	-	V _{DDA}	V
V _I OFFSET	Input offset voltage	25 °C, No Load on output.		-	-	±1.5	mV
		All voltage/Temp.		-	-	±3	
ΔV _I OFFSET	Input offset voltage drift	Normal mode		-	±5	-	μV/°C
		Low-power mode		-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 × V _{DDA})	-		-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 × V _{DDA})	-		-	1	1.35	
I _{LOAD}	Drive current	Normal mode	V _{DDA} ≥ 2 V	-	-	500	μA
		Low-power mode		-	-	100	
I _{LOAD_PGA}	Drive current in PGA mode	Normal mode	V _{DDA} ≥ 2 V	-	-	450	
		Low-power mode		-	-	50	
R _{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	V _{DDA} < 2 V	4	-	-	kΩ
		Low-power mode		20	-	-	
R _{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to VDDA)	Normal mode	V _{DDA} < 2 V	4.5	-	-	
		Low-power mode		40	-	-	
C _{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	

Table 73. OPAMP characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{network}	R2/R1 internal resistance values in PGA mode ⁽⁵⁾	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/40	-	
		PGA Gain = 8		-	140/20	-	
		PGA Gain = 16		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/2	-	MHz
		Gain = 4	-	-	GBW/4	-	
		Gain = 8	-	-	GBW/8	-	
		Gain = 16	-	-	GBW/16	-	
e_n	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
$I_{\text{DDA(OPAMP)}}^{(3)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	μA
		Low-power mode		-	45	100	

1. Guaranteed by design, unless otherwise specified.

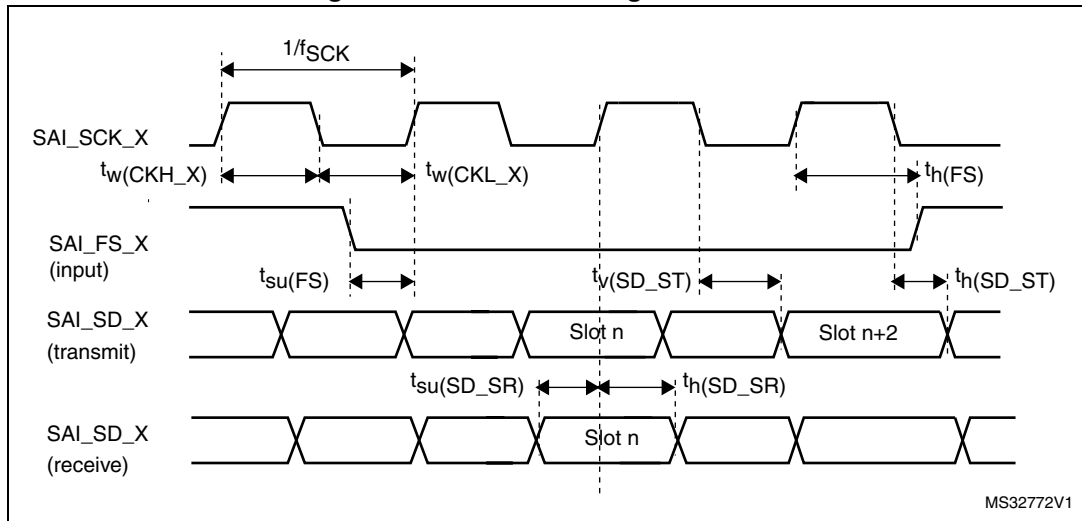
2. The temperature range is limited to 0 °C-125 °C when V_{DDA} is below 2 V

3. Guaranteed by characterization results.

4. Mostly I/O leakage, when used in analog mode. Refer to I_{lk} parameter in [Table 58: I/O static characteristics](#).

5. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain = $1+R2/R1$

Figure 33. SAI slave timing waveforms



MS32772V1

SDMMC characteristics

Unless otherwise specified, the parameters given in [Table 86](#) for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 22: General operating conditions](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 11$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output characteristics.

Table 86. SD / MMC dynamic characteristics, $V_{DD}=2.7$ V to 3.6 V⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	$f_{PP} = 50$ MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	$f_{PP} = 50$ MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	$f_{PP} = 50$ MHz	2	-	-	ns
t_{IH}	Input hold time HS	$f_{PP} = 50$ MHz	4.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	$f_{PP} = 50$ MHz	-	12	14	ns
t_{OH}	Output hold time HS	$f_{PP} = 50$ MHz	9	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	$f_{PP} = 50$ MHz	2	-	-	ns
t_{IHD}	Input hold time SD	$f_{PP} = 50$ MHz	4.5	-	-	ns

6.3.27 FSMC characteristics

Unless otherwise specified, the parameters given in [Table 88](#) to [Table 101](#) for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in [Table 22](#), with the following configuration:

- Output speed is set to $\text{OSPEEDRy}[1:0] = 11$
- Capacitive load $C = 30 \text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{\text{DD}}$

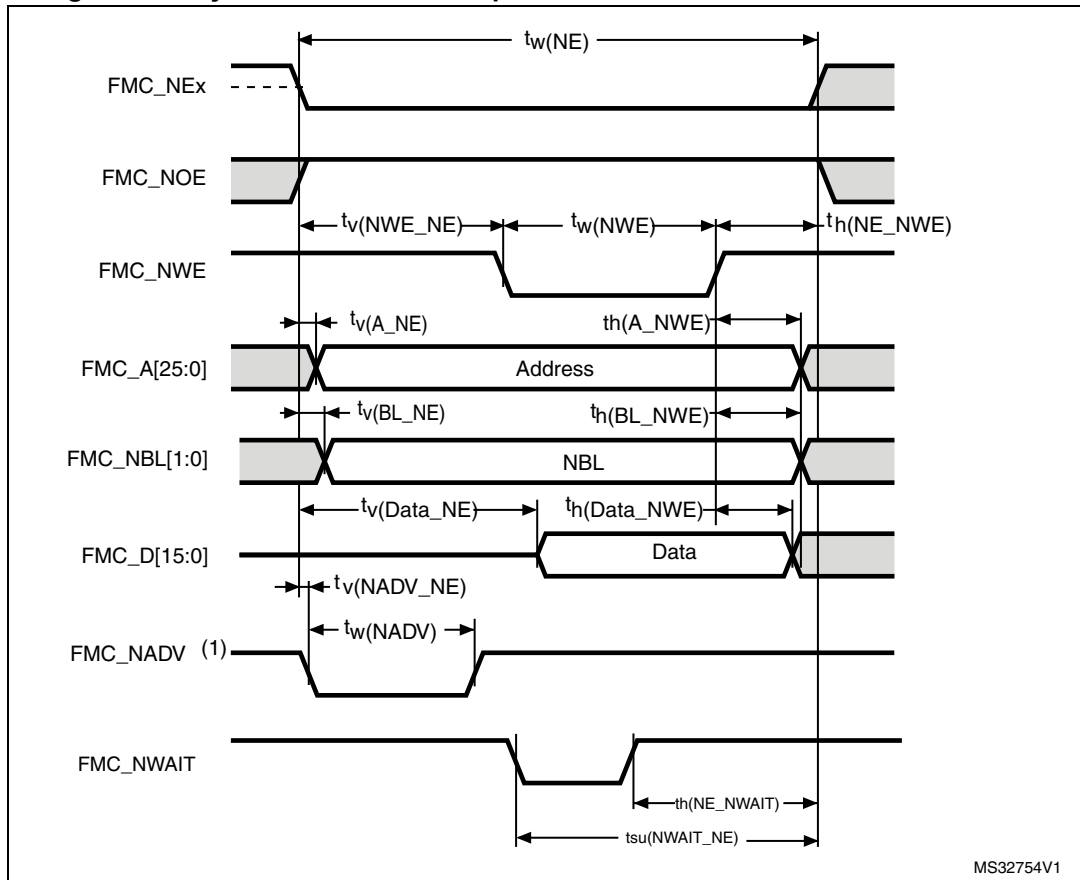
Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output characteristics.

Asynchronous waveforms and timings

[Figure 36](#) through [Figure 39](#) represent asynchronous waveforms and [Table 88](#) through [Table 95](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- $\text{AddressSetupTime} = 0x1$
- $\text{AddressHoldTime} = 0x1$
- $\text{DataSetupTime} = 0x1$ (except for asynchronous NWAIT mode, $\text{DataSetupTime} = 0x5$)
- $\text{BusTurnAroundDuration} = 0x0$

In all timing tables, the THCLK is the HCLK clock period.

Figure 37. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings⁽¹⁾⁽²⁾**

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FMC_NE low time	$3T_{HCLK}-1$	$3T_{HCLK}+2$	ns
$t_v(NWE_NE)$	FMC_NEx low to FMC_NWE low	$T_{HCLK}-0.5$	$T_{HCLK}+1.5$	
$t_w(NWE)$	FMC_NWE low time	$T_{HCLK}-1$	$T_{HCLK}+1$	
$t_h(NE_NWE)$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK}-0.5$	-	
$t_v(A_NE)$	FMC_NEx low to FMC_A valid	-	0	
$t_h(A_NWE)$	Address hold time after FMC_NWE high	$T_{HCLK}-1$	-	
$t_v(BL_NE)$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_h(BL_NWE)$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}-0.5$	-	
$t_v(Data_NE)$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+4$	
$t_h(Data_NWE)$	Data hold time after FMC_NWE high	$T_{HCLK}+1$	-	
$t_v(NADV_NE)$	FMC_NEx low to FMC_NADV low	-	1	
$t_w(NADV)$	FMC_NADV low time	-	$T_{HCLK}+0.5$	

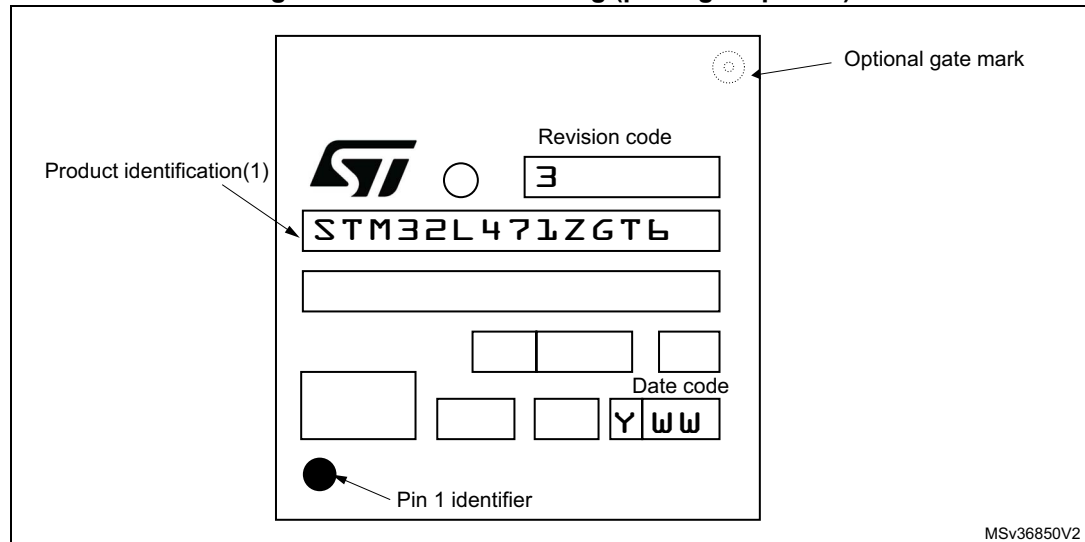
1. CL = 30 pF.

2. Guaranteed by characterization results.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 50. LQFP144 marking (package top view)



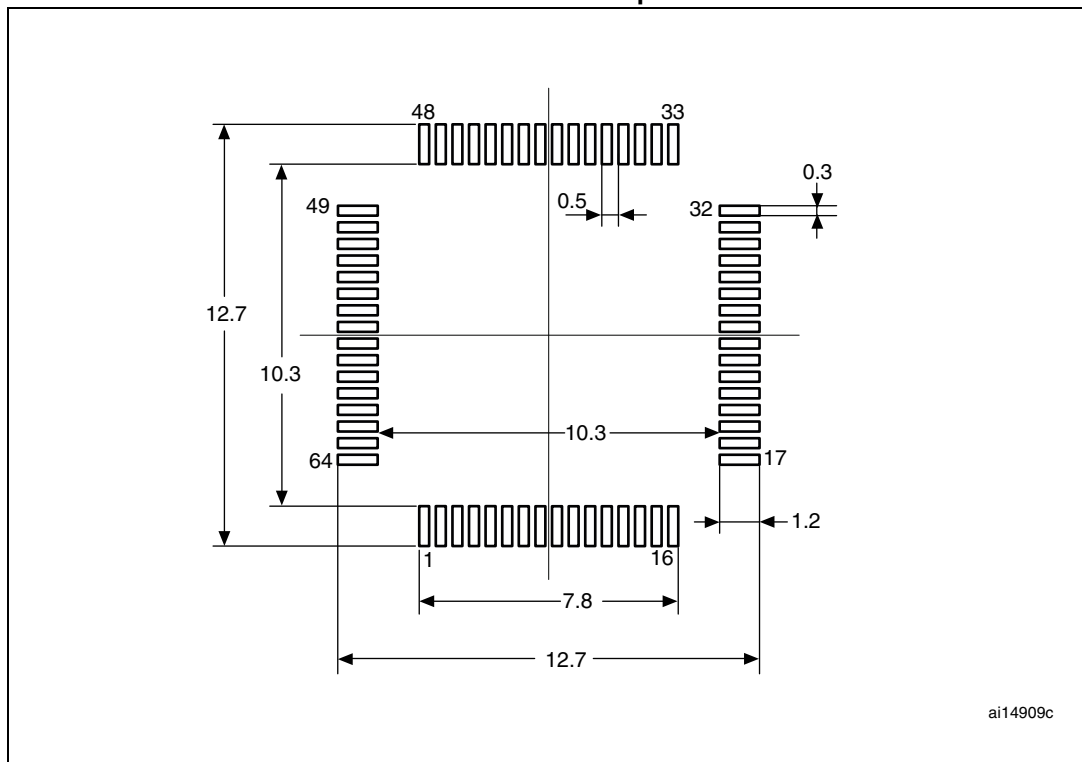
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 58. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.