Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l471rgt6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L471xx microcontrollers.

This document should be read in conjunction with the STM32L4x1 reference manual (RM0392). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.23.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.23.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32L471 (see *Table 10* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.23.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.23.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

3.26 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L471xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode.The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 12. STM32L4x1 USART/UART/LPUART features

USART modes/features[1]	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	40	M8	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	-	F6	61	VSS	S	-	-	-	-
-	-	G6	62	VDD	S	-	-	-	-
-	41	L8	63	PE10	I/O	FT	-	TIM1_CH2N, DFSDM_DATIN4, TSC_G5_IO1, QUADSPI_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	42	M9	64	PE11	I/O	FT	-	TIM1_CH2, DFSDM_CKIN4, TSC_G5_IO2, QUADSPI_NCS, FMC_D8, EVENTOUT	-
-	43	L9	65	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	44	M10	66	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-
-	45	M11	67	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	-
-	46	M12	68	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	-	I2C3_SMBA	-	-	-
	PG7	-	-	-	-	I2C3_SCL	-	-	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	-	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_ DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

Table 18. STM32L471xx memory map and peripheral register boundary addresses (continued)(1)

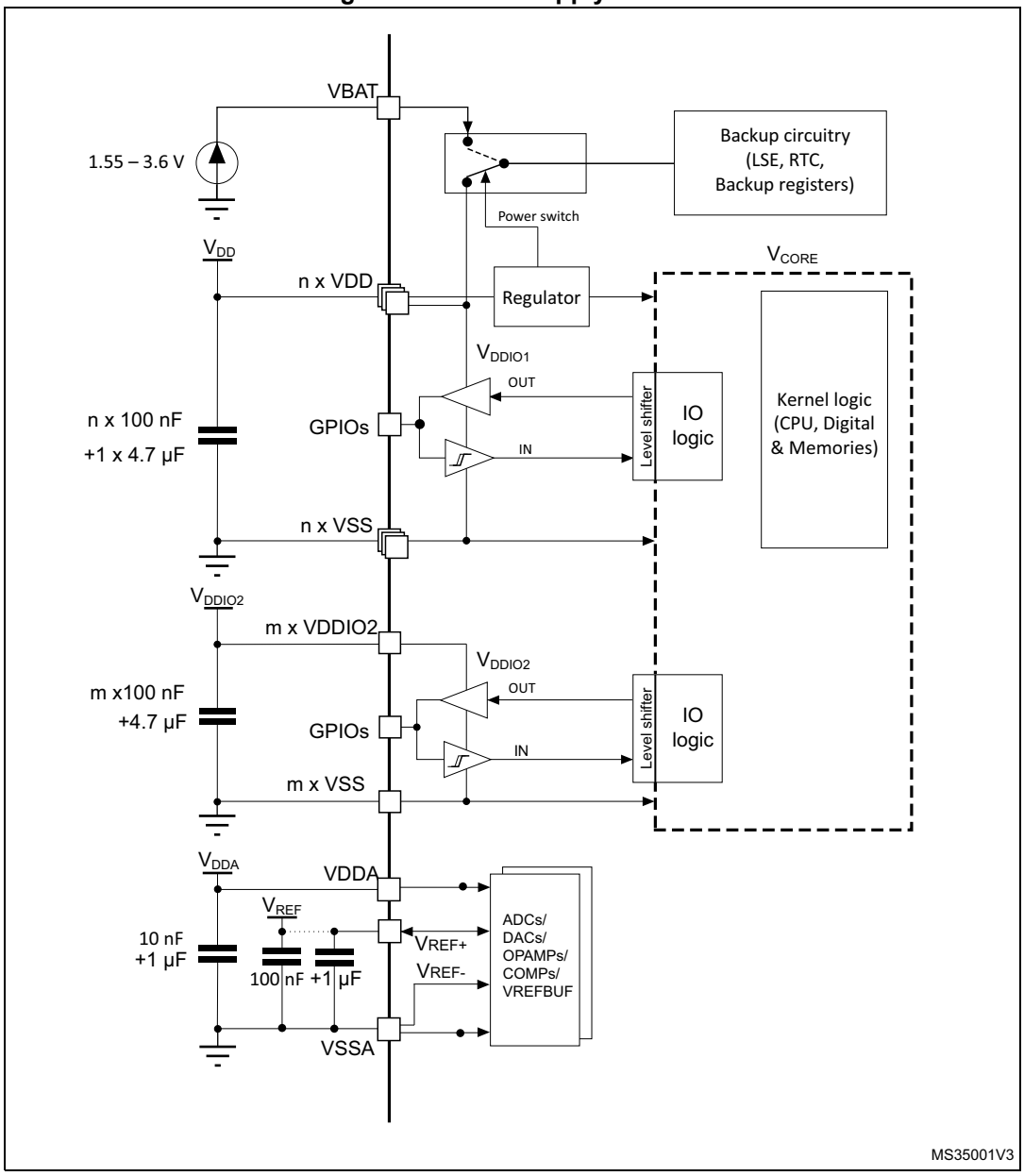
Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 6400 - 0x4001 FFFF	39 KB	Reserved
	0x4001 6000 - 0x4000 63FF	1 KB	DFSDM
	0x4001 5C00 - 0x4000 5FFF	1 KB	Reserved
	0x4001 5800 - 0x4000 5BFF	1 KB	SAI2
	0x4001 5400 - 0x4000 57FF	1 KB	SAI1
	0x4001 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
APB2	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	SDMMC1
	0x4001 2000 - 0x4001 27FF	2 KB	Reserved
	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800- 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG

Table 18. STM32L471xx memory map and peripheral register boundary addresses (continued)(1)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2

6.1.6 Power supply scheme

Figure 12. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 58: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 40: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Low-speed internal (LSI) RC oscillator

Table 49. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, TA = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)^{(2)}$	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI)^{(2)}$	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)^{(2)}$	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 50* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 50. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2.0645	-	80	MHz
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	64	-	344	MHz
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
$I_{DD}(PLL)$	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	150	200	µA
		VCO freq = 96 MHz	-	200	260	
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.

2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

Table 58. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	FT_xx input leakage current(3)	$V_{IN} \le Max(V_{DDXXX})$(4)	-	-	±100	nA
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4)(5)	-	-	650(3)(6)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u and PC3 IO	$V_{IN} \le Max(V_{DDXXX})$ (4)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4)	-	-	2500(3)(7)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	$V_{IN} \le Max(V_{DDXXX})$(6)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN}$ < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current (UFBGA132 only)	T_J = 75 °C	-	-	1	
R_{PU}	Weak pull-up equivalent resistor (8)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 21: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table.*
5. All TX_xx IO except FT_lu, FT_u and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDIO2}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Table 66. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

6.3.18 Digital-to-Analog converter characteristics

Table 69. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.8	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 78. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 80 MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	0.0125	819.2	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	-	53.68	s

1. TIMx is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 79. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 80. WWDG min/max timeout value at 80 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0512	3.2768	ms
2	1	0.1024	6.5536	
4	2	0.2048	13.1072	
8	3	0.4096	26.2144	

Table 84. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		2 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc=0	$t_{(CK)}/2$-2	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2$+2	
$t_{sf(IN)}$;$t_{sr(IN)}$	Data input setup time	Voltage Range 1 and 2	3.5	-	-	
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time		6.5	-	-	
$t_{vf(OUT)}$;$t_{vr(OUT)}$	Data output valid time	Voltage Range 1	-	11	12	
		Voltage Range 2		15	19	
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Data output hold time	Voltage Range 1	6	-	-	
		Voltage Range 2	8	-		

1. Guaranteed by characterization results.

Figure 30. Quad SPI timing diagram - SDR mode

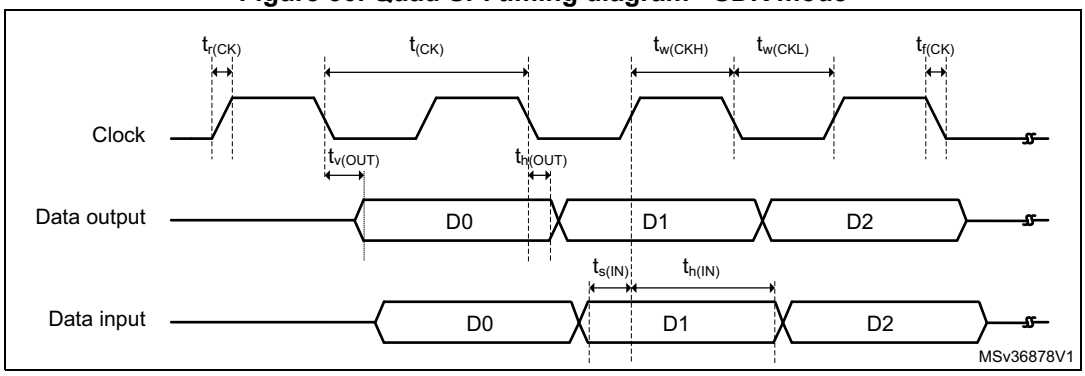


Figure 31. Quad SPI timing diagram - DDR mode

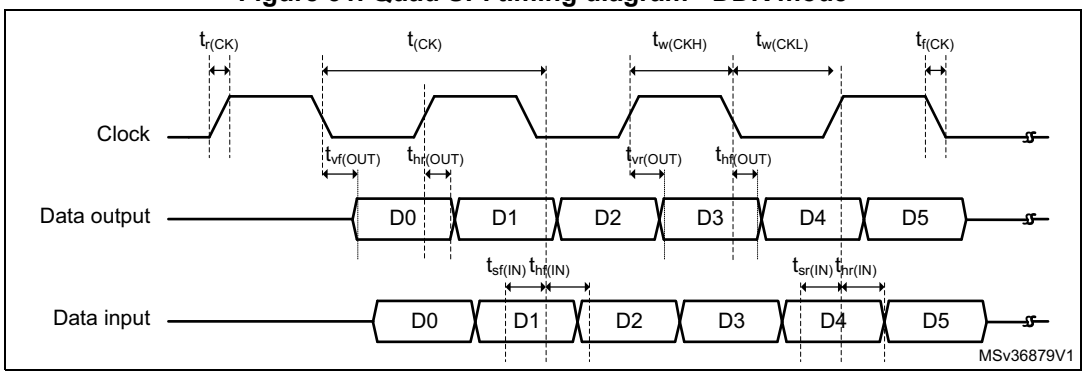


Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+0.5$	$8T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}-0.5$	$6T_{HCLK}+0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+2$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+2$	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 38. Asynchronous multiplexed PSRAM/NOR read waveforms

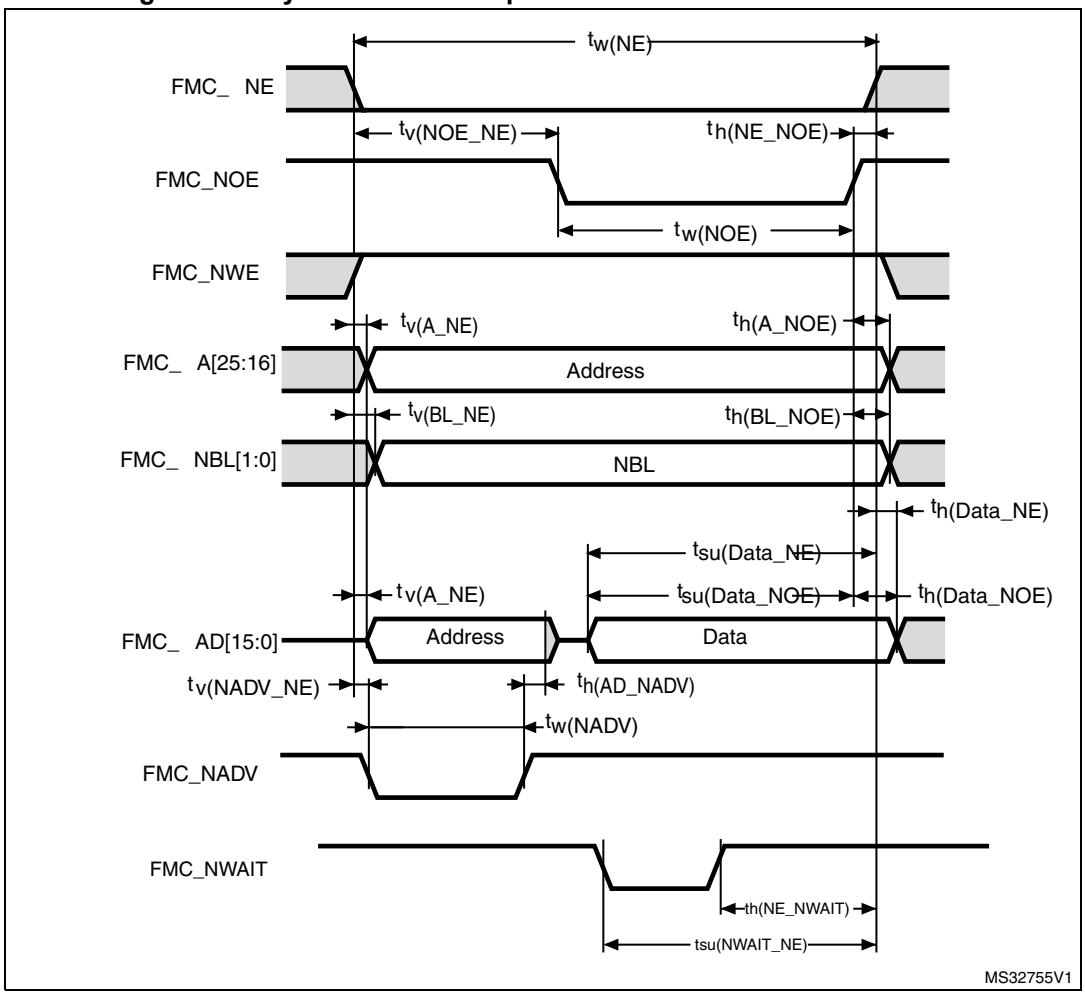


Table 97. Synchronous multiplexed PSRAM write timings(1)(2)

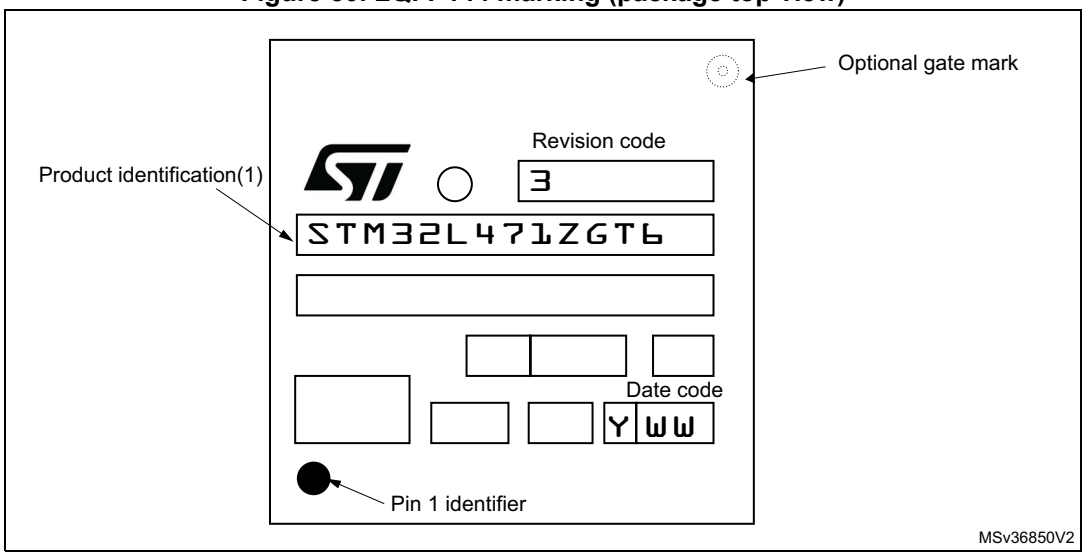
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	4	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	5.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2.5	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 50. LQFP144 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.