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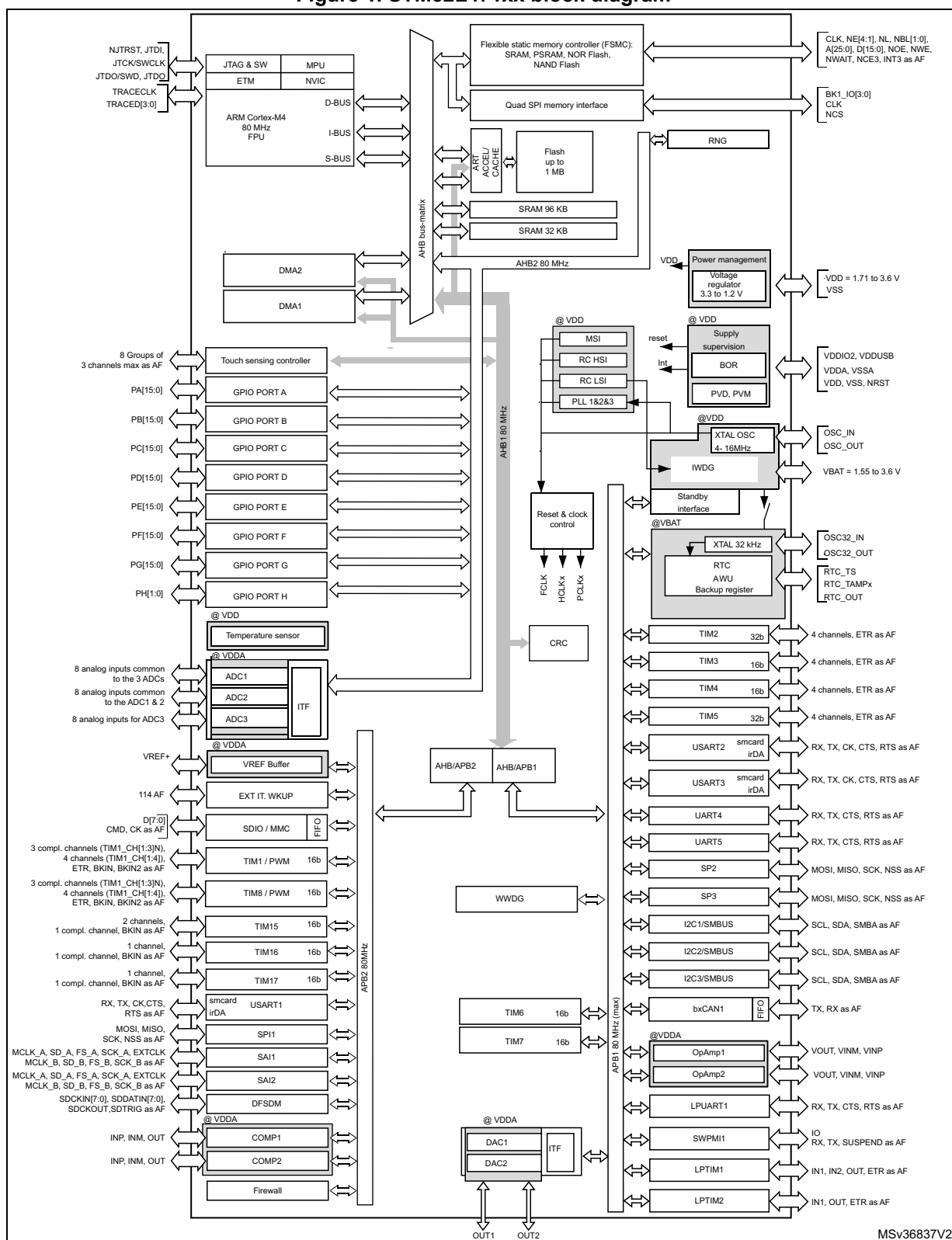
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l471vet6

Figure 1. STM32L471xx block diagram



Note: *AF: alternate function on I/O pins.*

3.21 Digital filter for Sigma-Delta Modulators (DFSDM)

The device embeds one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external $\Sigma\Delta$ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on $\Sigma\Delta$ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various $\Sigma\Delta$ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

Table 13. SAI implementation

SAI features ⁽¹⁾	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO Size	X (8 Word)	X (8 Word)
SPDIF	X	X

1. X: supported

3.30 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.31 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

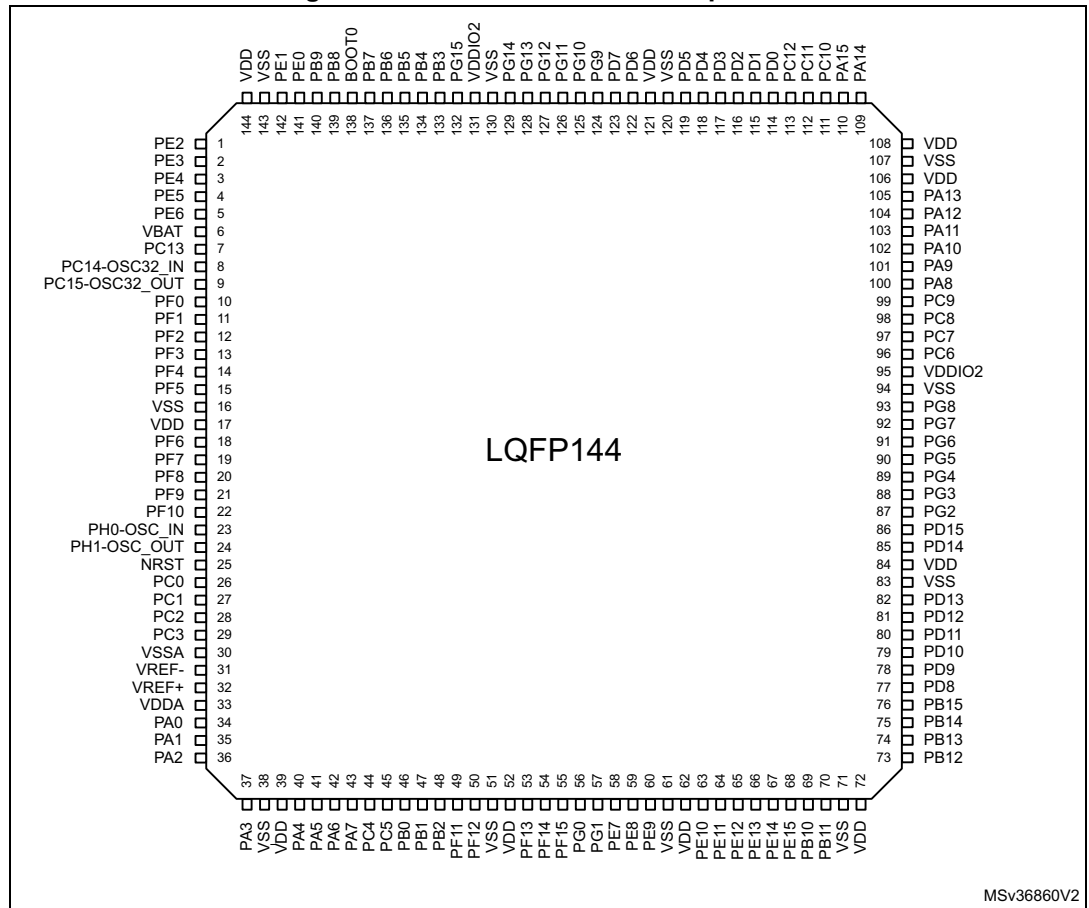
- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s

The Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
 - Instruction phase
 - Address phase
 - Alternate bytes phase
 - Dummy cycles phase
 - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

4 Pinouts and pin description

Figure 5. STM32L471Zx LQFP144 pinout⁽¹⁾



1. The above figure shows the package top view.

Table 15. STM32L471xx pin definitions

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	1	B2	1	PE2	I/O	FT	-	TRACECK, TIM3_ETR, TSC_G7_IO1, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	2	A1	2	PE3	I/O	FT	-	TRACED0, TIM3_CH1, TSC_G7_IO2, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	3	B1	3	PE4	I/O	FT	-	TRACED1, TIM3_CH2, DFSDM_DATIN3, TSC_G7_IO3, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	4	C2	4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM_CKIN3, TSC_G7_IO4, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	5	D2	5	PE6	I/O	FT	-	TRACED3, TIM3_CH4, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3/ WKUP3
1	6	E2	6	VBAT	S	-	-	-	-
2	7	C1	7	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
3	8	D1	8	PC14- OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	9	E1	9	PC15- OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	D6	10	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	D5	11	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	E4	13	PF3	I/O	FT_a	-	FMC_A3, EVENTOUT	ADC3_IN6
-	-	F3	14	PF4	I/O	FT_a	-	FMC_A4, EVENTOUT	ADC3_IN7
-	-	F4	15	PF5	I/O	FT_a	-	FMC_A5, EVENTOUT	ADC3_IN8
-	10	F2	16	VSS	S	-	-	-	-
-	11	G2	17	VDD	S	-	-	-	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	E9	90	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	-	G4	91	PG6	I/O	FT_s	-	I2C3_SMBA, LPUART1_RTS_DE, EVENTOUT	-
-	-	H4	92	PG7	I/O	FT_fs	-	I2C3_SCL, LPUART1_TX, FMC_INT3, EVENTOUT	-
-	-	J6	93	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	94	VSS	S	-	-	-	-
-	-	-	95	VDDIO2	S	-	-	-	-
37	63	E12	96	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM_CKIN3, TSC_G4_IO1, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
38	64	E11	97	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, DFSDM_DATIN3, TSC_G4_IO2, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
39	65	E10	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-
40	66	D12	99	PC9	I/O	FT	-	TIM8_BKIN2, TIM3_CH4, TIM8_CH4, TSC_G4_IO4, SDMMC1_D1, SAI2_EXTCLK, TIM8_BKIN2_COMP1, EVENTOUT	-
41	67	D11	100	PA8	I/O	FT	-	MCO, TIM1_CH1, USART1_CK, LPTIM2_OUT, EVENTOUT	-
42	68	D10	101	PA9	I/O	FT	-	TIM1_CH2, USART1_TX, TIM15_BKIN, EVENTOUT	-
43	69	C12	102	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, TIM17_BKIN, EVENTOUT	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see [Table 17](#)) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see [Table 17](#)) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	-	I2C3_SMBA	-	-	-
	PG7	-	-	-	-	I2C3_SCL	-	-	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	-	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_ DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see [Table 16](#)) (continued)

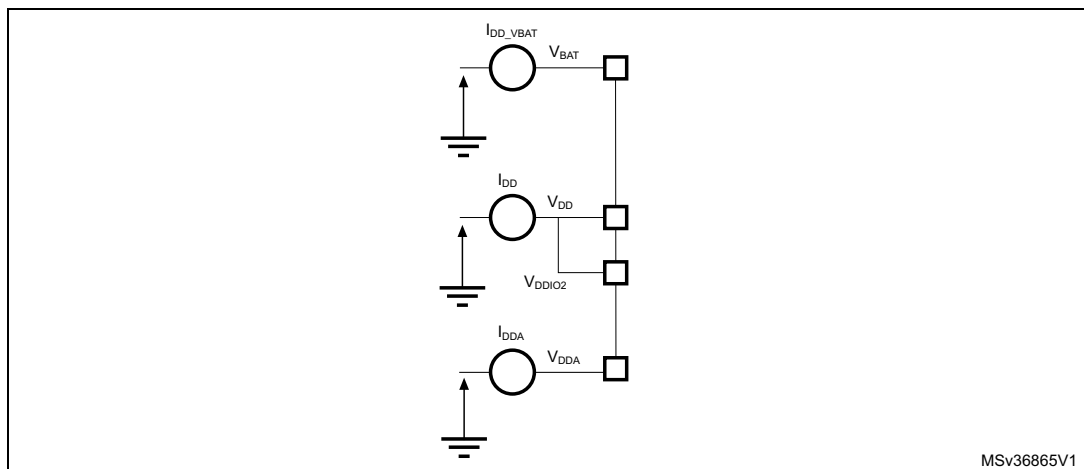
Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port E	PE0	-	-	-	-	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	-	-	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	-	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	-	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	-	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	-	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	-	-	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	QUADSPI_NCS	-	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	QUADSPI_BK1_IO0	-	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	QUADSPI_BK1_IO1	-	FMC_D10	-	-	EVENTOUT
	PE14	-	-	QUADSPI_BK1_IO2	-	FMC_D11	-	-	EVENTOUT
	PE15	-	-	QUADSPI_BK1_IO3	-	FMC_D12	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see [Table 16](#)) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_ CTS	-	-	-	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_ RTS_DE	-	-	-	-	-	-	EVENTOUT
	PG7	LPUART1_ TX	-	-	-	FMC_INT3	-	-	EVENTOUT
	PG8	LPUART1_ RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	FMC_NCE3/ FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	-	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	-	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	EVENTOUT

6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 19: Voltage characteristics](#), [Table 20: Current characteristics](#) and [Table 21: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD} , V_{DDA} , V_{DDIO2} , V_{BAT})	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT_XXX pins	$V_{SS}-0.3$	$\min(V_{DD}, V_{DDA}, V_{DDIO2}) + 4.0^{(3)(4)}$	V
	Input voltage on TT_XX pins	$V_{SS}-0.3$	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
	Input voltage on any other pins	$V_{SS}-0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different V_{DDx} power pins of the same domain	-	50	mV
$ V_{SSx}-V_{SS} $	Variations between all the different ground pins ⁽⁵⁾	-	50	mV

1. All main power (V_{DD} , V_{DDA} , V_{DDIO2} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 20: Current characteristics](#) for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 13: Current consumption measurement scheme](#).

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0392 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in [Table 26](#) to [Table 39](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22: General operating conditions](#).

6.3.8 Internal clock source characteristics

The parameters given in [Table 47](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22: General operating conditions](#). The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 47. HSI16 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	$V_{\text{DD}}=3.0\text{ V}$, $T_{\text{A}}=30\text{ }^{\circ}\text{C}$	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
$\text{DuCy}(\text{HSI16})^{(2)}$	Duty Cycle	-	45	-	55	%
$\Delta_{\text{Temp}}(\text{HSI16})$	HSI16 oscillator frequency drift over temperature	$T_{\text{A}}=0\text{ to }85\text{ }^{\circ}\text{C}$	-1	-	1	%
		$T_{\text{A}}=-40\text{ to }125\text{ }^{\circ}\text{C}$	-2	-	1.5	%
$\Delta_{\text{VDD}}(\text{HSI16})$	HSI16 oscillator frequency drift over V_{DD}	$V_{\text{DD}}=1.62\text{ V to }3.6\text{ V}$	-0.1	-	0.05	%
$t_{\text{su}}(\text{HSI16})^{(2)}$	HSI16 oscillator start-up time	-	-	0.8	1.2	μs
$t_{\text{stab}}(\text{HSI16})^{(2)}$	HSI16 oscillator stabilization time	-	-	3	5	μs
$I_{\text{DD}}(\text{HSI16})^{(2)}$	HSI16 oscillator power consumption	-	-	155	190	μA

1. Guaranteed by characterization results.

2. Guaranteed by design.

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 22: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 59. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	1.3	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 1.3$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 4 \text{ mA}$ $V_{DDIOx} \geq 1.62 \text{ V}$	-	0.45	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.45$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DDIOx} \geq 1.08 \text{ V}$	-	$0.35 \times V_{DDIOx}$	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$0.65 \times V_{DDIOx}$	-	
$V_{OLFM+}^{(3)}$	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	
		$ I_{IO} = 10 \text{ mA}$ $V_{DDIOx} \geq 1.62 \text{ V}$	-	0.4	
		$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DDIOx} \geq 1.08 \text{ V}$	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 19: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 22](#) and [Table 60](#), respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 22: General operating conditions](#).

Table 67. ADC accuracy - limited test conditions 3⁽¹⁾(2)(3) (continued)

Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency $\leq$ 80 MHz, Sampling rate $\leq$ 5.33 Msps, $1.65\text{ V} \leq V_{\text{DDA}} = V_{\text{REF+}} \leq 3.6\text{ V}$, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

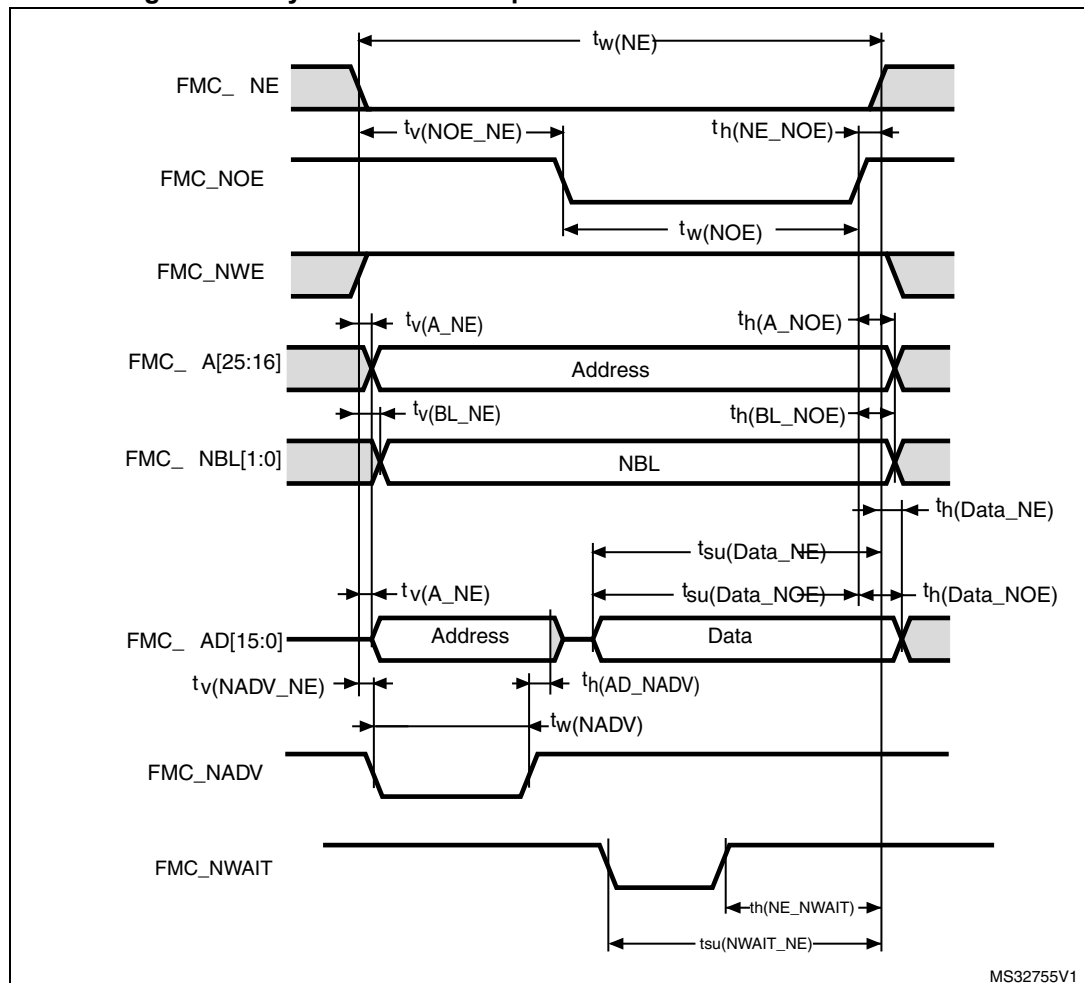
1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{\text{DDA}} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{\text{DDA}} < 2.4\text{ V}$). It is disable when $V_{\text{DDA}} \geq 2.4\text{ V}$. No oversampling.

Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+0.5$	$8T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}-0.5$	$6T_{HCLK}+0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+2$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+2$	-	

1. CL = 30 pF.

2. Guaranteed by characterization results.

Figure 38. Asynchronous multiplexed PSRAM/NOR read waveforms

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 43. Synchronous non-multiplexed PSRAM write timings

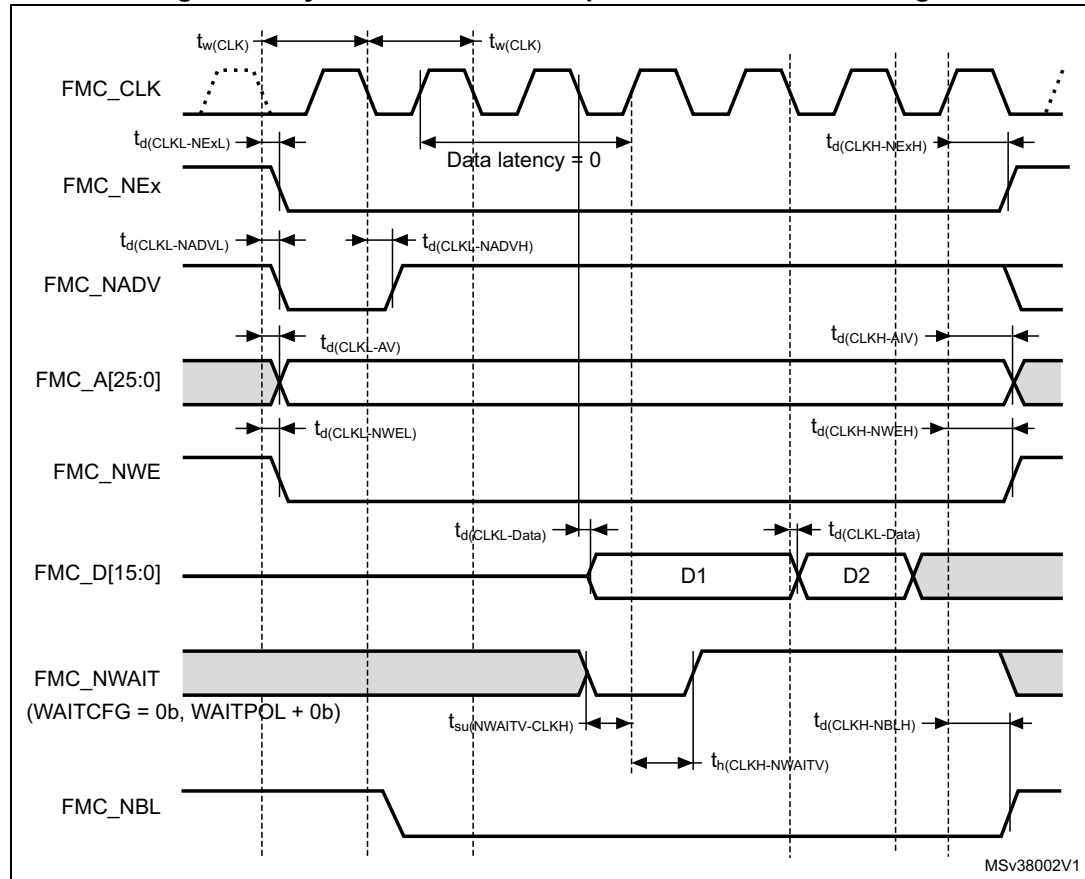


Table 103. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	0.080	-	-	0.0031	-
eee	-	0.150	-	-	0.0059	-
fff	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package recommended footprint

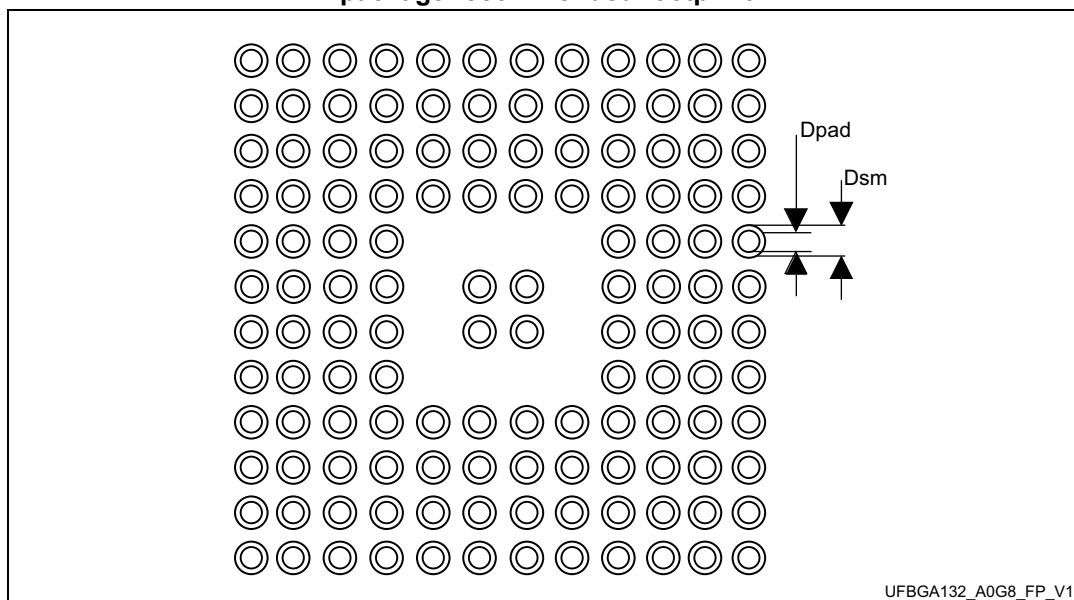
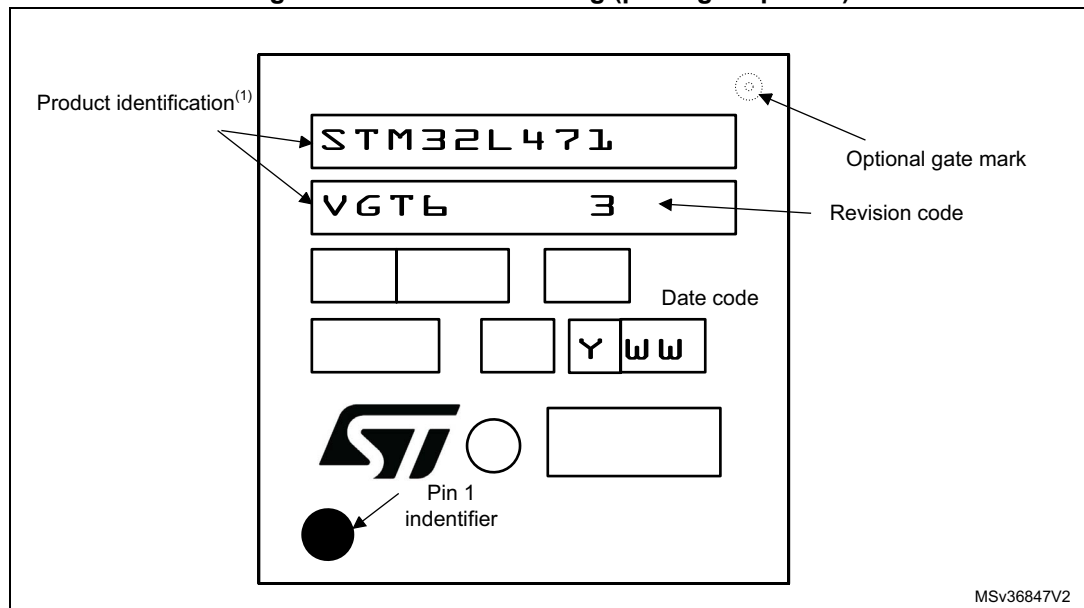


Table 104. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm
Ball diameter	0.280 mm

Figure 56. LQFP100 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.