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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l471zgt6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.17	Voltage	reference buffer (VREFBUF)	39							
3.18	Compai	Comparators (COMP)								
3.19	Operati	Operational amplifier (OPAMP) 40								
3.20	Touch s	Fouch sensing controller (TSC) 40								
3.21	Digital f	Digital filter for Sigma-Delta Modulators (DFSDM)								
3.22	Randon	n number generator (RNG)	43							
3.23	Timers	and watchdogs	43							
	3.23.1	Advanced-control timer (TIM1, TIM8)	43							
	3.23.2	General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)	44							
	3.23.3	Basic timers (TIM6 and TIM7)	44							
	3.23.4	Low-power timer (LPTIM1 and LPTIM2)	44							
	3.23.5	Independent watchdog (IWDG)	45							
	3.23.6	System window watchdog (WWDG)	45							
	3.23.7	SysTick timer	45							
3.24	Real-tin	ne clock (RTC) and backup registers	46							
3.25	Inter-int	egrated circuit interface (I ² C)	47							
3.26	Univers	al synchronous/asynchronous receiver transmitter (USART) .	48							
3.27	Low-po	wer universal asynchronous receiver transmitter (LPUART)	49							
.28	Serial p	eripheral interface (SPI)	50							
.29	Serial a	udio interfaces (SAI)	50							
3.30	Single v	wire protocol master interface (SWPMI)	51							
3.31	Controll	ler area network (CAN)	51							
3.32	Secure	digital input/output and MultiMediaCards Interface (SDMMC) .	52							
3.33	Flexible	e static memory controller (FSMC)	52							
3.34	Quad S	PI memory interface (QUADSPI)	53							
3.35	Develop	oment support	55							
	3.35.1	Serial wire JTAG debug port (SWJ-DP)	55							
	3.35.2	Embedded Trace Macrocell™	55							
	, <u>-</u>									
Pino	uts and	pin description	56							
Mem	orv man	pping	86							
	σιγπαμ	איייאי איז איז איז איז איז איז איז איז א								
Elect	rical cha	aracteristics	91							



4

5

6

List of figures

Figure 1.	STM32L471xx block diagram	15
Figure 2.	Power supply overview.	20
Figure 3.	Clock tree	34
Figure 4.	Voltage reference buffer	39
Figure 5.	STM32L471Zx LQFP144 pinout ⁽¹⁾	56
Figure 6.	STM32L471Qx UFBGA132 ballout ⁽¹⁾	57
Figure 7.	STM32L471Vx LQFP100 pinout ⁽¹⁾	57
Figure 8.	STM32L471Rx LQFP64 pinout ⁽¹⁾	58
Figure 9.	STM32L471 memory map	86
Figure 10.	Pin loading conditions	91
Figure 11.	Pin input voltage	91
Figure 12.	Power supply scheme.	92
Figure 13.	Current consumption measurement scheme	93
Figure 14.	VREFINT versus temperature	99
Figure 15.	High-speed external clock source AC timing diagram	121
Figure 16.	Low-speed external clock source AC timing diagram	122
Figure 17.	Typical application with an 8 MHz crystal	124
Figure 18.	Typical application with a 32.768 kHz crystal	125
Figure 19.	HSI16 frequency versus temperature	127
Figure 20.	Typical current consumption versus MSI frequency	130
Figure 21.	I/O input characteristics	139
Figure 22.	I/O AC characteristics definition ⁽¹⁾	143
Figure 23.	Recommended NRST pin protection	144
Figure 24.	ADC accuracy characteristics	157
Figure 25.	Typical connection diagram using the ADC	157
Figure 26.	12-bit buffered / non-buffered DAC.	160
Figure 27.	SPI timing diagram - slave mode and CPHA = 0	174
Figure 28.	SPI timing diagram - slave mode and CPHA = 1	175
Figure 29.	SPI timing diagram - master mode	175
Figure 30.	Quad SPI timing diagram - SDR mode	177
Figure 31.	Quad SPI timing diagram - DDR mode	177
Figure 32.	SAI master timing waveforms	179
Figure 33.	SAI slave timing waveforms	180
Figure 34.	SDIO high-speed mode	181
Figure 35.	SD default mode	182
Figure 36.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	184
Figure 37.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	186
Figure 38.	Asynchronous multiplexed PSRAM/NOR read waveforms.	187
Figure 39.	Asynchronous multiplexed PSRAM/NOR write waveforms	189
Figure 40.	Synchronous multiplexed NOR/PSRAM read timings	191
Figure 41.	Synchronous multiplexed PSRAM write timings.	193
Figure 42.	Synchronous non-multiplexed NOR/PSRAM read timings	195
Figure 43.	Synchronous non-multiplexed PSRAM write timings	196
Figure 44.	NAND controller waveforms for read access	198
Figure 45	NAND controller waveforms for write access	198
Figure 46.	NAND controller waveforms for common memory read access	198
Figure 47	NAND controller waveforms for common memory write access.	199
Figure 48.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline	200



Figure 49.	LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint.	202
Figure 50.	LQFP144 marking (package top view)	203
Figure 51.	UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array	
	package outline	204
Figure 52.	UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array	
	package recommended footprint	205
Figure 53.	UFBGA132 marking (package top view)	206
Figure 54.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	207
Figure 55.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat	
-	recommended footprint	208
Figure 56.	LQFP100 marking (package top view)	209
Figure 57.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline	210
Figure 58.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package	
U U	recommended footprint.	211
Figure 59.	LQFP64 marking (package top view)	212
Figure 60.	LQFP64 P_D max vs. T_A	215



3.10 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Interconnect source	Interconnect destination	Interconnect action	una	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
TIMx	ADCx DACx DFSDM	Conversion triggers	Y	Y	Y	Y	I	-
	DMA	Memory to memory transfer trigger	Y	Υ	Y	Υ	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Υ	-	-
COMPY	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison			Y	Y	-	-
COMPX	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
	TIM16	Timer input channel from RTC events		Υ	Y	Υ	-	-
RTC	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	locks sources (internal TIM2 Clock source used as input channel for RC measurement and trimming		Y	Y	Y	Y	1	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-

Table 6. STM32L471xx peripherals interconnect matrix



3.35 Development support

3.35.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.35.2 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L471xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.



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STM32L471xx

	Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see <i>Table 17</i>) (continued)										
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7		
Port		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	12C1/12C2/12C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3		
	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	USART3_CK		
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM_DATIN0	USART3_RTS_ DE		
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM_CKIN0	-		
	PB3	JTDO- TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE		
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	USART1_CTS		
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK		
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	-	DFSDM_DATIN5	USART1_TX		
Dort D	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	-	DFSDM_CKIN5	USART1_RX		
Port B	PB8	-	-	TIM4_CH3	-	I2C1_SCL	-	DFSDM_DATIN6	-		
	PB9	-	IR_OUT	TIM4_CH4	-	I2C1_SDA	SPI2_NSS	DFSDM_CKIN6	-		
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK	DFSDM_DATIN7	USART3_TX		
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	DFSDM_CKIN7	USART3_RX		
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_ COMP2	I2C2_SMBA	SPI2_NSS	DFSDM_DATIN1	USART3_CK		
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM_CKIN1	USART3_CTS		
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM_DATIN2	USART3_RTS_ DE		
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM_CKIN2	-		
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DocID027226 Rev 1

5

72/218

_	Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see Table 16)											
		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15			
Port		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT			
	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT			
	PA1	UART4_RX	-	-	-	-	-	TIM15_CH1N	EVENTOUT			
	PA2	-	-	-	-	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT			
	PA3	-	-	-	-	-	-	TIM15_CH2	EVENTOUT			
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT			
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT			
	PA6	-	-	QUADSPI_BK1_IO3	-	TIM1_BKIN_ COMP2	TIM8_BKIN_ COMP2	TIM16_CH1	EVENTOUT			
	PA7	-	-	QUADSPI_BK1_IO2	-	-	-	TIM17_CH1	EVENTOUT			
Port A	PA8	-	-	-	-	-	-	LPTIM2_OUT	EVENTOUT			
	PA9	-	-	-	-	-	-	TIM15_BKIN	EVENTOUT			
	PA10	-	-	-	-	-	-	TIM17_BKIN	EVENTOUT			
	PA11	-	CAN1_RX	-	-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT			
	PA12	-	CAN1_TX	-	-	-	-	-	EVENTOUT			
	PA13	-	-	-	-	-	-	-	EVENTOUT			
	PA14	-	-	-	-	-	-	-	EVENTOUT			
	PA15	UART4_RTS _DE	TSC_G3_IO1	-	-	-	SAI2_FS_B	-	EVENTOUT			

78/218

DocID027226 Rev 1

5

STM32L471xx

Pinouts and pin description

		Ta	able 17. Altern	ate function AF8 to	AF15 (for A	F0 to AF7 see Table	16) (continued	l)	
		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
P	ort	UART4, UART5, LPUART1	CAN1, TSC	QUADSPI		SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
	PB0	-	-	QUADSPI_BK1_IO1	-	COMP1_OUT	-	-	EVENTOUT
	PB1	-	-	QUADSPI_BK1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	-	-	-	-	EVENTOUT
	PB3	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS _DE	TSC_G2_IO1	-	-	-	SAI1_MCLK_ B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	-	-	TIM8_BKIN2_ COMP2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	-	-	FMC_NL	TIM8_BKIN_ COMP1	TIM17_CH1N	EVENTOUT
Port B	PB8	-	CAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK_ A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	-	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_ RX	-	QUADSPI_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_NCS	-	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_ RTS_DE	TSC_G1_IO1	-	-	SWPMI1_IO	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_ CTS	TSC_G1_IO2	-	-	SWPMI1_TX	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	SWPMI1_RX	SAI2_MCLK_ A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	SWPMI1_SUSPEND	SAI2_SD_A	TIM15_CH2	EVENTOUT

79/218

STM32L471xx

Pinouts and pin description

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see Table 16) (continued)										
		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
P	ort	UART4, UART5, LPUART1	UART4, UART5, CAN1, TSC QUAD LPUART1		-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT	
	PE0	-	-	-	-	FMC_NBL0	-	TIM16_CH1	EVENTOUT	
	PE1	-	-	-	-	FMC_NBL1	-	TIM17_CH1	EVENTOUT	
	PE2	-	TSC_G7_IO1	-	-	FMC_A23	SAI1_MCLK_ A	-	EVENTOUT	
	PE3	-	TSC_G7_IO2	-	-	FMC_A19	SAI1_SD_B	-	EVENTOUT	
	PE4	-	TSC_G7_IO3	-	-	FMC_A20	SAI1_FS_A	-	EVENTOUT	
	PE5	-	TSC_G7_IO4	-	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT	
	PE6	-	-	-	-	FMC_A22	SAI1_SD_A	-	EVENTOUT	
	PE7	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT	
PORE	PE8	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT	
	PE9	-	-	-	-	FMC_D6	SAI1_FS_B	-	EVENTOUT	
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	FMC_D7	SAI1_MCLK_ B	-	EVENTOUT	
	PE11	-	TSC_G5_IO2	QUADSPI_NCS	-	FMC_D8	-	-	EVENTOUT	
	PE12	-	TSC_G5_IO3	QUADSPI_BK1_IO0	-	FMC_D9	-	-	EVENTOUT	
	PE13	-	TSC_G5_IO4	QUADSPI_BK1_IO1	-	FMC_D10	-	-	EVENTOUT	
	PE14	-	-	QUADSPI_BK1_IO2	-	FMC_D11	-	-	EVENTOUT	
	PE15	-	-	QUADSPI_BK1_IO3	-	FMC_D12	-	-	EVENTOUT	

5

STM32L471xx

Pinouts and pin description

Bus	Boundary address	Size (bytes)	Peripheral
	0x4001 6400 - 0x4001 FFFF	39 KB	Reserved
	0x4001 6000 - 0x4000 63FF	1 KB	DFSDM
	0x4001 5C00 - 0x4000 5FFF	1 KB	Reserved
	0x4001 5800 - 0x4000 5BFF	1 KB	SAI2
APB2	0x4001 5400 - 0x4000 57FF	1 KB	SAI1
	0x4001 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	SDMMC1
APB2	0x4001 2000 - 0x4001 27FF	2 KB	Reserved
	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800- 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF		COMP
	0x4001 0030 - 0x4001 01FF	1 KB	VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG

Table 18. STM32L471xx memory map and peripheral register boundaryaddresses (continued)⁽¹⁾



- For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
- 4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see Section 7.5: Thermal characteristics).
- 5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see Section 7.5: Thermal characteristics).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Symbol	Parameter	Conditions	Min	Мах	Unit						
t _{VDD}	V _{DD} rise time rate		0	8	μs/V						
	V _{DD} fall time rate	-	10	8							
+	V _{DDA} rise time rate		0	8	ue\/						
۷DDA	V _{DDA} fall time rate	-	10	8	μ3/ ν						
t _{VDDIO2}	V _{DDIO2} rise time rate		0	8	ue\/						
	V _{DDIO2} fall time rate	-	10	∞	μ5/ ν						

Table 23. Operating conditions at power-up / power-down

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under the ambient temperature conditions summarized in *Table 22: General operating conditions*.

Symbol	Parameter	Conditions ⁽¹⁾	Min	Тур	Max	Unit	
t _{RSTTEMPO} ⁽²⁾	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	μs	
V (2)	Prown out report throughold 0	Rising edge	1.62	1.66	1.7	V	
VBOR0(-)		Falling edge	1.6	1.64	1.69	V	
V	Drown out react threshold 1	Rising edge	2.06	2.1	2.14	V	
VBOR1		Falling edge	1.96	2	2.04		
N/	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V	
VBOR2		Falling edge	edge 2.16 2.20 2.24		2.24		
V	Prown out report throughold 2	Rising edge	2.56	2.61	2.66	V	
VBOR3	BIOWII-OULTESEL LITESHOLD 5	Falling edge	2.47	2.52	2.57	V	
V	Drown out react threshold 4	Rising edge 2.85 2.9		2.90	2.95	V	
VBOR4	BIOWII-OULTESEL LITESHOLU 4	Falling edge	2.76	2.81	2.86	v	
	Programmable voltage	Rising edge	2.1	2.15	2.19	V	
VPVD0	detector threshold 0	Falling edge	2	2.05	2.1	v	

Table 24. Embedded reset and power control block characteristics



6.3.4 Embedded voltage reference

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

		· · ·				
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{REFINT}	Internal reference voltage	–40 °C < T _A < +130 °C	1.182	1.212	1.232	V
t _{S_vrefint} ⁽¹⁾	ADC sampling time when reading the internal reference voltage	_	4 ⁽²⁾	-	-	μs
t _{start_vrefint}	Start time of reference voltage buffer when ADC is enable		-	8	12 ⁽²⁾	μs
V_{REFINT} buffer consumption from V_{DD} when converted by ADC		-	-	12.5	20 ⁽²⁾	μA
ΔV_{REFINT}	ΔV _{REFINT} Internal reference voltage spread over the temperature V range		-	5	7.5 ⁽²⁾	mV
T _{Coeff}	Average temperature coefficient	–40°C < T _A < +130°C	-	30	50 ⁽²⁾	ppm/°C
A _{Coeff}	Long term stability	1000 hours, T = 25°C	-	-	TBD ⁽²⁾	ppm
V _{DDCoeff}	Average voltage coefficient	3.0 V < V _{DD} < 3.6 V	-	250	1200 ⁽²⁾	ppm/V
V _{REFINT_DIV1}	1/4 reference voltage		24	25	26	
V _{REFINT_DIV2}	1/2 reference voltage	-	49	50	51	% Vrefint
V _{REFINT_DIV3}	3/4 reference voltage		74	75	76	

Table	25.	Embedded	internal	voltage	reference
IUNIC	_ U.	LIIIbcaaca	miterinar	vonugo	101010100

1. The shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design.

Table 36. Current consumption in Stop 0 mode														
Symbol	Deremeter	Conditions			TYP					MAX ⁽¹⁾			Unit	
Symbol	Farameter	V _{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	Unit	
I _{DD} (Stop 0)		Supply	1.8 V	108	132	217	356	631	153	213	426	773	1461	
	current in	2.4 V	110	134	219	358	634	158	218	431	778	1468		
	IDD (Stop 0)	Stop 0 mode,	3 V	111	135	220	360	637	161	221	433	783	1476	μΛ
	KIC uisabled	3.6 V	113	137	222	363	642	166	226	438	791 ⁽²⁾	1488		

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1. Guaranteed by characterization results, unless otherwise specified.

2. Guaranteed by test in production.

110/218

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table	56.	Electrical	sensitivities
Table	UU .	LICCUICAI	30113111411103

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105 \text{ °C conforming to JESD78A}$	II level A ⁽¹⁾

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μ A/+0 μ A range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in Table 57.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Symbol	Description	Func susce	Unit		
Symbol	Description	Negative Positive injection injection			
I _{INJ}	Injected current on BOOT0 pin	-0	NA ⁽¹⁾		
	Injected current on pins except PA4, PA5, BOOT0	-5	NA ⁽¹⁾	mA	
	Injected current on PA4, PA5 pins	-5	0		

Table 57. I/O current injection susceptibility

1. NA: not applicable



Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Тур	Max	Unit
			Single	Fast channel (max speed)	-	4	5	
ст	Total		ended	Slow channel (max speed)	-	4	5	
	error		Differential	Fast channel (max speed)	-	3.5	4.5	
			Differential	Slow channel (max speed)	-	3.5	4.5	
			Single	Fast channel (max speed)	-	1	2.5	
FO	Offset		ended	Slow channel (max speed)	-	1	2.5	
	error		Differential	Fast channel (max speed)	-	1.5	2.5	
			Differential	Slow channel (max speed)	-	1.5	2.5	
			Single	Fast channel (max speed)	-	2.5	4.5	
EG Gain error		ended	Slow channel (max speed)	-	2.5	4.5	ISB	
EG	Gain entri		Differential Fast channel (max speed)	-	2.5	3.5	LSB	
			Differential	Slow channel (max speed)	-	2.5	3.5	
Differential ED linearity error			Single	Fast channel (max speed)Slow channel (max speed)	-	1	1.5	
	Differential linearity error		ended		-	1	1.5	
		ADC clock frequency ≤	Differential Fast channel (max speed)	-	1	1.2		
		80 MHz, Sampling rate < 5.33 Msps	Dillerential	Slow channel (max speed)	-	1	1.2	-
		$V_{DDA} = VREF + = 3 V,$ ntegral TA = 25 °C nearity error	Single ended	Fast channel (max speed)	-	1.5	2.5	
	Integral			Slow channel (max speed)	-	1.5	2.5	
	error		Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
			Single	Fast channel (max speed)	10.4	10.5	-	
ENOR	Effective	Effective	ended	Slow channel (max speed)	10.4	10.5	-	bite
ENOD	bits		Differential	Fast channel (max speed)	10.8	10.9	-	DILS
			Differential	Slow channel (max speed)	10.8	10.9	-	
	Signal to		Single	Fast channel (max speed)	64.4	65	-	
	noise and		ended	Slow channel (max speed)	64.4	65	-	
SINAD	distortion		Differential	Fast channel (max speed)	66.8	67.4	-	
	1010		Differential	Slow channel (max speed)	66.8	67.4	-	dD
			Single	Fast channel (max speed)	65	66	-	uБ
SNID	Signal-to-		ended	Slow channel (max speed)	65	66	-	
SINK	noise ratio		Difforantial	Fast channel (max speed)	67	68	-	
			Dinerential	Slow channel (max speed)	67	68	-	

Table 65, ADC accuracy - limited test conditions 1 ⁽¹⁾⁽²⁾⁽	Table 65. ADC a	ccuracy - limited	d test condition	າs 1 ⁽¹⁾⁽²⁾⁽³⁾
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6.3.26 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I^2 C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0392 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOX} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to Section 6.3.14: I/O port characteristics for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Symbol	Parameter	Min	Мах	Unit
t _{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

Table 81. I2C analog filter characteristics⁽¹⁾

1. Guaranteed by design.

2. Spikes with widths below $t_{AF(min)}$ are filtered.

3. Spikes with widths above $t_{AF(max)}$ are not filtered





Figure 33. SAI slave timing waveforms

SDMMC characteristics

Unless otherwise specified, the parameters given in *Table 86* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output characteristics.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
t _{W(CKL)}	Clock low time	f _{PP} = 50 MHz	8	10	-	ns
t _{W(CKH)}	Clock high time	f _{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t _{ISU}	Input setup time HS	f _{PP} = 50 MHz	2	-	-	ns
t _{IH}	Input hold time HS	f_{PP} = 50 MHz	4.5	-	-	ns
CMD, D outp	uts (referenced to CK) in MMC and SD	HS mode				
t _{OV}	Output valid time HS	f _{PP} = 50 MHz	-	12	14	ns
t _{OH}	Output hold time HS	f _{PP} = 50 MHz	9	-	-	ns
CMD, D input	s (referenced to CK) in SD default mod	le				
t _{ISUD}	Input setup time SD	f _{PP} = 50 MHz	2	-	-	ns
t _{IHD}	Input hold time SD	f _{PP} = 50 MHz	4.5	-	-	ns

Table 86. SD / MMC dynamic characteristics, V_{DD} =2.7 V to 3.6 V⁽¹⁾





Figure 41. Synchronous multiplexed PSRAM write timings



Symbol		millimeters			inches ⁽¹⁾	
Symbol	Min	Тур	Мах	Min	Тур	Мах
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
с	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ССС	-	-	0.080	-	-	0.0031

Table 102. LQFP144 - 144-pin, 20 x 2	0 mm low-profile q	uad flat package
mechanical data		

1. Values in inches are converted from mm and rounded to 4 decimal digits.







1. Dimensions are expressed in millimeters.

