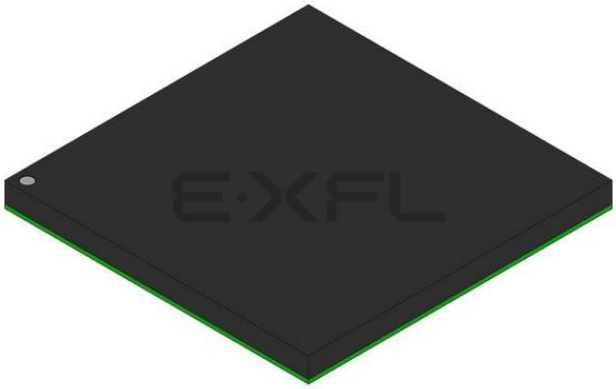

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	132MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc5566mzp132

Table 2. Absolute Maximum Ratings [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
28	Maximum solder temperature [11] Lead free (Pb-free) Leaded (SnPb)	T_{SDR}	— —	260.0 245.0	°C
29	Moisture sensitivity level [12]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

2 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

4 AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

5 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on eTPUB[15] and SINB during the internal power-on reset (POR) state.

6 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

7 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

9 Total injection current for all analog input pins must not exceed 15 mA.

10 Lifetime operation at these specification limits is not guaranteed.

11 Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

12 Moisture sensitivity per JEDEC test method A112.

3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

Table 3. MPC5566 Thermal Characteristics

Spec	MPC5566 Thermal Characteristic	Symbol	416 PBGA	Unit
1	Junction to ambient, natural convection (one-layer board) [1, 2]	$R_{\theta JA}$	24	°C/W
2	Junction to ambient, natural convection (four-layer board 2s2p) [1, 3]	$R_{\theta JA}$	16	°C/W
3	Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	18	°C/W
4	Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	13	°C/W
5	Junction to board (four-layer board 2s2p) [4]	$R_{\theta JB}$	8	°C/W
6	Junction to case [5]	$R_{\theta JC}$	6	°C/W
7	Junction to package top, natural convection [6]	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other board components, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Rd.
San Jose, CA., 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.3 Package

The MPC5566 is available in packaged form. Read the package options in Section 2, “Ordering Information.” Refer to Section 4, “Mechanicals,” for pinouts and package drawings.

3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications [1]

Spec	Characteristic	Minimum	Typical	Maximum	Unit
1	Scan range	0.15	—	1000	MHz
2	Operating frequency	—	—	f_{MAX}	MHz
3	V_{DD} operating voltages	—	1.5	—	V
4	V_{DDSYN}, V_{RC33}, V_{DD33}, V_{FLASH}, V_{DDE} operating voltages	—	3.3	—	V
5	V_{PP}, V_{DDEH}, V_{DDA} operating voltages	—	5.0	—	V
6	Maximum amplitude	—	—	14 [2] 32 [3]	dBuV
7	Operating temperature	—	—	25	°C

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

2 Measured with the single-chip EMI program.

3 Measured with the expanded EMI program.

1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

During initial power ramp-up, when V_{stby} is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until V_{DD} is applied. This current will not reoccur until V_{stby} is lowered below V_{stby} min. specification.

Figure 2 shows an approximate interpolation of the I_{STBY} worst-case specification to estimate values at different voltages and temperatures. The vertical lines shown at 25 °C, 60 °C, and 150 °C in Figure 2 are the actual I_{DD_STBY} specifications (27d) listed in Table 9.

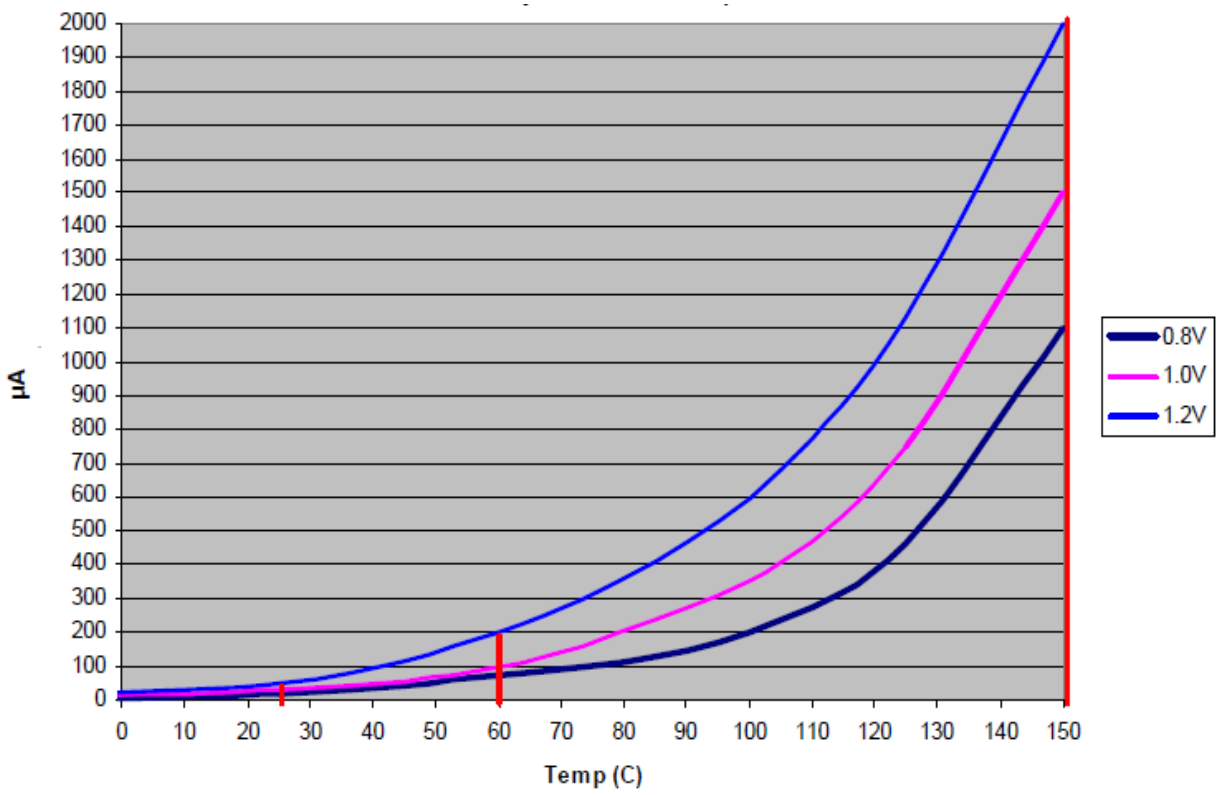

Figure 2. fI_{STBY} Worst-case Specifications

Table 12. FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at f_{SYS} max: [13, 14] Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	C_{JITTER}	 — —	 5.0 0.01	% f_{CLKOUT}
20	Frequency modulation range limit [15] (do not exceed f_{sys} maximum)	C_{MOD}	0.8	2.4	$\%f_{SYS}$
21	ICO frequency $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ [16] $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$	f_{ico}	48	f_{MAX}	MHz
22	Predivider output frequency (to PLL)	f_{PREDIV}	4	20 [17]	MHz

1 Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

2 All internal registers retain data at 0 Hz.

3 Up to the maximum frequency rating of the device (refer to Table 1).

4 Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

5 The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below f_{LOR}. SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

6 Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). (V_{extal} – V_{xtal}) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

7 Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). (V_{xtal} – V_{extal}) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

8 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

9 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

10 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

11 PLL is operating in 1:1 PLL mode.

12 V_{DDE} = 3.0–3.6 V.

13 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

14 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

15 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

16 $f_{sys} = f_{ico} \div (2^{RFD})$.

17 Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

Table 18. Derated Pad AC Specifications (V_{DDEH} = 3.3 V, V_{DDE} = 3.3 V) [1] (continued)

Spec	Pad	SRC/DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [3, 5] (ns)	Load Drive (pF)
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9500	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 3.0–3.6 V; V_{DDEH} = 3.0–3.6 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and guaranteed by design (not tested).

3 The output delay, and the rise and fall, are calculated to 20% or 80% of the respective signal.

4 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

5 This parameter is guaranteed by characterization rather than 100% tested.

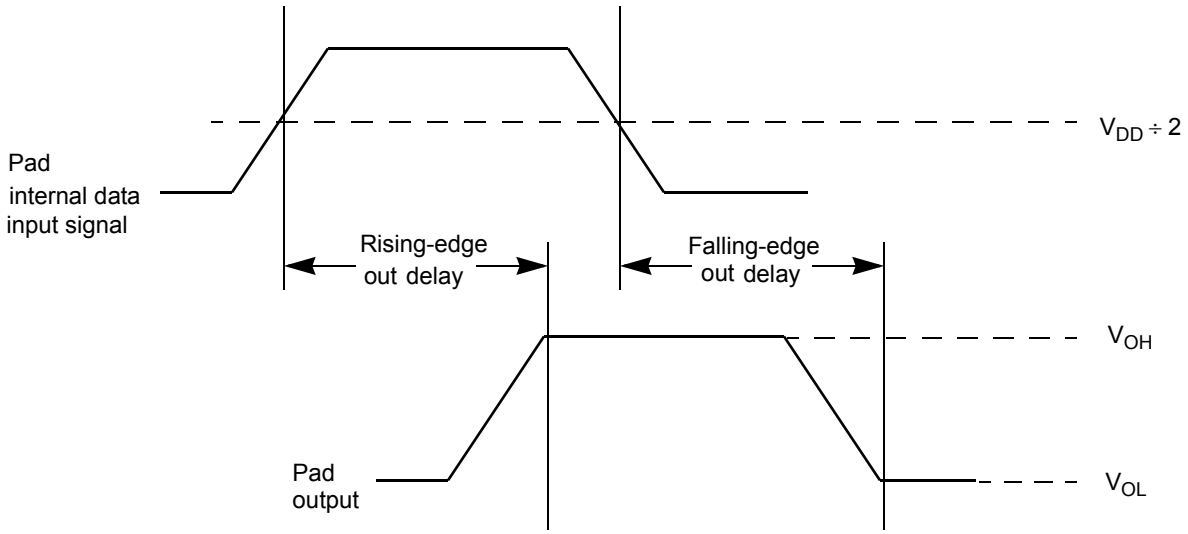

Figure 4. Pad Output Delay

3.13 AC Timing

3.13.1 Reset and Configuration Pin Timing

Table 19. Reset and Configuration Pin Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	$\overline{\text{RESET}}$ pulse width	t_{RPW}	10	—	t_{CYC}
2	$\overline{\text{RESET}}$ glitch detect pulse width	t_{GPW}	2	—	t_{CYC}

Table 19. Reset and Configuration Pin Timing [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
3	PLLCFG, BOOTCFG, WKPCFG, RSTCFG setup time to RSTOUT valid	t_{RCSU}	10	—	t_{CYC}
4	PLLCFG, BOOTCFG, WKPCFG, RSTCFG hold time from RSTOUT valid	t_{RCH}	0	—	t_{CYC}

1 Reset timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

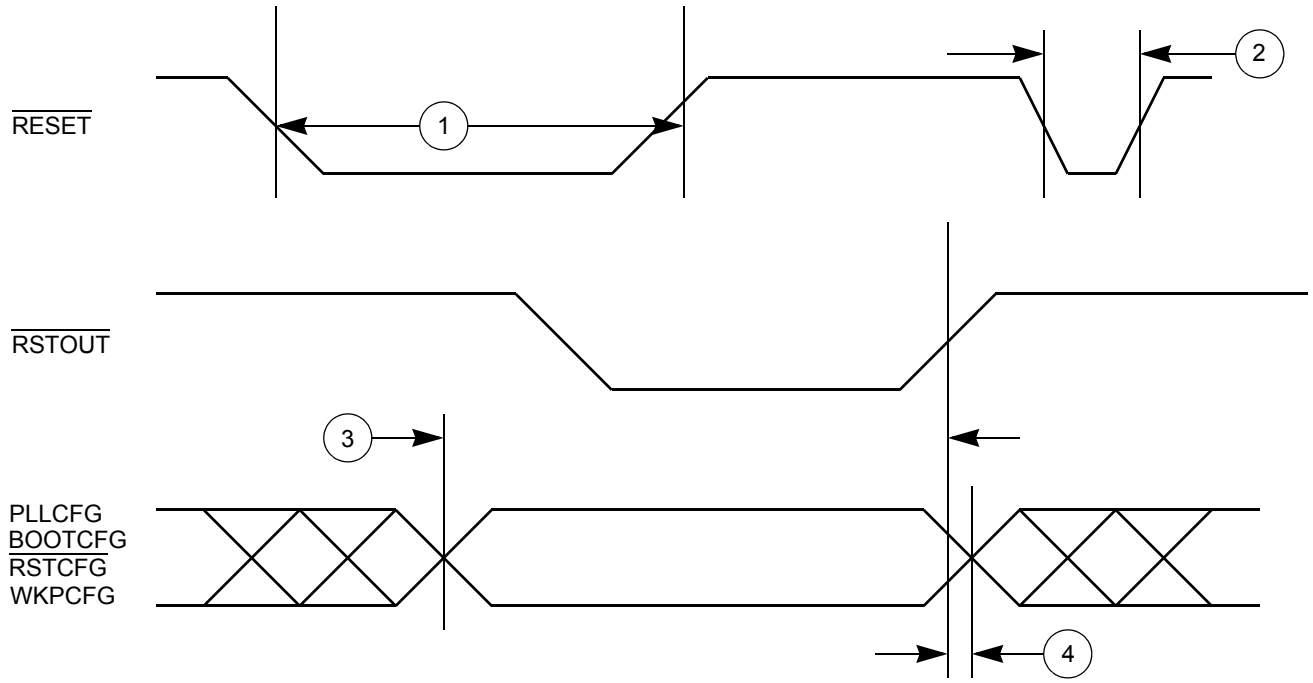

Figure 5. Reset and Configuration Pin Timing

3.13.2 IEEE 1149.1 Interface Timing

Table 20. JTAG Pin AC Electrical Characteristics [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	TCK cycle time	t_{JCYC}	100	—	ns
2	TCK clock pulse width (measured at $V_{DDE} \div 2$)	t_{JDC}	40	60	ns
3	TCK rise and fall times (40% to 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI data setup time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI data hold time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK low to TDO data valid	t_{TDOV}	—	20	ns
7	TCK low to TDO data invalid	t_{TDOI}	0	—	ns
8	TCK low to TDO high impedance	t_{TDOHZ}	—	20	ns
9	JCOMP assertion time	t_{JCMPPW}	100	—	ns
10	JCOMP setup time to TCK low	t_{JCMPS}	40	—	ns
11	TCK falling-edge to output valid	t_{BSDV}	—	50	ns

Table 22. Bus Operation Timing [1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]								Unit	Notes
			40 MHz		56 MHz		67 MHz		72 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
7a	Input signal valid to CLKOUT positive edge (setup time) Calibration bus interface CAL_ADDR[9:30] CAL_DATA[0:15] CAL_RD_WR CAL_TS	t_{CCIS}	11.0	—	8.0	—	6.0	—	4.0	—	ns	
8	CLKOUT positive edge to input signal invalid (hold time) External bus interface ADDR[8:31] DATA[0:31] BG [7] BR [5] BB RD_WR TA TEA TS TSIZ[0:1]	t_{CIH}	1.0	—	1.0	—	1.0	—	1.0	—	ns	
	CLKOUT positive edge to input signal invalid (hold time) Calibration bus interface CAL_ADDR[9:30] CAL_DATA[0:15] CAL_RD_WR CAL_TS	t_{CCIH}	1.0	—	1.0	—	1.0	—	1.0	—	ns	

1 EBI timing specified at V_{DDE} = 1.6–3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and CL = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM): 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; 135 MHz parts allow for 132 MHz system clock + 2% FM; and 147 MHz parts allow for 144 MHz system clock + 2% FM.

3 The external bus is limited to half the speed of the internal bus.

4 Refer to fast pad timing in Table 17 and Table 18 (different values for 1.8 V and 3.3 V).

5 Internal arbitration.

6 EBTS = 0 timings are tested and valid at V_{DDE} = 2.25–3.6 V only; EBTS = 1 timings are tested and valid at V_{DDE} = 1.6–3.6 V.

7 External arbitration.

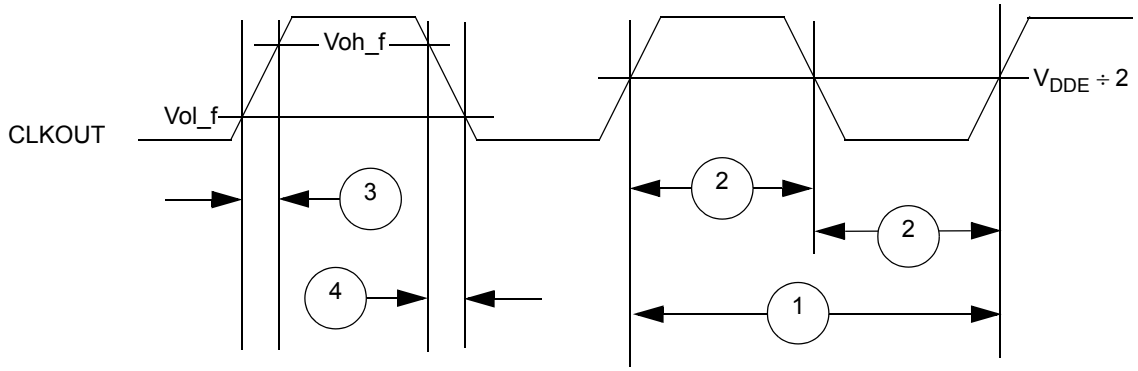

Figure 12. CLKOUT Timing

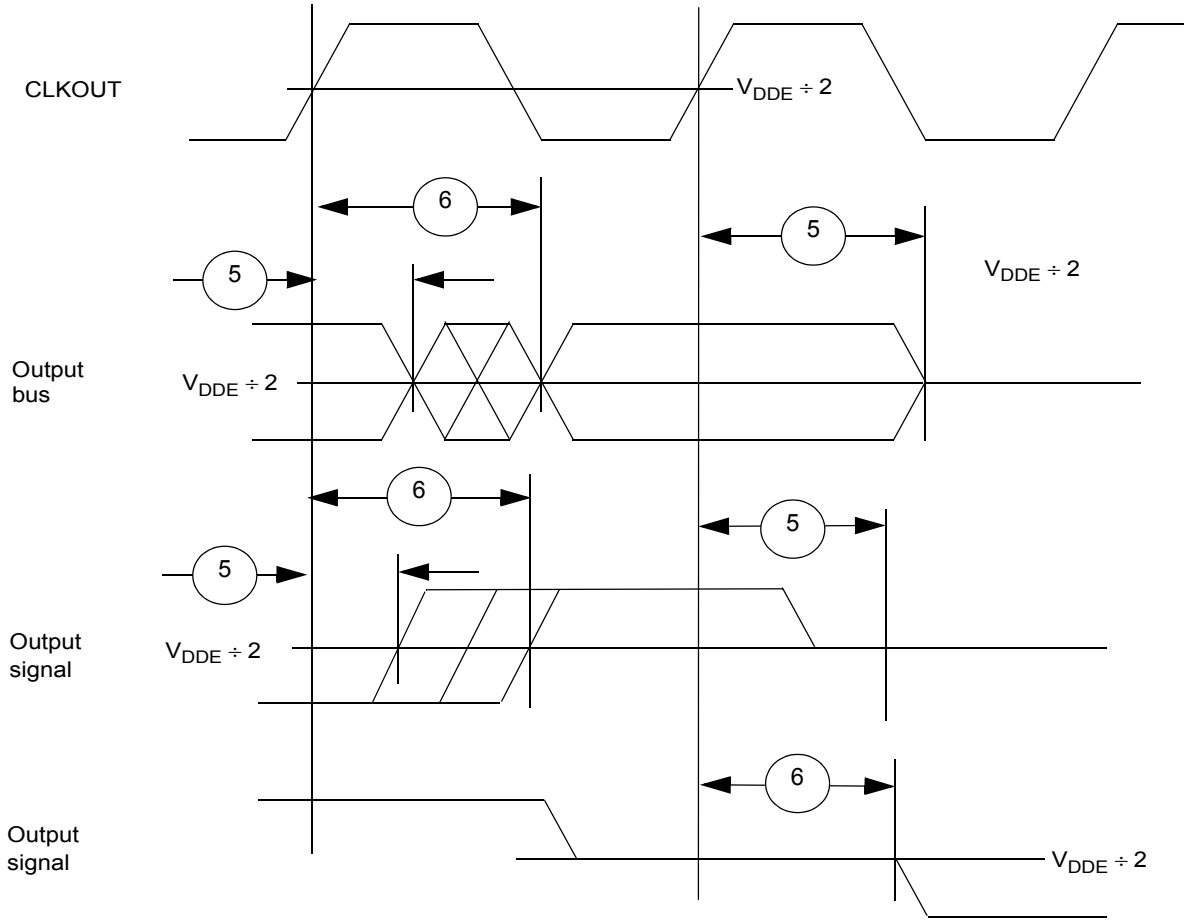

Figure 13. Synchronous Output Timing

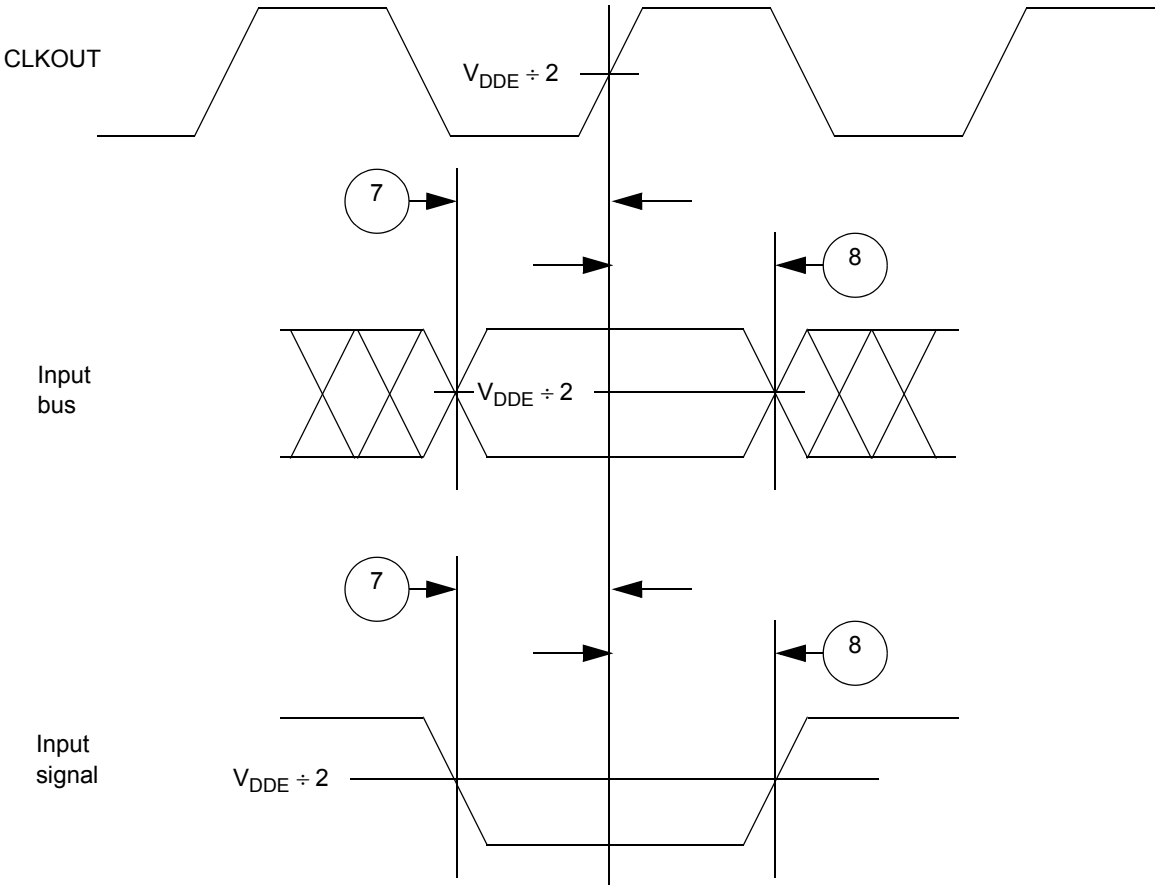

Figure 14. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Signals)

Table 23. External Interrupt Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	IRQ pulse-width low	t_{IPWL}	3	—	t_{CYC}
2	IRQ pulse-width high	T_{IPWH}	3	—	t_{CYC}
3	IRQ edge-to-edge time [2]	t_{ICYC}	6	—	t_{CYC}

1 IRQ timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

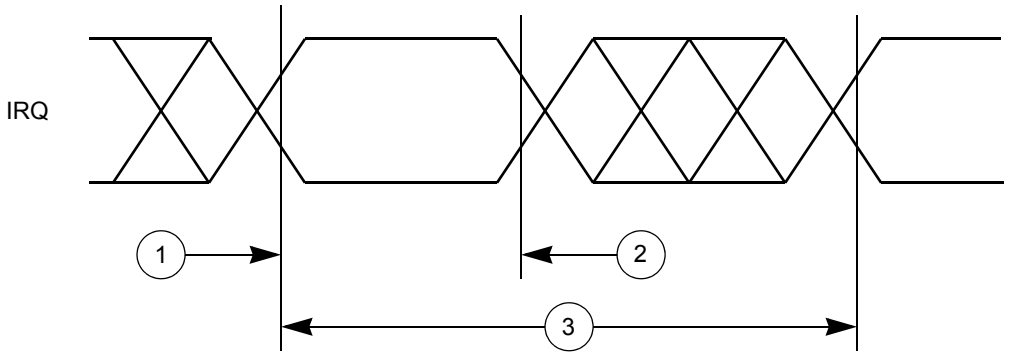

Figure 15. External Interrupt Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing [1]

Spec	Characteristic	Symbol	Min.	Max	Unit
1	eTPU input channel pulse width	t_{ICPW}	4	—	t_{CYC}
2	eTPU output channel pulse width	t_{OCPW}	2 [2]	—	t_{CYC}

1 eTPU timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

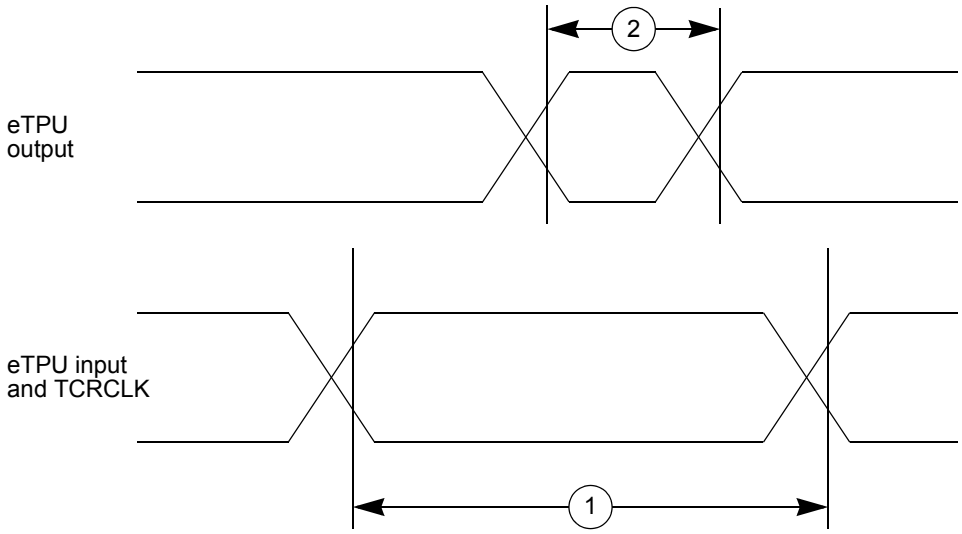

Figure 16. eTPU Timing

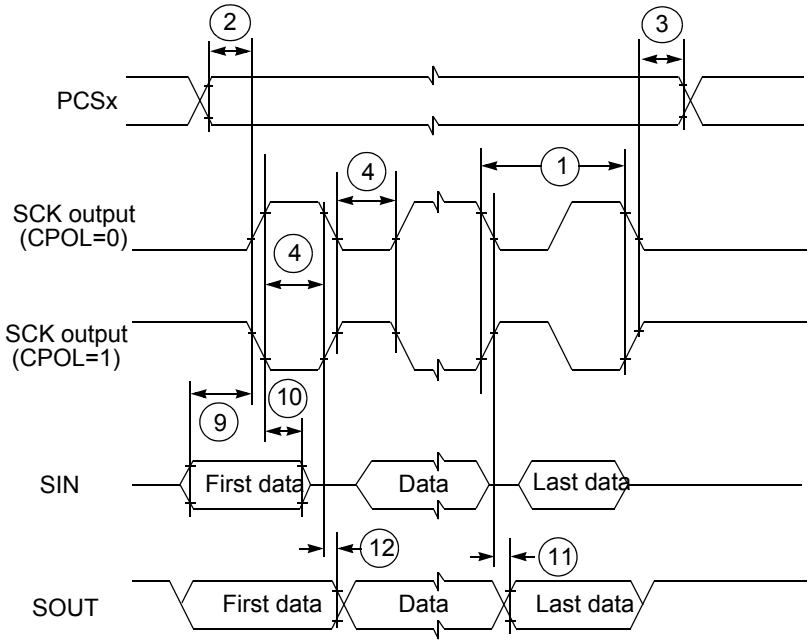

Figure 18. DSPI Classic SPI Timing—Master, CPHA = 0

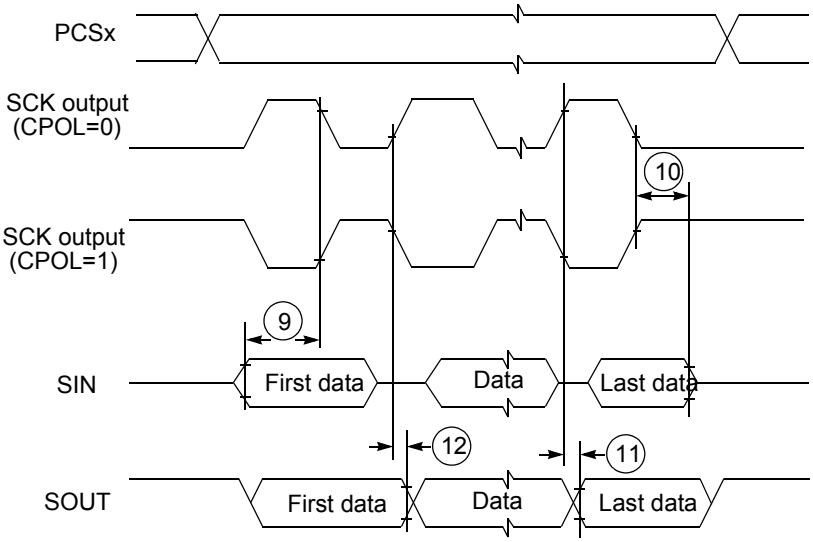

Figure 19. DSPI Classic SPI Timing—Master, CPHA = 1

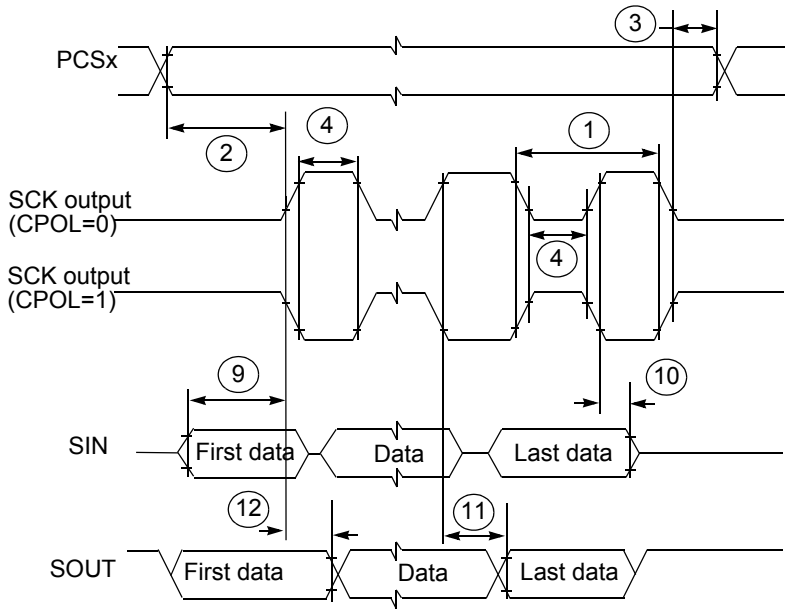

Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 0

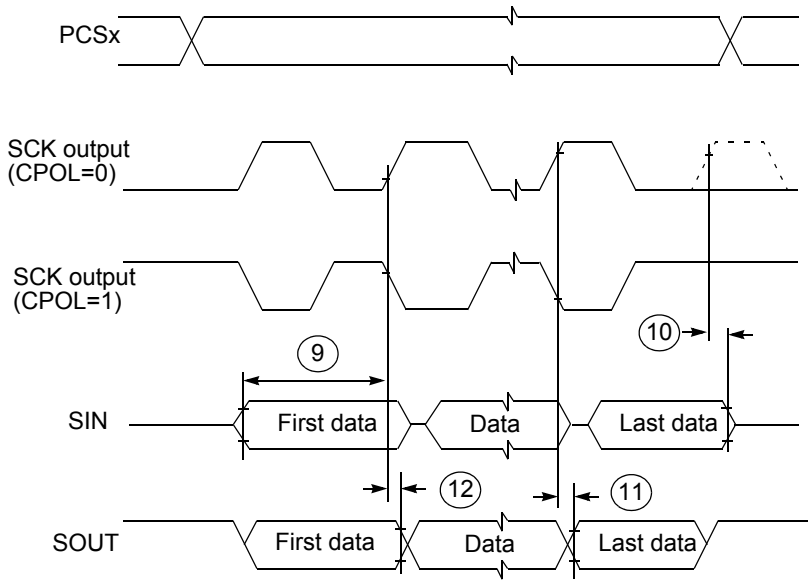

Figure 23. DSPI Modified Transfer Format Timing—Master, CPHA = 1

3.14 Fast Ethernet AC Timing Specifications

Media Independent Interface (MII) Fast Ethernet Controller (FEC) signals use transistor-to-transistor logic (TTL) signal levels compatible with devices operating at 3.3 V. The timing specifications for the MII FEC signals are independent of the system clock frequency (part speed designation).

3.14.1 MII FEC Receive Signal Timing FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK

The receive functions correctly up to an FEC_RX_CLK maximum frequency of 25 MHz plus one percent. There is no minimum frequency requirement. The processor clock frequency must exceed four times the FEC_RX_CLK frequency.

Table 28 lists MII FEC receive channel timings.

Table 28. MII FEC Receive Signal Timing

Spec	Characteristic	Min.	Max	Unit
1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
3	FEC_RX_CLK pulse-width high	35%	65%	FEC_RX_CLK period
4	FEC_RX_CLK pulse-width low	35%	65%	FEC_RX_CLK period

Figure 28 shows MII FEC receive signal timings listed in Table 28.

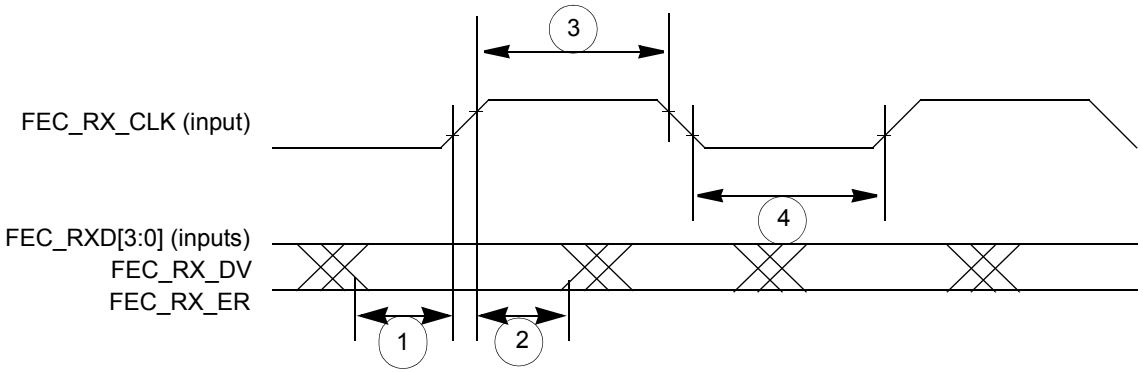

Figure 28. MII FEC Receive Signal Timing Diagram

3.14.3 MII FEC Asynchronous Inputs Signal Timing FEC_CRS and FEC_COL

Table 30 lists MII FEC asynchronous input signal timing.

Table 30. MII FEC Asynchronous Inputs Signal Timing

Spec	Characteristic	Min.	Max	Unit
9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

Figure 30 shows MII FEC asynchronous input timing listed in Table 30.

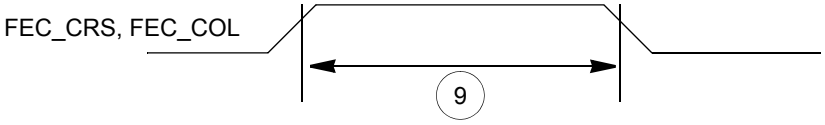

Figure 30. MII FEC Asynchronous Inputs Timing Diagram

3.14.4 MII FEC Serial Management Channel Timing FEC_MDIO and FEC_MDC

Table 31 lists MII FEC serial management channel timing. The FEC functions correctly with a maximum FEC_MDC frequency of 2.5 MHz.

Table 31. MII FEC Serial Management Channel Timing

Spec	Characteristic	Min.	Max	Unit
10	FEC_MDC falling-edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
11	FEC_MDC falling-edge to FEC_MDIO output valid (maximum propagation delay)	—	25	ns
12	FEC_MDIO (input) to FEC_MDC rising-edge setup	10	—	ns
13	FEC_MDIO (input) to FEC_MDC rising-edge hold	0	—	ns
14	FEC_MDC pulse-width high	40%	60%	FEC_MDC period
15	FEC_MDC pulse-width low	40%	60%	FEC_MDC period

Figure 31 shows MII FEC serial management channel timing listed in Table 31.

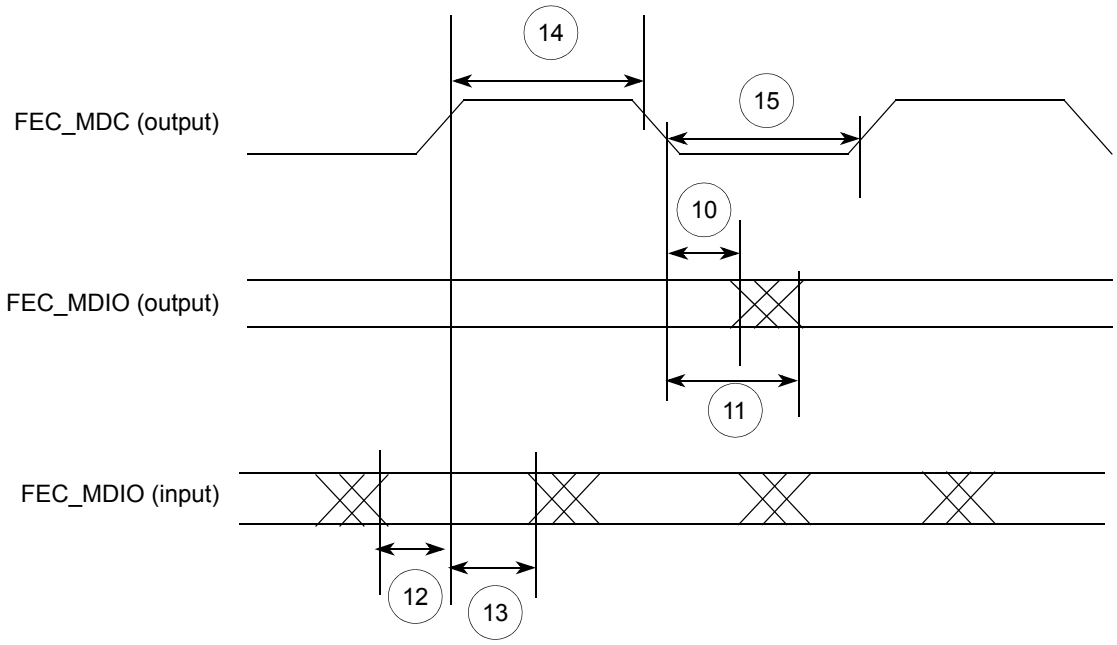

Figure 31. MII FEC Serial Management Channel Timing Diagram

5.3 Information Changed Between Revisions 0.0 and 1.0

The following table lists the global changes made throughout the document, as well as the changes to sections of text not contained in a figure or table.

Table 34. Global and Text Changes Between Rev. 0.0 and 1.0

Location	Description of Changes

Global Changes	• Third paragraph and throughout the document, replaced:
	  • kilobytes with KB.
	  • megabytes with MB.
	• Put overbars on the following signals: $\overline{BB}$, $\overline{BG}$, $\overline{BR}$, $\overline{BDIP}$, $\overline{OE}$, $\overline{TA}$, $\overline{TEA}$, $\overline{TS}$,
	• Changed $\overline{WE}$[0:3]/$\overline{BE}$[0:3] to $\overline{WE}$/$\overline{BE}$[0:3].
	• Added a 144 MHz system frequency option for the MPC5566 microcontroller.

Section 1, “Overview”:	• First paragraph, text changed from “ based on the PowerPC Book E architecture” to “built on the Power Architecture embedded technology.” • Second paragraph: Changed terminology from PowerPC Book E architecture to Power Architecture terminology. • Added new fourth paragraph about VLE feature. • Paragraph nine: changed “the MPC5566 has an on-chip 20-channel enhanced queued analog-to-digital converter (eQADC)” to “has an on-chip 40-channel dual enhanced queued” • Added paragraph about the Fast Ethernet Controller directly after the System Integration Unit paragraph. • Added the sentence directly preceding Table 1: ‘Unless noted in this data sheet, all specifications apply from T_L to T_H.’
3.7.1, 3.7.2 and 3.7.3: Reordered sections resulting in the following order and section renumbering:	• Section 3.7.1, “Input Value of Pins During POR Dependent on VDD33,” then • Section 3.7.2, “Power-Up Sequence (VRC33 Grounded),” then • Section 3.7.3, “Power-Down Sequence (VRC33 Grounded).
Section 3.7.1, “Input Value of Pins During POR Dependent on VDD33,” changed:	From: ‘To avoid accidentally selecting the bypass clock because PLLCFG[0:1] and $\overline{RSTCFG}$ are not treated as ones (1s) when POR negates, V_{DD33} must not lag V_{DDSYN} and the $\overline{RESET}$ pin power (V_{DDEH6}) when powering the device by more than the V_{DD33} lag specification in Table 6. V_{DD33} individually can lag either V_{DDSYN} or the $\overline{RESET}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification. V_{DD33} can lag one of the V_{DDSYN} or V_{DDEH6} supplies, but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.’ To: ‘When powering the device, V_{DD33} must not lag V_{DDSYN} and the $\overline{RESET}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and RSTCFG are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} or the $\overline{RESET}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.’

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 2, Absolute Maximum Ratings:	• Deleted Spec 3, “Flash core voltage.” • Spec 12 “DC Input Voltage”: Deleted from second line‘. . .except for eTPUB15 and SINB (DSPI_B_SIN)’ leaving V_{DDEH} powered I/O pads. Deleted third line ‘V_{DDEH} powered by I/O pads (eTPUB15 and SINB), including the min. and max values of -0.3 and 6.5 respectively, and deleted old footnote 7. • Spec 12 “DC Input Voltage”: Added footnote 8 to second line “V_{DDE} powered I/O pads” that reads: ‘Internal structures hold the input voltage less than the maximum voltage on all pads powered by the V_{DDE} supplies, if the maximum injection current specification is met (s mA for all pins) and V_{DDE} is within the operating voltage specifications. • Spec 14, column 2, changed: ‘V_{SS} differential voltage’ to ‘V_{SS} to V_{SSA} differential voltage.’ • Spec 15, column 2, changed: ‘V_{DD} differential voltage’ to ‘V_{DD} to V_{DDA} differential voltage.’ • Spec 21, Added the name of the spec, ‘*V_{RC33} to V_{DDSYN} differential voltage,’* as well as the name and cross reference to Table 9, *DC Electrical Specification*s, to which the Spec was moved. • Spec 28 “Maximum Solder Temperature”: Added two subordinate lines: Lead free (PbFree) and Leaded (SnPb) with maximum values of 260 C and 245 C respectively. • Footnote 1, added: ‘any of’ between ‘beyond’ and ‘the listed maxima.’ • Deleted footnote 2: ‘Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.’Spec 26 “Maximum Operating Temperature Range”: replaced -40 C with T_L. • Footnote 6 (now footnote 5): Changed to the following sentence to the end, “Internal structures hold the input voltage greater than -1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than -0.6 V on eTPU[15] and on SINB during the internal power-on reset (POR) state.”
Table 4, EMI Testing Specifications:	• Changed the maximum operating frequency to from 132 to f_{MAX}. • Footnote 2: Deleted ‘Refer to Table 1 for the maximum operating frequency.’

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 15, Flash EEPROM Module Life:	• Replaced (Full Temperature Range) with ($T_A = T_L - T_H$) in the table title. • Spec 1b, Min. column value changed from 10,000 to 1,000.
Table 16, FLASH BIU Settings vs. Frequency of Operations:	• 'Added footnote 1 to the end of the table title, The footnote reads: 'Illegal combinations exist. Use entries from the same row in this table.' • Added fourth row '147 MHz' after the '135 MHz' row and before the 'Default setting after reset': Columns DPFEN, IPFEN, PFLIM, and BFEN are the same as the 135 MHz column. New values for the following columns: APC = 0b011, RWSC = 0b100, WWSC = 0b01. • Moved footnote 2:' For maximum flash performance, set to 0b11' to the 'DPFEN' column header. • Deleted the x-refs in the 'DPFEN' column for the rows. • Created a x-ref for footnote 2 and inserted in the 'IPFEN' column header. • Deleted the x-refs in the 'IPFEN' column for the rows. • Moved footnote 3:' For maximum flash performance, set to 0b110' to the 'PFLIM' column header. • Deleted the x-refs in the 'PFLIM' column for the rows. • Moved footnote 4:' For maximum flash performance, set to 0b1' to the 'BFEN' column header. • Deleted the x-refs in the 'BFEN' column for the rows. • Changed footnotes 1, 5, and 6 to become footnotes 5, 6, and 7. Added footnote 8. -- footnote 5 82 MHz parts allow for 80 MHz system clock + 2% frequency modulation (FM). -- footnote 6 102 MHz parts allow for 100 MHz system clock + 2% FM. -- footnote 7 135 MHz parts allow for 132 MHz system clock + 2% FM. -- footnote 8 147 MHz parts allow for 144 MHz system clock + 2% FM. • Footnote 9: added to the end of the 1st column for the 147 MHz row that reads: Preliminary setting. Final setting pending characterization.
Table 17, Pad AC Specifications and Table 18, Derated Pad AC Specifications:	• Footnote 1, deleted 'F_{SYS} = 132 MHz.' • Footnote 2, changed from 'tested' to '(not tested).' • Footnote 3, changed from 'Out delay. . .' to 'The output delay. . .', • Changed from ' Add a maximum of one system clock to the output delay to get the output delay with respect to the system clock' to 'To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.' • Footnote 4: changed 'Delay' to 'The output delay.' • Footnote 5: deleted 'before qualification.' • Changed from 'This parameter is supplied for reference and is not guaranteed by design and not tested' to 'This parameter is supplied for reference and is guaranteed by design and tested.'
Table 19, Reset and Configuration Pin Timing:	Footnote 1, deleted 'F_{SYS} = 132 MHz.'
Table 20, JTAG Pin AC Electrical Characteristics:	• Footnote 1, deleted: ', and CL = 30 pF with DSC = 0b10, SRC = 0b11' • Footnote 1, changed 'functional' to 'Nexus.'
Table 21, Nexus Debug Port Timing.	Changed Spec 12, TCK Low to TDO Data Valid: Changed 'VDDE = 3.0 to 3.6 volts' maximum value in column 4 from 9 to 10. Now reads 'V_{DDE} = 3.0–3.6 V' with a max value of 10.

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 22, Bus Operation Timing:	• Added a column to the table for 72 MHz minimum and maximum bus frequencies. • Spec 1: 72 MHz Min. column = 13.3. • Specs 5 and 6: *CLKOUT positive edge to output signals invalid of high*: Corrected format to show the bus timing values for various frequencies with EBTS bit = 0 and EBTS bit = 1. • Specs 5, and 6: Added the $\overline{BB}$ signal for arbitration. Added the following calibration signals: CAL_ADDR[9:30], CAL_$\overline{CS}$[0:3], CAL_DATA[0:15], CAL_$\overline{OE}$, CAL_RD_$\overline{WR}$, CAL_$\overline{TS}$, CAL_$\overline{WE}$/$\overline{BE}$[0:1]. • Spec 5: EBI and Calibration sections, 72 MHz Min column, EBTS = 0 is 1.0, EBTS = 1 is 1.5. • Spec 6: EBI section, 72 MHz Max column, EBTS = 0 is 5.0, EBTS = 1 is 6.0. • Spec 6a: Calibration section, 72 MHz Max column, EBTS = 0 is 6.0, EBTS = 1 is 7.0 • Specs 7 and 8: Added the $\overline{BB}$ signal for arbitration. Added the following calibration signals: CAL_ADDR[9:30], CAL_DATA[0:15], CAL_RD_$\overline{WR}$, CAL_$\overline{TS}$.
Table 23, External Interrupt Timing:	• Footnote 1: Deleted '. . F_{SYS} = 132 MHz', 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and ' .and CL = 200 pF with SRC = 0b11.' • Deleted second figure after table 'External Interrupt Setup Timing.'
Table 24, eTPU Timing	• Footnote 1: Deleted '. . .F_{SYS} = 132 MHz', 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and 'and CL = 200 pF with SRC = 0b11.' • Deleted second figure, '*eTPU Input/Output Timing*' after this table. • Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).'
Table 25, eMIOS Timing:	• Deleted (MTS) from the heading, table, and footnotes. • Footnote 1: Deleted '. . .F_{SYS} = 132 MHz, 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and 'and CL = 200 pF with SRC = 0b11.' • Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).'
Figure 17, eMIOS Timing: Added figure.	
Table 26, DSPI Timing:	• Added 144 MHz column to the table. • Spec1:*SCK Cycle Time*: changes to values: 80 MHz, min. = 24.4; 112 MHz, min. = 17.5, max = 2.1; 132 MHz, min. = 14.8, max = 1.8; 144 MHz, min. = 13.6, max = 1.6. • Spec1:*SCK Cycle Time*: Added footnote 4 to the 144 MHz min. and max values that reads: Preliminary. Specification pending final characterization • Spec 2, *PCS to SCK delay*, 144 MHz, min. TBD • Spec 3, *After SCK delay*, 144 MHz, min. TBD • Spec 9, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. TBD • Spec 10, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. TBD • Spec 11, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, max TBD • Spec 12, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. TBD • Added to beginning of footnote 1 'All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate.' • Footnote 1: Deleted 'V_{DD} = 1.35–1.65 V' and 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V.