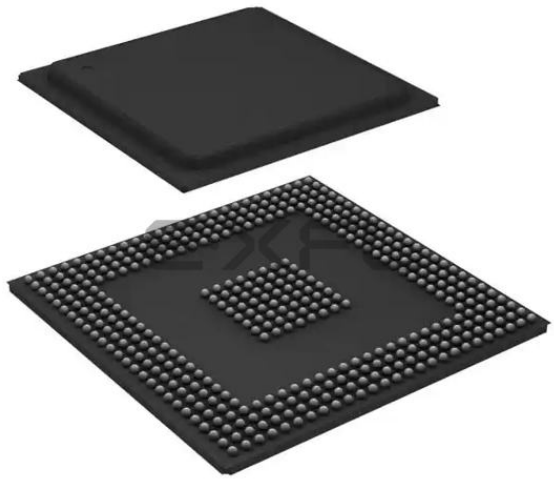

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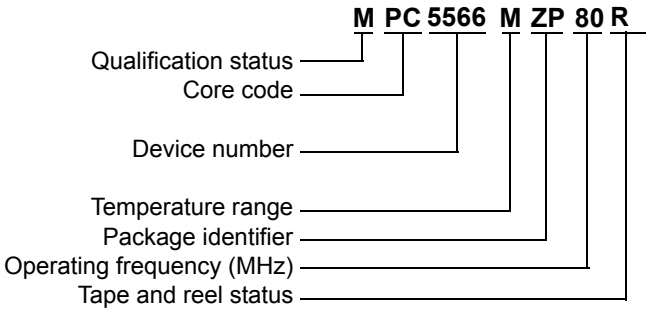
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5566mzp144

2 Ordering Information



Temperature Range
M = –40° C to 125° C

Package Identifier
ZP = 416PBGA SnPb
VR = 416PBGA Pb-free

Operating Frequency
80 = 80 MHz
112 = 112 MHz
132 = 132 MHz
144 = 144 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to Table 1.

Figure 1. MPC5500 Family Part Number Example

Unless noted in this data sheet, all specifications apply from T_L to T_H.

Table 1. Orderable Part Numbers

Freescale Part Number[1]	Package Description	Speed (MHz)		Operating Temperature [2]	
		Nominal	Max. [3] (f_{MAX})	Min. (T_L)	Max. (T_H)
MPC5566MVR144	MPC5566 416 package Lead-free (PbFree)	144	147	–40° C	125° C
MPC5566MVR132		132	135		
MPC5566MVR112		112	114		
MPC5566MVR80		80	82		
MPC5566MZP144	MPC5566 416 package Leaded (SnPb)	144	147	–40° C	125° C
MPC5566MZP132		132	135		
MPC5566MZP112		112	114		
MPC5566MZP80		80	82		

1 All devices are PPC5566, rather than MPC5566 or SPC5566, until product qualifications are complete. Not all configurations are available in the PPC parts.

2 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

3 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; 135 MHz parts allow for 132 MHz system clock + 2% FM; and 147 MHz parts allow for 144 MHz system clock + 2% FM.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings [1, 2]

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	Ω
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins) 750 (corner pins)	V
Number of pulses per pin: Positive pulses (HBM) Negative pulses (HBM)	 — —	 1 1	 — —
Interval of pulses	—	1	second

1 All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

3.6 Voltage Regulator Controller (V_{RC}) and Power-On Reset (POR) Electrical Specifications

The following table lists the V_{RC} and POR electrical specifications:

Table 6. V_{RC} and POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V (V_{DD}) POR [1]	Negated (ramp up) Asserted (ramp down)	V_{POR15}	1.1 1.1	1.35 1.35	V
2	3.3 V (V_{DDSYN}) POR [1]	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	V_{POR33}	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	$\overline{\text{RESET}}$ pin supply (V_{DDEH6}) POR [1, 2]	Negated (ramp up) Asserted (ramp down)	V_{POR5}	2.0 2.0	2.85 2.85	V
4	V_{RC33} voltage	Before V_{RC} allows the pass transistor to start turning on	V_{TRANS_START}	1.0	2.0	V
5		When V_{RC} allows the pass transistor to completely turn on [3, 4]	V_{TRANS_ON}	2.0	2.85	V
6		When the voltage is greater than the voltage at which the V_{RC} keeps the 1.5 V supply in regulation [5, 6]	$V_{VRC33REG}$	3.0	—	V
7	Current can be sourced by V_{RCCTL} at Tj:	–40° C 25° C 150° C	I_{VRCCTL} [7]	11.0 9.0 7.5	— — —	mA mA mA
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27e	Operating current 1.5 V supplies @ 147 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 650 530 820 650 750 585	 mA mA mA mA mA mA
27a	Operating current 1.5 V supplies @ 135 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 630 500 785 630 710 550	 mA mA mA mA mA mA
27b	Operating current 1.5 V supplies @ 114 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 600 450 680 500 650 490	 mA mA mA mA mA mA
27c	Operating current 1.5 V supplies @ 82 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 490 360 545 400 530 395	 mA mA mA mA mA mA
27d	RAM standby current.[12] I_{DD_STBY} @ 25° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 60° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 150° C (Tj) V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V	 I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY}	 — — — — — — — — —	 20 30 50 70 100 200 1200 1500 2000	 µA µA µA µA µA µA µA µA µA

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} [13]	I_{DD_33}	—	2 + (values derived from procedure of footnote [13])	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} (V_{DDA0} + V_{DDA1})	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH}, V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA
30	Operating current V_{DDE} supplies: [14]				
	V_{DDEH1}	I_{DD1}	—	Refer to footnote [14]	mA
	V_{DDE2}	I_{DD2}	—		mA
	V_{DDE3}	I_{DD3}	—		mA
	V_{DDEH4}	I_{DD4}	—		mA
	V_{DDE5}	I_{DD5}	—		mA
	V_{DDEH6}	I_{DD6}	—		mA
	V_{DDE7}	I_{DD7}	—		mA
	V_{DDEH8}	I_{DD8}	—		mA
	V_{DDEH9}	I_{DD9}	—		mA
31	Fast I/O weak pullup current [15]	I_{ACT_F}			
	1.62–1.98 V		10	110	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
	Fast I/O weak pulldown current [15]				
	1.62–1.98 V		10	100	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
32	Slow and medium I/O weak pullup/down current [15]	I_{ACT_S}			
	3.0–3.6 V		10	150	µA
	4.5–5.5 V		20	170	µA
33	I/O input leakage current [16]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [17]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [18]	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	V_{SSA} – 0.1	V_{SSA} + 0.1	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	V_{DDA} – 0.1	V_{DDA} + 0.1	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current ($T_A = T_L$ to T_H)[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

1 These values are estimates from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: [1] Crystal reference External reference Dual controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys} \div 2$	MHz
2	System frequency [2]	f_{sys}	$f_{ICO(MIN)} \div 2^{RFD}$	f_{MAX} [3]	MHz
3	System clock period	t_{CYC}	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency [4]	f_{LOR}	100	1000	kHz
5	Self-clocked mode (SCM) frequency [5]	f_{SCM}	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode [6] All other modes [dual controller (1:1), bypass, external reference]	V_{IHEXT} V_{IHEXT}	V_{XTAL} + 0.4 V $(V_{DDE5} \div 2)$ + 0.4 V	— —	V V
7	EXTAL input low voltage crystal mode [7] All other modes [dual controller (1:1), bypass, external reference]	V_{ILEXT} V_{ILEXT}	— —	V_{XTAL} – 0.4 V $(V_{DDE5} \div 2)$ – 0.4 V	V V
8	XTAL current [8]	I_{XTAL}	2	6	mA
9	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L) - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [9]	pF
13	Discrete load capacitance to connect to XTAL	C_{L_XTAL}	—	$(2 \times C_L) - C_{S\_XTAL} - C_{PCB\_XTAL}$ [9]	pF
14	PLL lock time [10]	t_{lpll}	—	750	µs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) [11, 12]	t_{skew}	–2	2	ns
16	Duty cycle of reference	t_{DC}	40	60	%
17	Frequency unLOCK range	f_{UL}	–4.0	4.0	% f_{SYS}
18	Frequency LOCK range	f_{LCK}	–2.0	2.0	% f_{SYS}

Table 16 shows the FLASH_BIU settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 16. FLASH_BIU Settings vs. Frequency of Operation [1]

Maximum Frequency (MHz)	APC	RWSC	WWSC	DPFEN [2]	IPFEN [2]	PFLIM [3]	BFEN [4]
Up to and including 82 MHz [5]	0b001	0b001	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Up to and including 102 MHz [6]	0b001	0b010	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Up to and including 135 MHz [7]	0b010	0b011	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Up to and including 147 MHz [8]	0b011	0b100	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Default setting after reset	0b111	0b111	0b11	0b00	0b00	0b000	0b0

1 Illegal combinations exist. Use entries from the same row in this table.
2 For maximum flash performance, set to 0b11.
3 For maximum flash performance, set to 0b110.
4 For maximum flash performance, set to 0b1.
5 82 MHz parts allow for 80 MHz system clock + 2% frequency modulation (FM).
6 102 MHz parts allow for 100 MHz system clock + 2% FM.
7 135 MHz parts allow for 132 MHz system clock + 2% FM.
8 147 MHz parts allow for 144 MHz system clock + 2% FM.

3.12 AC Specifications

3.12.1 Pad AC Specifications

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V) [1]

Spec	Pad	SRC / DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [4, 5] (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	26	15	50
			82	60	200
		01	75	40	50
			137	80	200
		00	377	200	50
			476	260	200

Table 19. Reset and Configuration Pin Timing [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
3	PLLCFG, BOOTCFG, WKPCFG, RSTCFG setup time to RSTOUT valid	t_{RCSU}	10	—	t_{CYC}
4	PLLCFG, BOOTCFG, WKPCFG, RSTCFG hold time from RSTOUT valid	t_{RCH}	0	—	t_{CYC}

1 Reset timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

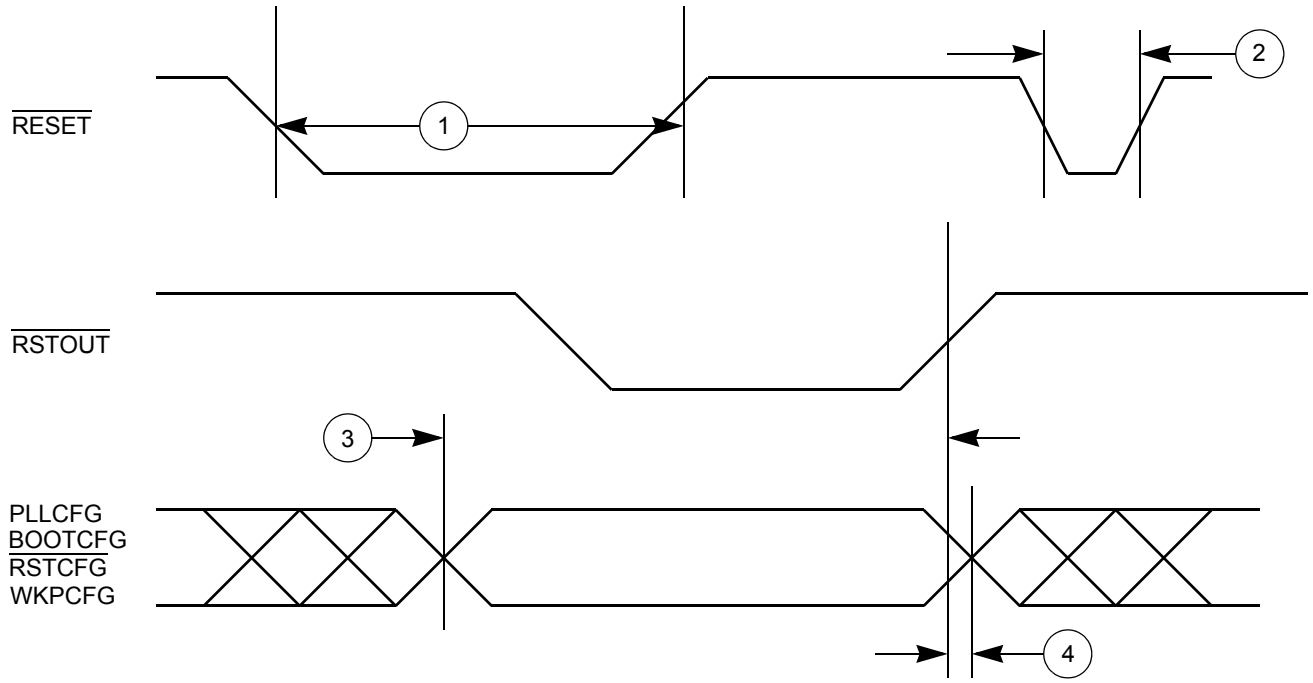


Figure 5. Reset and Configuration Pin Timing

3.13.2 IEEE 1149.1 Interface Timing

Table 20. JTAG Pin AC Electrical Characteristics [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	TCK cycle time	t_{JCYC}	100	—	ns
2	TCK clock pulse width (measured at $V_{DDE} \div 2$)	t_{JDC}	40	60	ns
3	TCK rise and fall times (40% to 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI data setup time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI data hold time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK low to TDO data valid	t_{TDOV}	—	20	ns
7	TCK low to TDO data invalid	t_{TDOI}	0	—	ns
8	TCK low to TDO high impedance	t_{TDOHZ}	—	20	ns
9	JCOMP assertion time	t_{JCMPPW}	100	—	ns
10	JCOMP setup time to TCK low	t_{JCMPS}	40	—	ns
11	TCK falling-edge to output valid	t_{BSDV}	—	50	ns

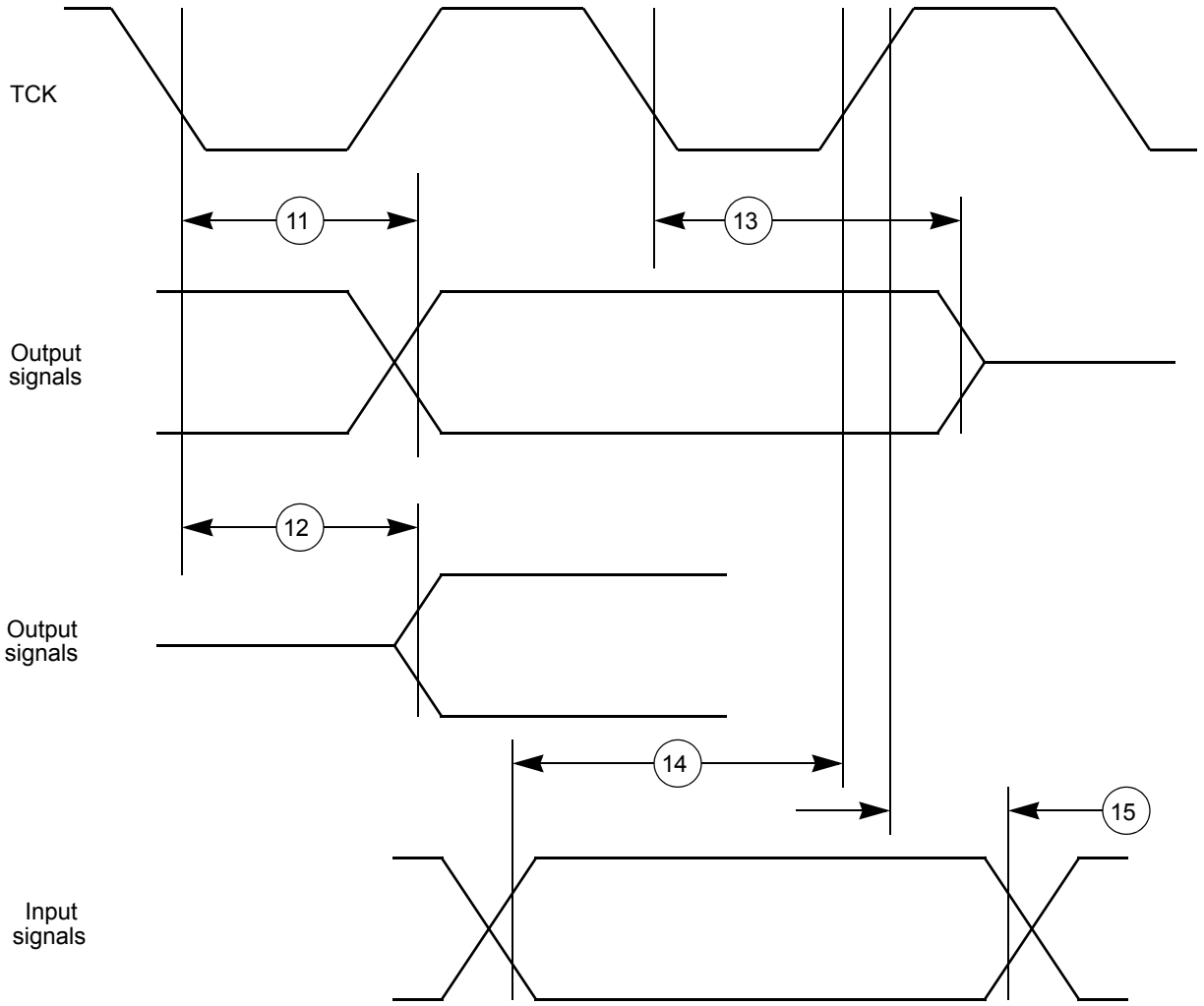


Figure 9. JTAG Boundary Scan Timing

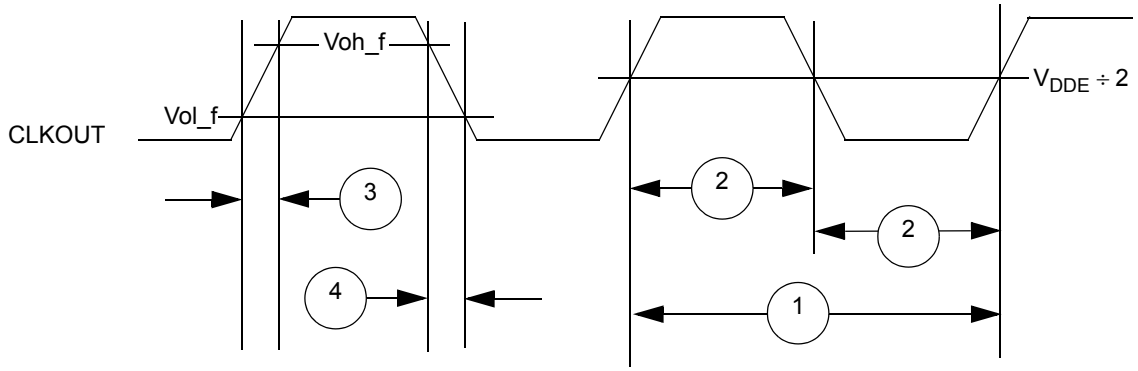


Figure 12. CLKOUT Timing

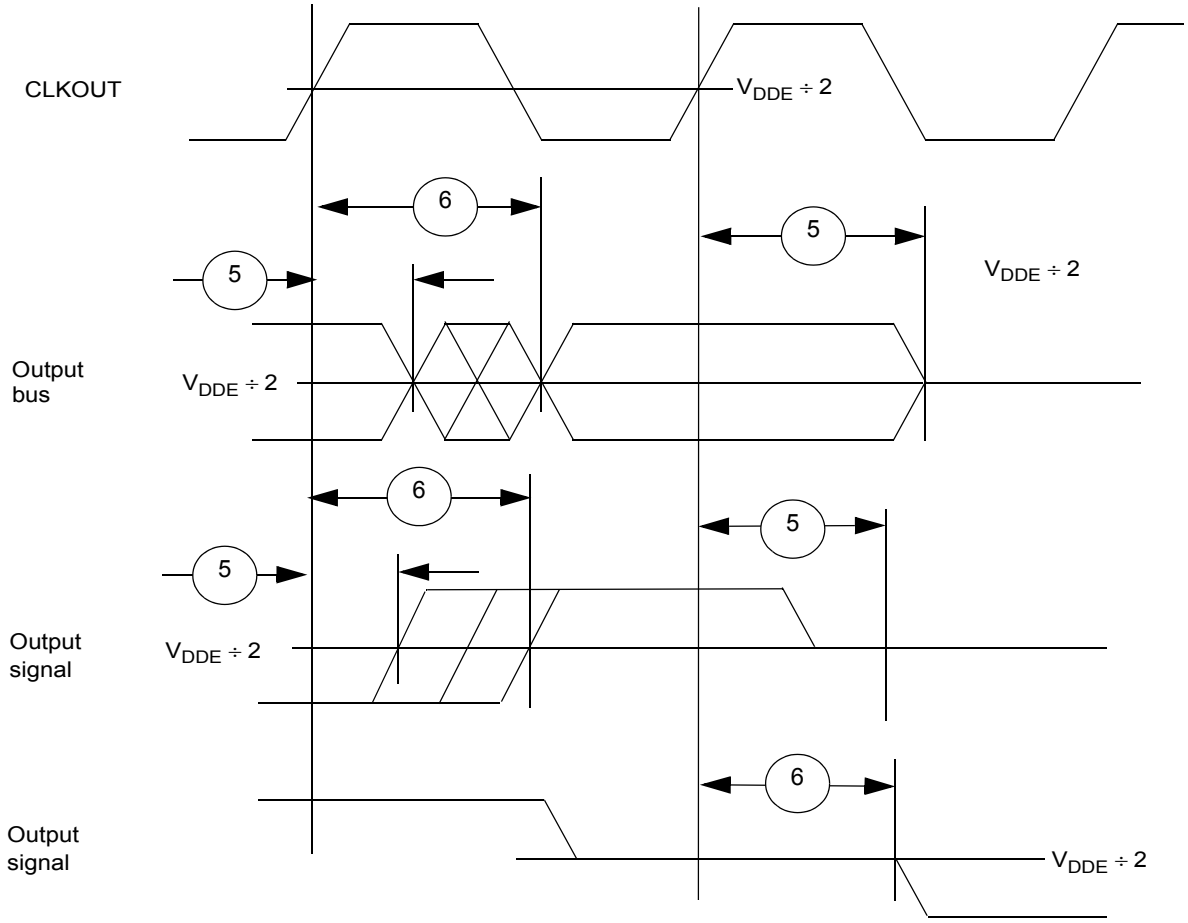


Figure 13. Synchronous Output Timing

3.14.2 MII FEC Transmit Signal Timing FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, FEC_TX_CLK

The transmitter functions correctly up to the FEC_TX_CLK maximum frequency of 25 MHz plus one percent. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

The transmit outputs (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER) can be programmed to transition from either the rising- or falling-edge of TX_CLK, and the timing is the same in either case. These options allow the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the device reference manual for details of this option and how to enable it.

Table 29 lists MII FEC transmit channel timings.

Table 29. MII FEC Transmit Signal Timing

Spec	Characteristic	Min.	Max	Unit
5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	25	ns
7	FEC_TX_CLK pulse-width high	35%	65%	FEC_TX_CLK period
8	FEC_TX_CLK pulse-width low	35%	65%	FEC_TX_CLK period

Figure 29 shows MII FEC transmit signal timings listed in Table 29.

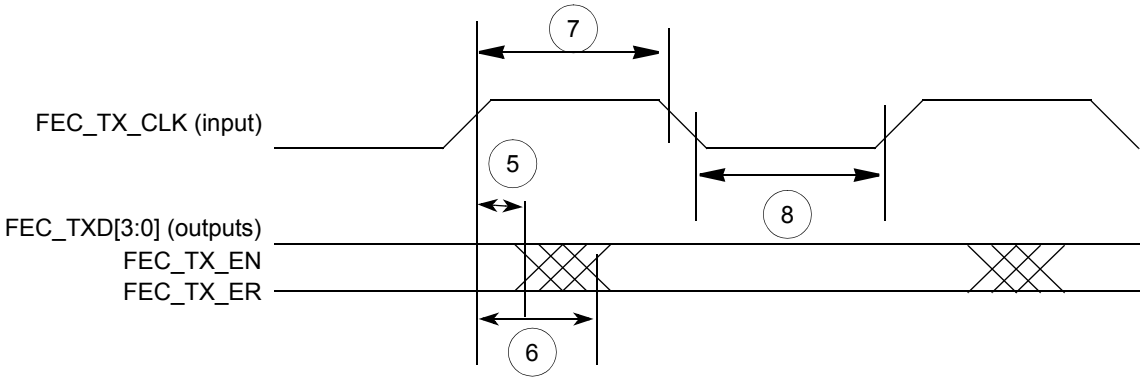


Figure 29. MII FEC Transmit Signal Timing Diagram

3.14.3 MII FEC Asynchronous Inputs Signal Timing FEC_CRS and FEC_COL

Table 30 lists MII FEC asynchronous input signal timing.

Table 30. MII FEC Asynchronous Inputs Signal Timing

Spec	Characteristic	Min.	Max	Unit
9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

Figure 30 shows MII FEC asynchronous input timing listed in Table 30.

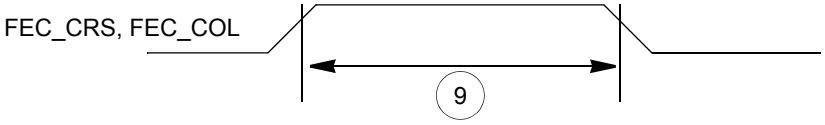


Figure 30. MII FEC Asynchronous Inputs Timing Diagram

3.14.4 MII FEC Serial Management Channel Timing FEC_MDIO and FEC_MDC

Table 31 lists MII FEC serial management channel timing. The FEC functions correctly with a maximum FEC_MDC frequency of 2.5 MHz.

Table 31. MII FEC Serial Management Channel Timing

Spec	Characteristic	Min.	Max	Unit
10	FEC_MDC falling-edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
11	FEC_MDC falling-edge to FEC_MDIO output valid (maximum propagation delay)	—	25	ns
12	FEC_MDIO (input) to FEC_MDC rising-edge setup	10	—	ns
13	FEC_MDIO (input) to FEC_MDC rising-edge hold	0	—	ns
14	FEC_MDC pulse-width high	40%	60%	FEC_MDC period
15	FEC_MDC pulse-width low	40%	60%	FEC_MDC period

Figure 31 shows MII FEC serial management channel timing listed in Table 31.

4 Mechanicals

4.1 MPC5566 416 PBGA Pinout

Figure 32, Figure 33, and Figure 34 show the pinout for the MPC5566 416 PBGA package. The alternate Fast Ethernet Controller (FEC) signals are multiplexed with the data calibration bus signals.

NOTE

The MPC5500 devices are pin compatible for software portability and use the primary function names to label the pins in the BGA diagram. Although some devices do not support all the primary functions shown in the BGA diagram, the muxed and GPIO signals on those pins remain available. See the signals chapter in the device reference manual for the signal muxing.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VSTBY	AN37	AN11	VDDA1	AN16	AN1	AN5	VRH	AN23	AN27	AN28	AN35	VSSA0	AN15	ETRIG 1	ETPUB 18	ETPUB 20	ETPUB 24	ETPUB 27	GPIO 205	MDO11	MDO8	VDD	VDD33	VSS	A
B	VDD	VSS	AN36	AN39	AN19	AN20	AN0	AN4	REF BYPC	AN22	AN26	AN31	AN32	VSSA0	AN14	ETRIG 0	ETPUB 21	ETPUB 25	ETPUB 28	ETPUB 31	MDO10	MDO7	MDO4	MDO0	VSS	VDDE7	B
C	VDD33	VDD	VSS	AN8	AN17	VSSA1	AN21	AN3	AN7	VRL	AN25	AN30	AN33	VDDA0	AN13	ETPUB 19	ETPUB 22	ETPUB 26	ETPUB 30	MDO9	MDO6	MDO3	MDO1	VSS	VDDE7	VDD	C
D	ETPUA 30	ETPUA 31	VDD	VSS	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34	VDDEH 9	AN12	ETPUB 16	ETPUB 17	ETPUB 23	ETPUB 29	MDO5	MDO2	VDDEH 8	VSS	VDDE7	TCK	TDI	D
E	ETPUA 28	ETPUA 29	VDDEH 1	VDD																			VDDE7	TMS	TDO	TEST	E
F	ETPUA 24	ETPUA 27	ETPUA 26	VDDEH 1																			MSEO0	JCOMP	EVTI	EVTO	F
G	ETPUA 23	ETPUA 22	ETPUA 25	ETPUA 21																			MSEO1	MCKO	GPIO 204	ETPUB 15	G
H	ETPUA 20	ETPUA 19	ETPUA 18	ETPUA 17																			RDY	GPIO 203	ETPUB 14	ETPUB 13	H
J	ETPUA 16	ETPUA 15	ETPUA 14	ETPUA 13																			VDDEH 6	ETPUB 12	ETPUB 11	ETPUB 9	J
K	ETPUA 12	ETPUA 11	ETPUA 10	ETPUA 9						VSS	VSS	VSS	VSS	VDDE7	VDDE7	VDDE7	VDDE7						ETPUB 10	ETPUB 8	ETPUB 7	ETPUB 5	K
L	ETPUA 8	ETPUA 7	ETPUA 6	ETPUA 5						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDE7						ETPUB 6	ETPUB 4	ETPUB 3	ETPUB 2	L
M	ETPUA 4	ETPUA 3	ETPUA 2	ETPUA 1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VDDE7						TCRCLK B	ETPUB 1	ETPUB 0	SINB	M
N	BDIP	TEA	ETPUA 0	TCRCLK A						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VDDE7						SOUTB	PCSB3	PCSB0	PCSB1	N
P	CS3	CS2	CS1	CS0						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						PCSA3	PCSB4	SCKB	PCSB2	P
R	WE3	WE2	WE1	WE0						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						PCSB5	SOUTA	SINA	SCKA	R
T	VDDE2	TSIZ0	RD_WR	VDDE2						VDDE2	VSS	VDDE2	VDDE2	VDDE2	VDDE2	VSS	VSS						PCSA1	PCSA0	PCSA2	VPP	T
U	ADDR 16	TSIZ1	TA	VDD33						VSS	VDDE2	VDDE2	VDDE2	VDDE2	VDDE2	VSS	VSS						PCSA4	TXDA	PCSA5	VFLASH	U
V	ADDR 18	ADDR 17	TS	ADDR 8																			CNTXC	RXDA	RSTOUT	RST CFG	V
W	ADDR 20	ADDR 19	ADDR 9	ADDR 10																			RXDB	CNRXC	TXDB	RESET	W
Y	ADDR 22	ADDR 21	ADDR 11	VDDE2						Note:	NC	No connect. AC22 & AD23 reserved											WKP CFG	BOOT CFG1	VRC VSS	VSS SYN	Y
AA	ADDR 24	ADDR 23	ADDR 13	ADDR 12																			VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL	AA
AB	VDDE2	ADDR 25	ADDR 15	ADDR 14																			VDD	VRC CTL	PLL CFG0	XTAL	AB
AC	ADDR 26	ADDR 27	ADDR 31	VSS	VDD	DATA 26	DATA 28	VDDE2	DATA 30	DATA 31	DATA 8	DATA 10	VDDE2	DATA 12	DATA 14	EMIOS 2	EMIOS 8	EMIOS 12	EMIOS 21	VDDEH 4	VDDE5	NC	VSS	VDD	VRC33	VDD SYN	AC
AD	ADDR 28	ADDR 30	VSS	VDD	DATA 24	DATA 25	DATA 27	DATA 29	VDD33	GPIO 207	DATA 9	DATA 11	DATA 13	DATA 15	EMIOS 3	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC	VSS	VDD	VDD33	AD
AE	ADDR 29	VSS	VDD	DATA 17	DATA 19	DATA 21	DATA 23	DATA 0	DATA 2	DATA 4	DATA 6	OE	BR	BG	EMIOS 1	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD	AE
AF	VSS	VDD	DATA 16	DATA 18	VDDE2	DATA 20	DATA 22	GPIO 206	DATA 1	DATA 3	VDDE2	DATA 5	DATA 7	BB	EMIOS 0	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 32. MPC5566 416 Package

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
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	CASE NUMBER: 1494–01	13 JUL 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 36. MPC5566 416 TEPBGA Package (continued)

5.3 Information Changed Between Revisions 0.0 and 1.0

The following table lists the global changes made throughout the document, as well as the changes to sections of text not contained in a figure or table.

Table 34. Global and Text Changes Between Rev. 0.0 and 1.0

Location	Description of Changes

Global Changes	• Third paragraph and throughout the document, replaced:
	  • kilobytes with KB.
	  • megabytes with MB.
	• Put overbars on the following signals: $\overline{BB}$, $\overline{BG}$, $\overline{BR}$, $\overline{BDIP}$, $\overline{OE}$, $\overline{TA}$, $\overline{TEA}$, $\overline{TS}$,
	• Changed $\overline{WE}$[0:3]/$\overline{BE}$[0:3] to $\overline{WE}$/$\overline{BE}$[0:3].
	• Added a 144 MHz system frequency option for the MPC5566 microcontroller.

Section 1, “Overview”:	• First paragraph, text changed from “ based on the PowerPC Book E architecture” to “built on the Power Architecture embedded technology.” • Second paragraph: Changed terminology from PowerPC Book E architecture to Power Architecture terminology. • Added new fourth paragraph about VLE feature. • Paragraph nine: changed “the MPC5566 has an on-chip 20-channel enhanced queued analog-to-digital converter (eQADC)” to “has an on-chip 40-channel dual enhanced queued” • Added paragraph about the Fast Ethernet Controller directly after the System Integration Unit paragraph. • Added the sentence directly preceding Table 1: ‘Unless noted in this data sheet, all specifications apply from T_L to T_H.’
3.7.1, 3.7.2 and 3.7.3: Reordered sections resulting in the following order and section renumbering:	• Section 3.7.1, “Input Value of Pins During POR Dependent on VDD33,” then • Section 3.7.2, “Power-Up Sequence (VRC33 Grounded),” then • Section 3.7.3, “Power-Down Sequence (VRC33 Grounded).
Section 3.7.1, “Input Value of Pins During POR Dependent on VDD33,” changed:	From: ‘To avoid accidentally selecting the bypass clock because PLLCFG[0:1] and $\overline{RSTCFG}$ are not treated as ones (1s) when POR negates, V_{DD33} must not lag V_{DDSYN} and the $\overline{RESET}$ pin power (V_{DDEH6}) when powering the device by more than the V_{DD33} lag specification in Table 6. V_{DD33} individually can lag either V_{DDSYN} or the $\overline{RESET}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification. V_{DD33} can lag one of the V_{DDSYN} or V_{DDEH6} supplies, but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.’ To: ‘When powering the device, V_{DD33} must not lag V_{DDSYN} and the $\overline{RESET}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and RSTCFG are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} or the $\overline{RESET}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.’

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 2, Absolute Maximum Ratings:	• Deleted Spec 3, “Flash core voltage.” • Spec 12 “DC Input Voltage”: Deleted from second line‘. . .except for eTPUB15 and SINB (DSPI_B_SIN)’ leaving V_{DDEH} powered I/O pads. Deleted third line ‘V_{DDEH} powered by I/O pads (eTPUB15 and SINB), including the min. and max values of -0.3 and 6.5 respectively, and deleted old footnote 7. • Spec 12 “DC Input Voltage”: Added footnote 8 to second line “V_{DDE} powered I/O pads” that reads: ‘Internal structures hold the input voltage less than the maximum voltage on all pads powered by the V_{DDE} supplies, if the maximum injection current specification is met (s mA for all pins) and V_{DDE} is within the operating voltage specifications. • Spec 14, column 2, changed: ‘V_{SS} differential voltage’ to ‘V_{SS} to V_{SSA} differential voltage.’ • Spec 15, column 2, changed: ‘V_{DD} differential voltage’ to ‘V_{DD} to V_{DDA} differential voltage.’ • Spec 21, Added the name of the spec, ‘*V_{RC33} to V_{DDSYN} differential voltage,’* as well as the name and cross reference to Table 9, *DC Electrical Specification*s, to which the Spec was moved. • Spec 28 “Maximum Solder Temperature”: Added two subordinate lines: Lead free (PbFree) and Leaded (SnPb) with maximum values of 260 C and 245 C respectively. • Footnote 1, added: ‘any of’ between ‘beyond’ and ‘the listed maxima.’ • Deleted footnote 2: ‘Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.’Spec 26 “Maximum Operating Temperature Range”: replaced -40 C with T_L. • Footnote 6 (now footnote 5): Changed to the following sentence to the end, “Internal structures hold the input voltage greater than -1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than -0.6 V on eTPU[15] and on SINB during the internal power-on reset (POR) state.”
Table 4, EMI Testing Specifications:	• Changed the maximum operating frequency to from 132 to f_{MAX}. • Footnote 2: Deleted ‘Refer to Table 1 for the maximum operating frequency.’

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 5, ESD Characteristics: Added (Electromagnetic Static Discharge) in the table title.	

Table 6, VCR/POR Electrical Specifications:	• Added footnote 1 to specs 1, 2, and 3 that reads: On power up, assert $\overline{\text{RESET}}$ before V_{POR15}, V_{POR33}, and V_{POR5} negate (internal POR). RESET must remain asserted until the power supplies are within the operating conditions as specified in Table 9 *DC Electrical Specifications*. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.
	• Subscript all symbol names that appear after the first underscore character.
	• Specs 7 and 10: added 'at Tj ' at the end of the first line in the second column: Characteristic.
	• Removed 'Tj ' after '150 C' in the last line, second column: Characteristic.
	• Spec 10, second column, second line:
	Added cross-reference to footnote 6: 'I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.' Changed '(@ V_{DD} = 1.35 V, $f_{sys} = f_{MAX}$)' to '(@ $f_{sys} = f_{MAX}$).'
	• Footnote 10: Deleted 'Preliminary value. Final specification pending characterization."
	• Added to Spec 2:
	3.3 V (V_{DDSYN}) POR negated (ramp down) Min 0.0 Max 0.30 V
	3.3 V (V_{DDSYN}) POR asserted (ramp up) Min 0.0 Max 0.30 V
	• Added new footnote 1 to both lines in Spec 3: " V_{IL_S} (Table 9, Spec 15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.
	• Spec 5: Changed old Footnote 1 (now footnote 2): 'User must be able to supply full operating current for the 1.5V supply when the 3.3V supply reaches this range." to 'Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range."
	• Spec 3: Added new footnote 3 for both lines: 'It is possible to reach the current limit during ramp up--do not treat this event as a short circuit current.'
	• Spec 10:
	  • Changed the minimum values of: -40 C = 60; 25 C = 65.
	  • Added old footnote 5 new footnote 6.
	  • Added a new footnote 7, 'Refer to Table 1 for the maximum operating frequency.'
	  • Rewrote old footnote 7(new footnote 9) to: Represents the worst-case external transistor BETA. It is measured on a per part basis and calculated as (I_{DD} ÷ I_{VRCCTL}).
	• Deleted old footnote 8: 'Preliminary value. Final specification pending characterization.'

Table 7, Power Sequence Pin Status for Fast Pads:	• Changed title to *Pin Status for Fast Pads During the Power Sequence* • Changed preceding paragraph From: Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies depending on power. Prior to exiting POR, the pads are in a high impedance state (Hi-Z). To: There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up/down varies depending on which supplies are powered. • Deleted the 'Comment' column. • Added a POR column after the V_{DD} column. • Added row 2:' V_{DDE}, Low, Low, Asserted, High' and row 5: V_{DDE}, V_{DD33}, V_{DD}, Asserted, Hi-Z.
Table 8, Power Sequence Pin Status for Medium/Slow Pads:	• Changed title to *Pin Status for Medium and Slow Pads During the Power Sequence* • Updated preceding paragraph. • Deleted the 'Comment' column. • Added a POR column after the V_{DD} column. • Added row 3:' V_{DDEH}, V_{DD}, Asserted, Hi-Z.'

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 9, DC Electrical Specifications:	• Spelled out meaning of the slash '/' as 'and' as well as 'I/O' as 'input/output.' Sentence still very confusing. Deleted 'input/output' from the specs to improve clarity. • Spec 20, column 2, *Characteristics*,' Slow and medium output high voltage (I_{OH_S} = –2.0 mA):' Created a left-justified second line and moved 'I_{OH_S} = –2.0 mA' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OH_S} = –1.0 mA.' • Spec 20, column 4, *Min*: Added a blank line before and after '0.80 × V_{DDEH}' and put '0.85 × V_{DDEH}' on the last line. • Spec 22, column 2, '*Slow and medium output low voltage (I_{OL_S} = 2.0 mA)*:' Created a left-justified second line and moved 'I_{OL_S} = 2.0 mA.' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OL_S} = 1.0 mA.' • Spec 22, column 5, *Max*: Added a blank line before and after '0.20 × V_{DDEH}' and put '0.15 × V_{DDEH}' on the last line. • Spec 26: Changed 'AN[12]_MA[1]_SDO' to 'AN[13]_MA[1]_SDO'. • Added footnote 10 to specs 27a, b, and c on the 4-way cache line that reads: Four-way cache enabled (L1CSR0[CORG] = 0b1) or (L1CSR0[CORG] = 0b0 with L1CSR0[WAM] = 0b1, L1CSR0[WID] = 0b1111, L1CSR0[WDD] = 0b1111, L1CSR0[AWID] = 0b1, and L1CSR0[AWDD] = 0b1). • Added footnote 11 to specs 27a, b, and c on the max numeric values: "Preliminary. Specification pending final characterization." • Added footnote 12 to specs 27a, b, and c on the max TBD values: "Specification pending final characterization." • Spec 27a: *Operating current 1.5 V supplies @ 132 MHz*: Changed 132 MHz to 135 MHz. Changed maximum values for 8-way cache: All 8-way cache max values have footnote 18. -- 1.65 typical = 630 -- 1.35 typical = 500 -- 1.65 high = 785 -- 1.35 high = 630 Changed 4-way cache with footnote 10: -- 1.65 high = 685 -- 1.35 high = TBD with footnote 19. • Spec 27b, *Operating current 1.5 V supplies @ 114 MHz*: Changed maximum values for 8-way cache. All 8-way cache max values have footnote 18: -- 1.65 typical = 600 -- 1.35 typical = 450 -- 1.65 high = 680 -- 1.35 high = 500 Changed 4-way cache values: -- 1.65 high = TBD with footnote 19 -- 1.35 high = TBD with footnote 19 • Spec 27c, *Operating current 1.5 V supplies @ 82 MHz*: Changed maximum values for 8-way cache: All 8-way cache max values have footnote 18. -- 1.65 typical = 490, -- 1.35 typical = 360, -- 1.65 high = 520, -- 1.35 high = 390. Changed 4-way cache values: -- 1.65 high = TBD with footnote 19 -- 1.35 high = TBD with footnote 19

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Document Number: MPC5566
Rev. 3
9/2012