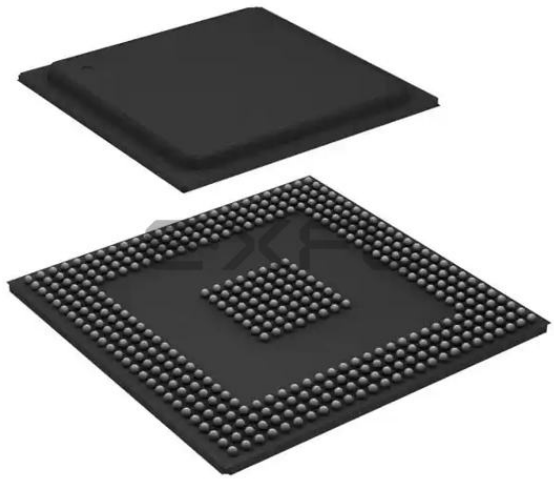

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5566mvr144

3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Rd.
San Jose, CA., 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.3 Package

The MPC5566 is available in packaged form. Read the package options in Section 2, “Ordering Information.” Refer to Section 4, “Mechanicals,” for pinouts and package drawings.

3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications [1]

Spec	Characteristic	Minimum	Typical	Maximum	Unit
1	Scan range	0.15	—	1000	MHz
2	Operating frequency	—	—	f_{MAX}	MHz
3	V_{DD} operating voltages	—	1.5	—	V
4	V_{DDSYN}, V_{RC33}, V_{DD33}, V_{FLASH}, V_{DDE} operating voltages	—	3.3	—	V
5	V_{PP}, V_{DDEH}, V_{DDA} operating voltages	—	5.0	—	V
6	Maximum amplitude	—	—	14 [2] 32 [3]	dBuV
7	Operating temperature	—	—	25	°C

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

2 Measured with the single-chip EMI program.

3 Measured with the expanded EMI program.

1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} [13]	I_{DD_33}	—	2 + (values derived from procedure of footnote [13])	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} (V_{DDA0} + V_{DDA1})	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH}, V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA
30	Operating current V_{DDE} supplies: [14]				
	V_{DDEH1}	I_{DD1}	—	Refer to footnote [14]	mA
	V_{DDE2}	I_{DD2}	—		mA
	V_{DDE3}	I_{DD3}	—		mA
	V_{DDEH4}	I_{DD4}	—		mA
	V_{DDE5}	I_{DD5}	—		mA
	V_{DDEH6}	I_{DD6}	—		mA
	V_{DDE7}	I_{DD7}	—		mA
	V_{DDEH8}	I_{DD8}	—		mA
	V_{DDEH9}	I_{DD9}	—		mA
31	Fast I/O weak pullup current [15]	I_{ACT_F}			
	1.62–1.98 V		10	110	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
	Fast I/O weak pulldown current [15]				
	1.62–1.98 V		10	100	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
32	Slow and medium I/O weak pullup/down current [15]	I_{ACT_S}			
	3.0–3.6 V		10	150	µA
	4.5–5.5 V		20	170	µA
33	I/O input leakage current [16]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [17]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [18]	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	V_{SSA} – 0.1	V_{SSA} + 0.1	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	V_{DDA} – 0.1	V_{DDA} + 0.1	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
41	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
42	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	–50	50	mV
43	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	–100	100	mV
43a	V_{RC33} to V_{DDSYN} differential voltage	$V_{RC33} - V_{DDSYN}$	–0.1	0.1 [19]	V
44	Analog input differential signal range (with common mode 2.5 V)	V_{IDIFF}	–2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L$ to $T_H)$	T_L	T_H	°C
46	Slew rate on power-supply pins	—	—	50	V/ms

1 V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if SIU_ECCR[EBTS] = 1.

2 $| V_{DDA0} - V_{DDA1} |$ must be < 0.1 V.

3 V_{PP} can drop to 3.0 V during read operations.

4 If standby operation is not required, connect V_{STBY} to ground.

5 Applies to CLKOUT, external bus pins, and Nexus pins.

6 Maximum average RMS DC current.

7 Eight-way cache enabled (L1CSR0[CORG] = 0b0).

8 Average current measured on automotive benchmark.

9 Peak currents can be higher on specialized code.

10 High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an ‘idle’ loop that crosses cache lines is run from cache. Write code to avoid this condition.

11 Four-way cache enabled (L1CSR0[CORG] = 0b1) or (L1CSR0[CORG] = 0b0 with L1CSR0[WAM] = 0b1, L1CSR0[WID] = 0b1111, L1CSR0[WDD] = 0b1111, L1CSR0[AWID] = 0b1, and L1CSR0[AWDD] = 0b1).

12 The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, “Power-Up/Down Sequencing”, Figure 2.

13 Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to Table 11 for values to calculate the power dissipation for a specific operation.

14 Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

15 Absolute value of current, measured at V_{IL} and V_{IH}.

16 Weak pullup/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

17 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 °C to 12 °C, in the ambient temperature range of 50 °C to 125 °C. Applies to pad types: pad_a and pad_ae.

18 V_{SSA} refers to both V_{SSA0} and V_{SSA1}. $| V_{SSA0} - V_{SSA1} |$ must be < 0.1 V.

19 Up to 0.6 V during power up and power down.

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

Table 12. FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at f_{SYS} max: [13, 14] Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	C_{JITTER}	 — —	 5.0 0.01	% f_{CLKOUT}
20	Frequency modulation range limit [15] (do not exceed f_{sys} maximum)	C_{MOD}	0.8	2.4	$\%f_{SYS}$
21	ICO frequency $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ [16] $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$	f_{ico}	48	f_{MAX}	MHz
22	Predivider output frequency (to PLL)	f_{PREDIV}	4	20 [17]	MHz

1 Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

2 All internal registers retain data at 0 Hz.

3 Up to the maximum frequency rating of the device (refer to Table 1).

4 Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

5 The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below f_{LOR}. SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

6 Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). (V_{extal} – V_{xtal}) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

7 Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). (V_{xtal} – V_{extal}) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

8 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

9 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

10 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

11 PLL is operating in 1:1 PLL mode.

12 V_{DDE} = 3.0–3.6 V.

13 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

14 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

15 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

16 $f_{sys} = f_{ico} \div (2^{RFD})$.

17 Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

3.11 H7Fa Flash Memory Electrical Characteristics

Table 14. Flash Program and Erase Specifications ($T_A = T_L$ to T_H)

Spec	Flash Program Characteristic	Symbol	Min.	Typical [1]	Initial Max. [2]	Max. [3]	Unit
3	Doubleword (64 bits) program time [4]	$T_{dwprogram}$	—	10	—	500	µs
4	Page program time [4]	$T_{pprogram}$	—	22	44 [5]	500	µs
7	16 KB block pre-program and erase time	$T_{16kpperase}$	—	265	400	5000	ms
9	48 KB block pre-program and erase time	$T_{48kpperase}$	—	345	400	5000	ms
10	64 KB block pre-program and erase time	$T_{64kpperase}$	—	415	500	5000	ms
8	128 KB block pre-program and erase time	$T_{128kpperase}$	—	500	1250	7500	ms
11	Minimum operating frequency for program and erase operations [6]	—	25	—	—	—	MHz

1 Typical program and erase times are calculated at 25 ^{o}C operating temperature using nominal supply values.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Page size is 256 bits (8 words).

6 The read frequency of the flash can range up to the maximum operating frequency. There is no minimum read frequency condition.

Table 15. Flash EEPROM Module Life ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min.	Typical [1]	Unit
1a	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
1b	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	P/E	1000	100,000	cycles
2	Data retention Blocks with 0–1,000 P/E cycles Blocks with 1,001–100,000 P/E cycles	Retention	 20 5	 — —	years

1 Typical endurance is evaluated at 25^{o} C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of typical endurance, refer to engineering bulletin EB619 Typical Endurance for Nonvolatile Memory.

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V) [1] (continued)

Spec	Pad	SRC / DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [4, 5] (ns)	Load Drive (pF)
2	Medium high voltage (MH)	11	16	8	50
			43	30	200
		01	34	15	50
			61	35	200
		00	192	100	50
			239	125	200
3	Fast	00	3.1	2.7	10
		01		2.5	20
		10		2.4	30
		11		2.3	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9000	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 1.62–1.98 V; V_{DDEH} = 4.5–5.25 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and T_A = T_L to T_H.

2 This parameter is supplied for reference and is guaranteed by design (not tested).

3 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

4 The output delay and rise and fall are measured to 20% or 80% of the respective signal.

5 This parameter is guaranteed by characterization rather than 100% tested.

Table 18. Derated Pad AC Specifications (V_{DDEH} = 3.3 V, V_{DDE} = 3.3 V) [1]

Spec	Pad	SRC/DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [3, 5] (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium high voltage (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200

Table 19. Reset and Configuration Pin Timing [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
3	PLLCFG, BOOTCFG, WKPCFG, RSTCFG setup time to RSTOUT valid	t_{RCSU}	10	—	t_{CYC}
4	PLLCFG, BOOTCFG, WKPCFG, RSTCFG hold time from RSTOUT valid	t_{RCH}	0	—	t_{CYC}

1 Reset timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

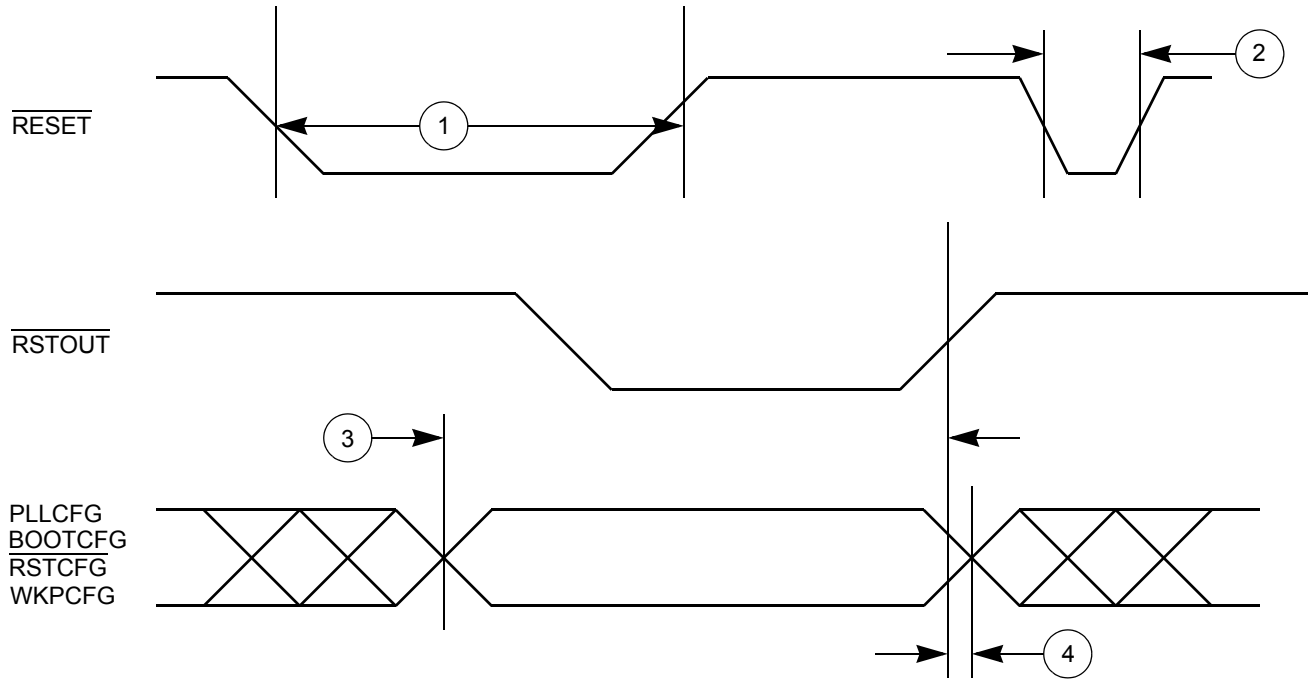

Figure 5. Reset and Configuration Pin Timing

3.13.2 IEEE 1149.1 Interface Timing

Table 20. JTAG Pin AC Electrical Characteristics [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	TCK cycle time	t_{JCYC}	100	—	ns
2	TCK clock pulse width (measured at $V_{DDE} \div 2$)	t_{JDC}	40	60	ns
3	TCK rise and fall times (40% to 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI data setup time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI data hold time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK low to TDO data valid	t_{TDOV}	—	20	ns
7	TCK low to TDO data invalid	t_{TDOI}	0	—	ns
8	TCK low to TDO high impedance	t_{TDOHZ}	—	20	ns
9	JCOMP assertion time	t_{JCMPPW}	100	—	ns
10	JCOMP setup time to TCK low	t_{JCMPS}	40	—	ns
11	TCK falling-edge to output valid	t_{BSDV}	—	50	ns

Table 20. JTAG Pin AC Electrical Characteristics [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
12	TCK falling-edge to output valid out of high impedance	t_{BSDVZ}	—	50	ns
13	TCK falling-edge to output high impedance (Hi-Z)	t_{BSDHZ}	—	50	ns
14	Boundary scan input valid to TCK rising-edge	t_{BSDST}	50	—	ns
15	TCK rising-edge to boundary scan input invalid	t_{BSDHT}	50	—	ns

1 These specifications apply to JTAG boundary scan only. JTAG timing specified at: V_{DDE} = 3.0–3.6 V and $T_A = T_L$ to T_H. Refer to Table 21 for Nexus specifications.

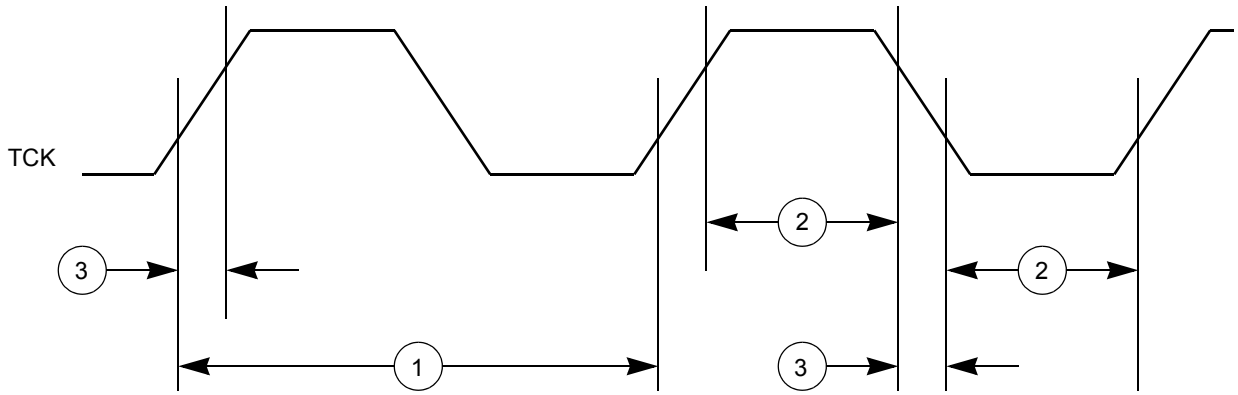

Figure 6. JTAG Test Clock Input Timing

Table 22. Bus Operation Timing [1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]								Unit	Notes
			40 MHz		56 MHz		67 MHz		72 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
7a	Input signal valid to CLKOUT positive edge (setup time) Calibration bus interface CAL_ADDR[9:30] CAL_DATA[0:15] CAL_RD_WR CAL_TS	t_{CCIS}	11.0	—	8.0	—	6.0	—	4.0	—	ns	
8	CLKOUT positive edge to input signal invalid (hold time) External bus interface ADDR[8:31] DATA[0:31] BG [7] BR [5] BB RD_WR TA TEA TS TSIZ[0:1]	t_{CIH}	1.0	—	1.0	—	1.0	—	1.0	—	ns	
	CLKOUT positive edge to input signal invalid (hold time) Calibration bus interface CAL_ADDR[9:30] CAL_DATA[0:15] CAL_RD_WR CAL_TS	t_{CCIH}	1.0	—	1.0	—	1.0	—	1.0	—	ns	

1 EBI timing specified at V_{DDE} = 1.6–3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and CL = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM): 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; 135 MHz parts allow for 132 MHz system clock + 2% FM; and 147 MHz parts allow for 144 MHz system clock + 2% FM.

3 The external bus is limited to half the speed of the internal bus.

4 Refer to fast pad timing in Table 17 and Table 18 (different values for 1.8 V and 3.3 V).

5 Internal arbitration.

6 EBTS = 0 timings are tested and valid at V_{DDE} = 2.25–3.6 V only; EBTS = 1 timings are tested and valid at V_{DDE} = 1.6–3.6 V.

7 External arbitration.

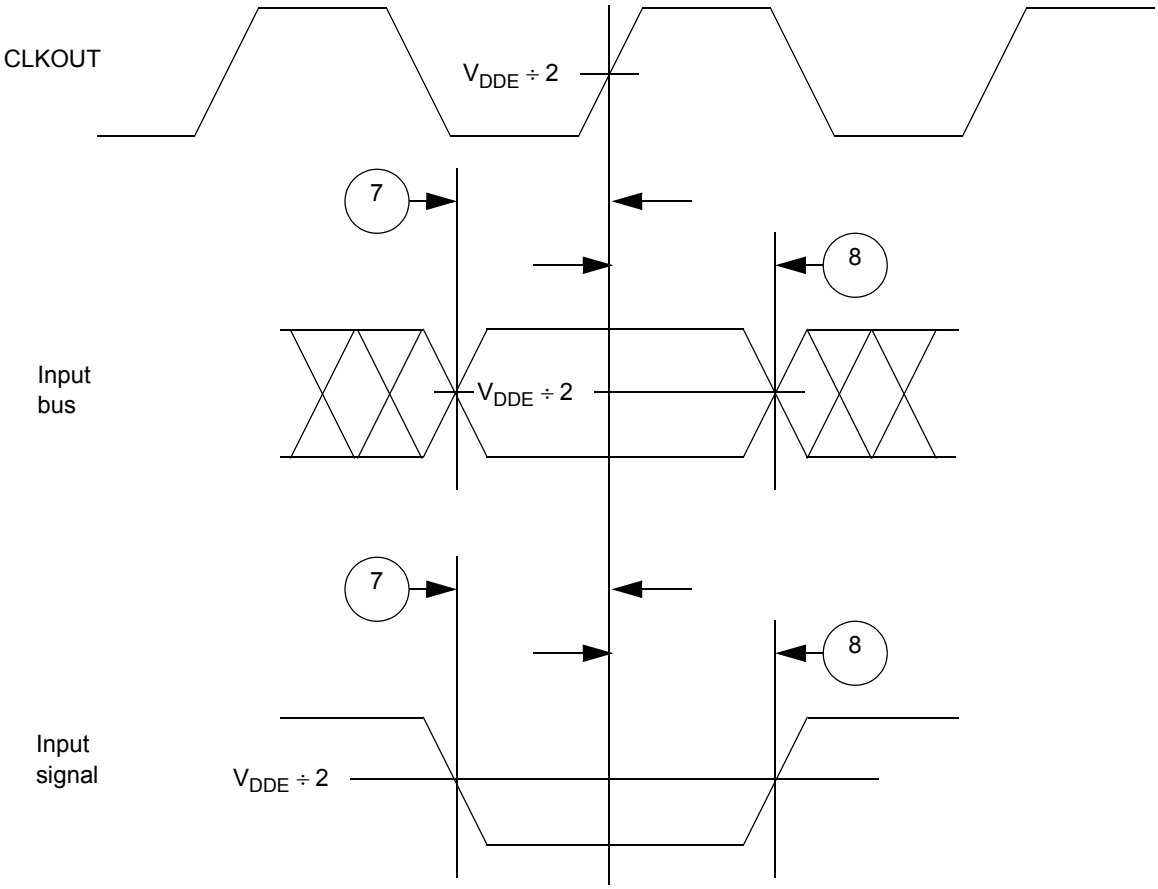

Figure 14. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Signals)

Table 23. External Interrupt Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	IRQ pulse-width low	t_{IPWL}	3	—	t_{CYC}
2	IRQ pulse-width high	T_{IPWH}	3	—	t_{CYC}
3	IRQ edge-to-edge time [2]	t_{ICYC}	6	—	t_{CYC}

1 IRQ timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

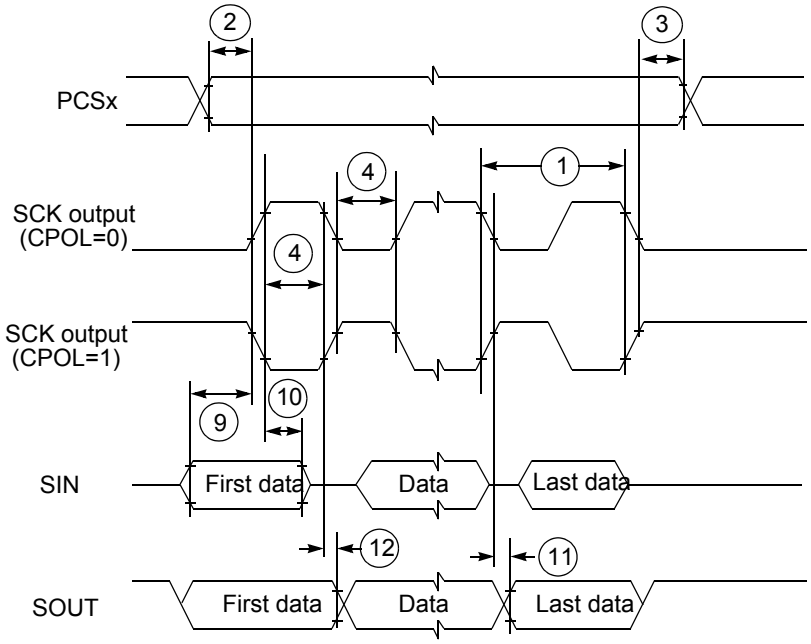

Figure 18. DSPI Classic SPI Timing—Master, CPHA = 0

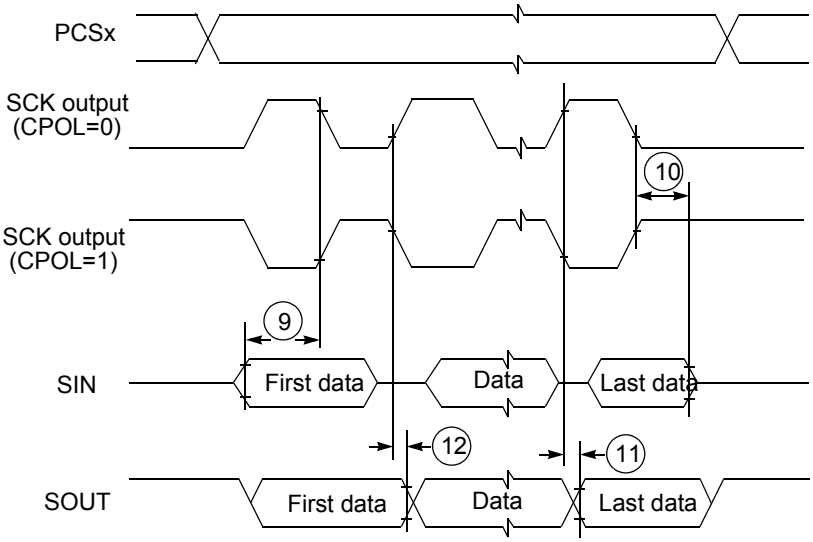

Figure 19. DSPI Classic SPI Timing—Master, CPHA = 1

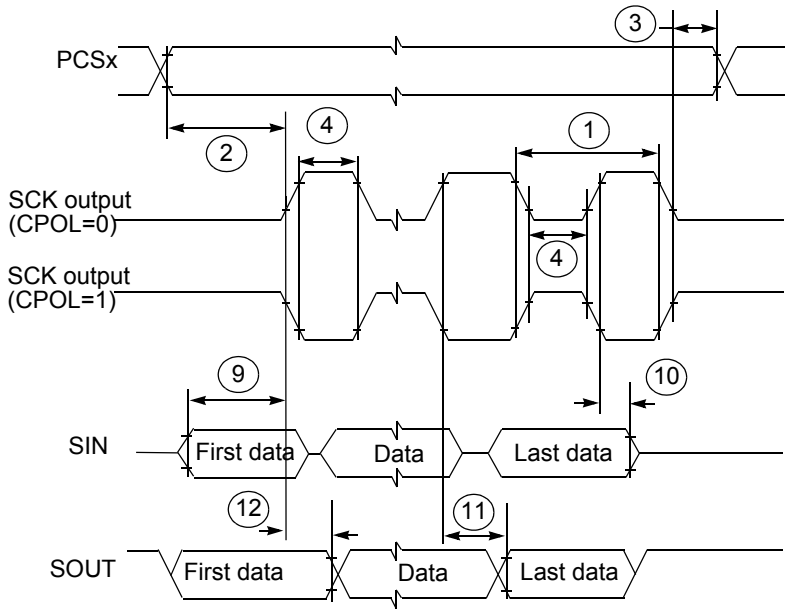

Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 0

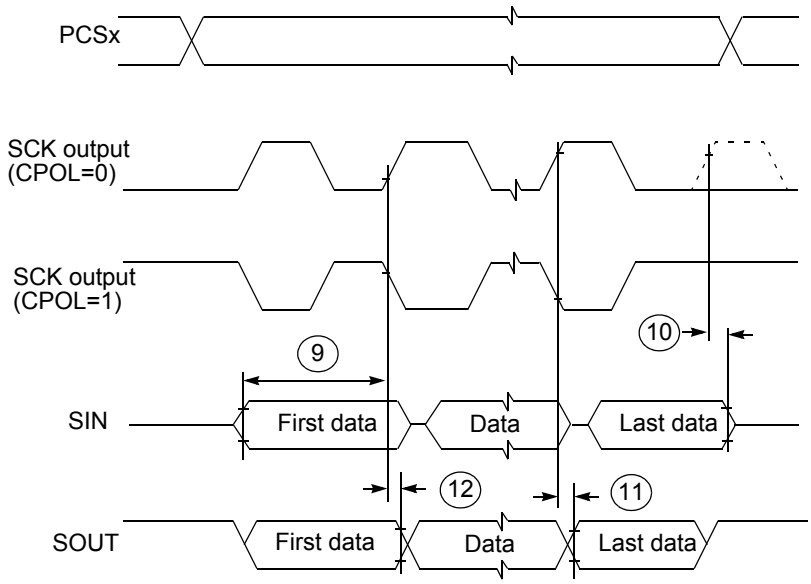

Figure 23. DSPI Modified Transfer Format Timing—Master, CPHA = 1

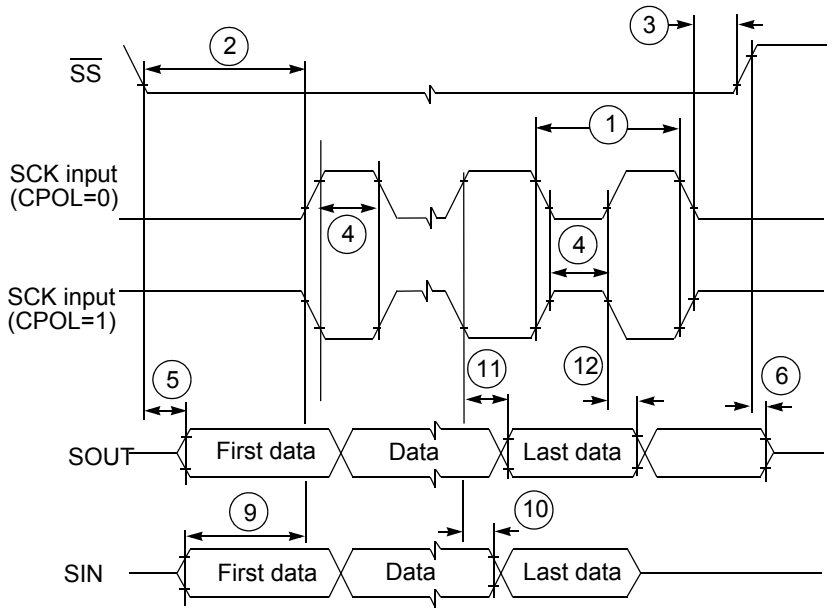

Figure 24. DSPI Modified Transfer Format Timing—Slave, CPHA = 0

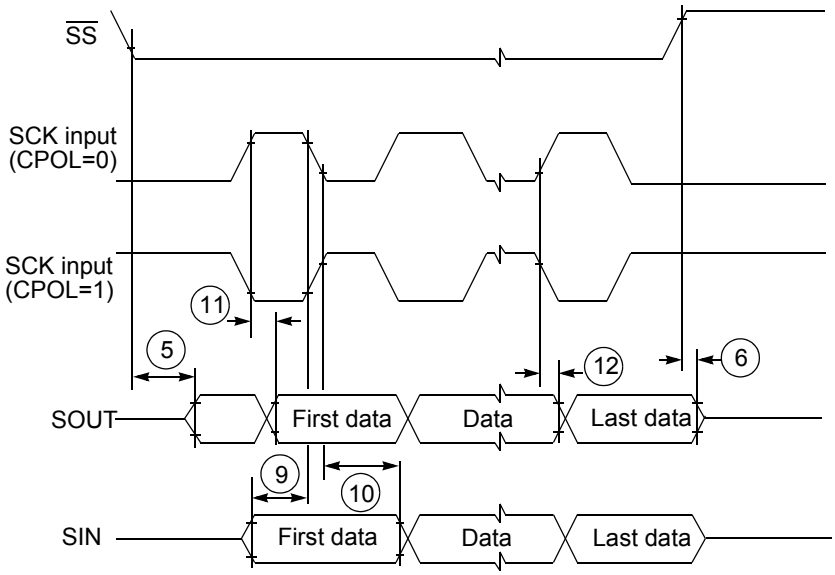

Figure 25. DSPI Modified Transfer Format Timing—Slave, CPHA = 1

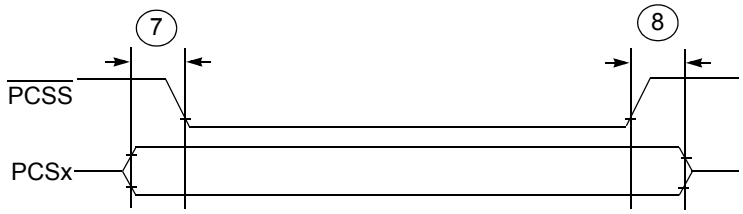

Figure 26. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

3.14.2 MII FEC Transmit Signal Timing FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, FEC_TX_CLK

The transmitter functions correctly up to the FEC_TX_CLK maximum frequency of 25 MHz plus one percent. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

The transmit outputs (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER) can be programmed to transition from either the rising- or falling-edge of TX_CLK, and the timing is the same in either case. These options allow the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the device reference manual for details of this option and how to enable it.

Table 29 lists MII FEC transmit channel timings.

Table 29. MII FEC Transmit Signal Timing

Spec	Characteristic	Min.	Max	Unit
5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	25	ns
7	FEC_TX_CLK pulse-width high	35%	65%	FEC_TX_CLK period
8	FEC_TX_CLK pulse-width low	35%	65%	FEC_TX_CLK period

Figure 29 shows MII FEC transmit signal timings listed in Table 29.

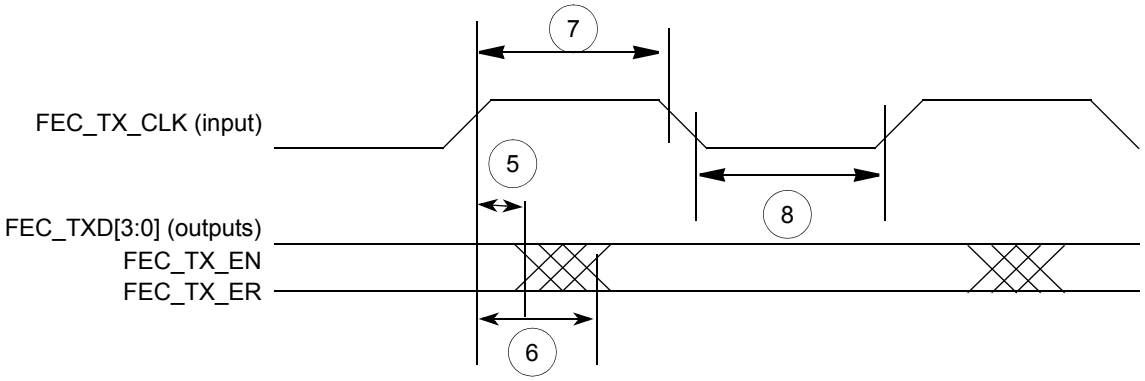

Figure 29. MII FEC Transmit Signal Timing Diagram

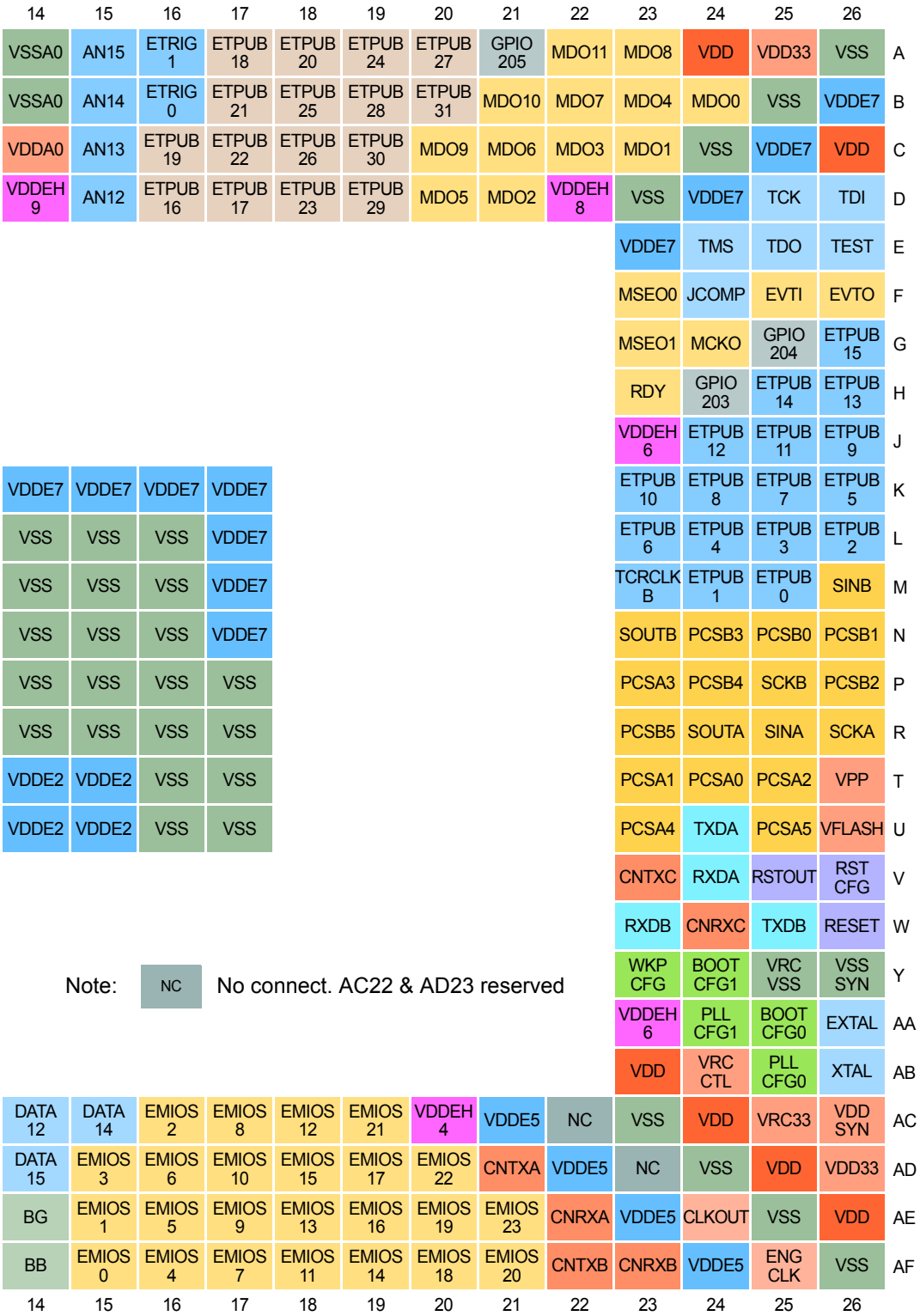

Figure 34. MPC5566 416 Package Right Side (view 2 of 2)

Figure 35. MPC5567 416 Package

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 9, DC Electrical Specifications:	• Spelled out meaning of the slash '/' as 'and' as well as 'I/O' as 'input/output.' Sentence still very confusing. Deleted 'input/output' from the specs to improve clarity. • Spec 20, column 2, *Characteristics*,' Slow and medium output high voltage (I_{OH_S} = –2.0 mA):' Created a left-justified second line and moved 'I_{OH_S} = –2.0 mA' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OH_S} = –1.0 mA.' • Spec 20, column 4, *Min*: Added a blank line before and after '0.80 × V_{DDEH}' and put '0.85 × V_{DDEH}' on the last line. • Spec 22, column 2, '*Slow and medium output low voltage (I_{OL_S} = 2.0 mA)*:' Created a left-justified second line and moved 'I_{OL_S} = 2.0 mA.' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OL_S} = 1.0 mA.' • Spec 22, column 5, *Max*: Added a blank line before and after '0.20 × V_{DDEH}' and put '0.15 × V_{DDEH}' on the last line. • Spec 26: Changed 'AN[12]_MA[1]_SDO' to 'AN[13]_MA[1]_SDO'. • Added footnote 10 to specs 27a, b, and c on the 4-way cache line that reads: Four-way cache enabled (L1CSR0[CORG] = 0b1) or (L1CSR0[CORG] = 0b0 with L1CSR0[WAM] = 0b1, L1CSR0[WID] = 0b1111, L1CSR0[WDD] = 0b1111, L1CSR0[AWID] = 0b1, and L1CSR0[AWDD] = 0b1). • Added footnote 11 to specs 27a, b, and c on the max numeric values: "Preliminary. Specification pending final characterization." • Added footnote 12 to specs 27a, b, and c on the max TBD values: "Specification pending final characterization." • Spec 27a: *Operating current 1.5 V supplies @ 132 MHz*: Changed 132 MHz to 135 MHz. Changed maximum values for 8-way cache: All 8-way cache max values have footnote 18. -- 1.65 typical = 630 -- 1.35 typical = 500 -- 1.65 high = 785 -- 1.35 high = 630 Changed 4-way cache with footnote 10: -- 1.65 high = 685 -- 1.35 high = TBD with footnote 19. • Spec 27b, *Operating current 1.5 V supplies @ 114 MHz*: Changed maximum values for 8-way cache. All 8-way cache max values have footnote 18: -- 1.65 typical = 600 -- 1.35 typical = 450 -- 1.65 high = 680 -- 1.35 high = 500 Changed 4-way cache values: -- 1.65 high = TBD with footnote 19 -- 1.35 high = TBD with footnote 19 • Spec 27c, *Operating current 1.5 V supplies @ 82 MHz*: Changed maximum values for 8-way cache: All 8-way cache max values have footnote 18. -- 1.65 typical = 490, -- 1.35 typical = 360, -- 1.65 high = 520, -- 1.35 high = 390. Changed 4-way cache values: -- 1.65 high = TBD with footnote 19 -- 1.35 high = TBD with footnote 19