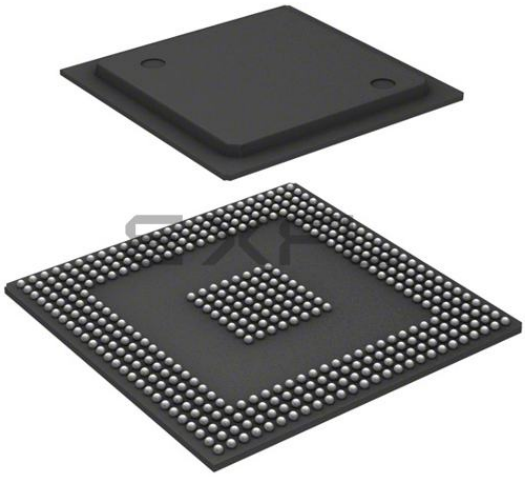

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5566mzp144

The MPC5500 family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565x.

The host processor core of the MPC5566 also includes an instruction set enhancement allowing variable length encoding (VLE). This allows optional encoding of mixed 16- and 32-bit instructions. With this enhancement, it is possible to significantly reduce the code size footprint.

The MPC5566 has two levels of memory hierarchy. The fastest accesses are to the 32-kilobytes (KB) unified cache. The next level in the hierarchy contains the 128-KB on-chip internal SRAM and three-megabytes (MB) internal flash memory. The internal SRAM and flash memory hold instructions and data. The external bus interface is designed to support most of the standard memories used with the MPC5*xx* family.

The complex input/output timer functions of the MPC5566 are performed by two enhanced time processor unit (eTPU) engines. Each eTPU engine controls 32 hardware channels, providing a total of 64 hardware channels. The eTPU has been enhanced over the TPU by providing: 24-bit timers, double-action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU is programmed using a high-level programming language.

The less complex timer functions of the MPC5566 are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPIs), and enhanced serial communications interfaces (eSCIs). The DSPIs support pin reduction through hardware serialization and deserialization of timer channels and general-purpose input/output (GPIOs) signals.

The MCU has an on-chip enhanced queued dual analog-to-digital converter (eQADC).s 40-channels.

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also determined by the SIU. The internal multiplexer submodule provides multiplexing of eQADC trigger sources, daisy chaining the DSPIs, and external interrupt signal multiplexing.

The Fast Ethernet (FEC) module is a RISC-based controller that supports both 10 and 100 Mbps Ethernet/IEEE® 802.3 networks and is compatible with three different standard MAC (media access controller) PHY (physical) interfaces to connect to an external Ethernet bus. The FEC supports the 10 or 100 Mbps MII (media independent interface), and the 10 Mbps-only with a seven-wire interface, which uses a subset of the MII signals. The upper 16-bits of the 32-bit external bus interface (EBI) are used to connect to an external Ethernet device. The FEC contains built-in transmit and receive message FIFOs and DMA support.

3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings [1, 2]

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	Ω
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins) 750 (corner pins)	V
Number of pulses per pin: Positive pulses (HBM) Negative pulses (HBM)	 — —	 1 1	 — —
Interval of pulses	—	1	second

1 All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

3.6 Voltage Regulator Controller (V_{RC}) and Power-On Reset (POR) Electrical Specifications

The following table lists the V_{RC} and POR electrical specifications:

Table 6. V_{RC} and POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V (V_{DD}) POR [1]	Negated (ramp up) Asserted (ramp down)	V_{POR15}	1.1 1.1	1.35 1.35	V
2	3.3 V (V_{DDSYN}) POR [1]	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	V_{POR33}	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	$\overline{\text{RESET}}$ pin supply (V_{DDEH6}) POR [1, 2]	Negated (ramp up) Asserted (ramp down)	V_{POR5}	2.0 2.0	2.85 2.85	V
4	V_{RC33} voltage	Before V_{RC} allows the pass transistor to start turning on	V_{TRANS_START}	1.0	2.0	V
5		When V_{RC} allows the pass transistor to completely turn on [3, 4]	V_{TRANS_ON}	2.0	2.85	V
6		When the voltage is greater than the voltage at which the V_{RC} keeps the 1.5 V supply in regulation [5, 6]	$V_{VRC33REG}$	3.0	—	V
7	Current can be sourced by V_{RCCTL} at Tj:	–40° C 25° C 150° C	I_{VRCCTL} [7]	11.0 9.0 7.5	— — —	mA mA mA
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V

1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27e	Operating current 1.5 V supplies @ 147 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 650 530 820 650 750 585	 mA mA mA mA mA mA
27a	Operating current 1.5 V supplies @ 135 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 630 500 785 630 710 550	 mA mA mA mA mA mA
27b	Operating current 1.5 V supplies @ 114 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 600 450 680 500 650 490	 mA mA mA mA mA mA
27c	Operating current 1.5 V supplies @ 82 MHz: [6] 8-way cache [7] V_{DD} (including V_{DDF} max current) @1.65 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.35 V typical use [8, 9] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10] 4-way cache [11] V_{DD} (including V_{DDF} max current) @1.65 V high use [9, 10] V_{DD} (including V_{DDF} max current) @1.35 V high use [9, 10]	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 490 360 545 400 530 395	 mA mA mA mA mA mA
27d	RAM standby current.[12] I_{DD_STBY} @ 25° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 60° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 150° C (Tj) V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V	 I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY}	 — — — — — — — — —	 20 30 50 70 100 200 1200 1500 2000	 µA µA µA µA µA µA µA µA µA

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} [13]	I_{DD_33}	—	2 + (values derived from procedure of footnote [13])	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} (V_{DDA0} + V_{DDA1})	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH}, V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA
30	Operating current V_{DDE} supplies: [14]				
	V_{DDEH1}	I_{DD1}	—	Refer to footnote [14]	mA
	V_{DDE2}	I_{DD2}	—		mA
	V_{DDE3}	I_{DD3}	—		mA
	V_{DDEH4}	I_{DD4}	—		mA
	V_{DDE5}	I_{DD5}	—		mA
	V_{DDEH6}	I_{DD6}	—		mA
	V_{DDE7}	I_{DD7}	—		mA
	V_{DDEH8}	I_{DD8}	—		mA
	V_{DDEH9}	I_{DD9}	—		mA
31	Fast I/O weak pullup current [15]	I_{ACT_F}			
	1.62–1.98 V		10	110	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
	Fast I/O weak pulldown current [15]				
	1.62–1.98 V		10	100	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
32	Slow and medium I/O weak pullup/down current [15]	I_{ACT_S}			
	3.0–3.6 V		10	150	µA
	4.5–5.5 V		20	170	µA
33	I/O input leakage current [16]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [17]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [18]	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	V_{SSA} – 0.1	V_{SSA} + 0.1	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	V_{DDA} – 0.1	V_{DDA} + 0.1	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: [1] Crystal reference External reference Dual controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys} \div 2$	MHz
2	System frequency [2]	f_{sys}	$f_{ICO(MIN)} \div 2^{RFD}$	f_{MAX} [3]	MHz
3	System clock period	t_{CYC}	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency [4]	f_{LOR}	100	1000	kHz
5	Self-clocked mode (SCM) frequency [5]	f_{SCM}	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode [6] All other modes [dual controller (1:1), bypass, external reference]	V_{IHEXT} V_{IHEXT}	V_{XTAL} + 0.4 V $(V_{DDE5} \div 2)$ + 0.4 V	— —	V V
7	EXTAL input low voltage crystal mode [7] All other modes [dual controller (1:1), bypass, external reference]	V_{ILEXT} V_{ILEXT}	— —	V_{XTAL} – 0.4 V $(V_{DDE5} \div 2)$ – 0.4 V	V V
8	XTAL current [8]	I_{XTAL}	2	6	mA
9	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L) - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [9]	pF
13	Discrete load capacitance to connect to XTAL	C_{L_XTAL}	—	$(2 \times C_L) - C_{S\_XTAL} - C_{PCB\_XTAL}$ [9]	pF
14	PLL lock time [10]	t_{lpll}	—	750	µs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) [11, 12]	t_{skew}	–2	2	ns
16	Duty cycle of reference	t_{DC}	40	60	%
17	Frequency unLOCK range	f_{UL}	–4.0	4.0	% f_{SYS}
18	Frequency LOCK range	f_{LCK}	–2.0	2.0	% f_{SYS}

3.11 H7Fa Flash Memory Electrical Characteristics

Table 14. Flash Program and Erase Specifications ($T_A = T_L$ to T_H)

Spec	Flash Program Characteristic	Symbol	Min.	Typical [1]	Initial Max. [2]	Max. [3]	Unit
3	Doubleword (64 bits) program time [4]	$T_{dwprogram}$	—	10	—	500	µs
4	Page program time [4]	$T_{pprogram}$	—	22	44 [5]	500	µs
7	16 KB block pre-program and erase time	$T_{16kpperase}$	—	265	400	5000	ms
9	48 KB block pre-program and erase time	$T_{48kpperase}$	—	345	400	5000	ms
10	64 KB block pre-program and erase time	$T_{64kpperase}$	—	415	500	5000	ms
8	128 KB block pre-program and erase time	$T_{128kpperase}$	—	500	1250	7500	ms
11	Minimum operating frequency for program and erase operations [6]	—	25	—	—	—	MHz

1 Typical program and erase times are calculated at 25 ^{o}C operating temperature using nominal supply values.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Page size is 256 bits (8 words).

6 The read frequency of the flash can range up to the maximum operating frequency. There is no minimum read frequency condition.

Table 15. Flash EEPROM Module Life ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min.	Typical [1]	Unit
1a	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
1b	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	P/E	1000	100,000	cycles
2	Data retention Blocks with 0–1,000 P/E cycles Blocks with 1,001–100,000 P/E cycles	Retention	 20 5	 — —	years

1 Typical endurance is evaluated at 25^{o} C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of typical endurance, refer to engineering bulletin EB619 Typical Endurance for Nonvolatile Memory.

Table 22. Bus Operation Timing [1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]								Unit	Notes
			40 MHz		56 MHz		67 MHz		72 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
6	CLKOUT positive edge to output signal *valid* (output delay) External bus interface CS[0:3] ADDR[8:31] DATA[0:31] BDIP BG [5] BR [7] BB OE RD_WR TA TEA TS TSIZ[0:1] WE/BE[0:3]	t_{COV}	—	10.0 [6] 11.0	—	7.5 [6] 8.5	—	6.0 [6] 7.0	—	5.0 [6] 6.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.
6a	CLKOUT positive edge to output signal valid (output delay) Calibration bus interface CAL_CS[0:3] CAL_ADDR[9:30] CAL_DATA[0:15] CAL_OE CAL_RD_WR CAL_TS CAL_WE/BE[0:1]	t_{CCOV}	—	11.0 [6] 12.0	—	8.5 [6] 9.5	—	7.0 [6] 8.0	—	6.0 [6] 7.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.
7	Input signal valid to CLKOUT positive edge (setup time) External bus interface ADDR[8:31] DATA[0:31] BG [7] BR [5] BB RD_WR TA TEA TS TSIZ[0:1]	t_{CIS}	10.0	—	7.0	—	5.0	—	4.0	—	ns	

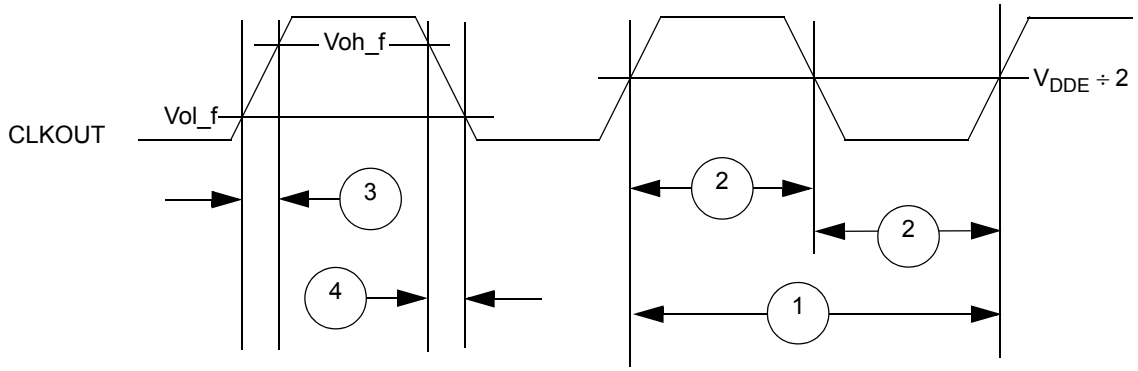

Figure 12. CLKOUT Timing

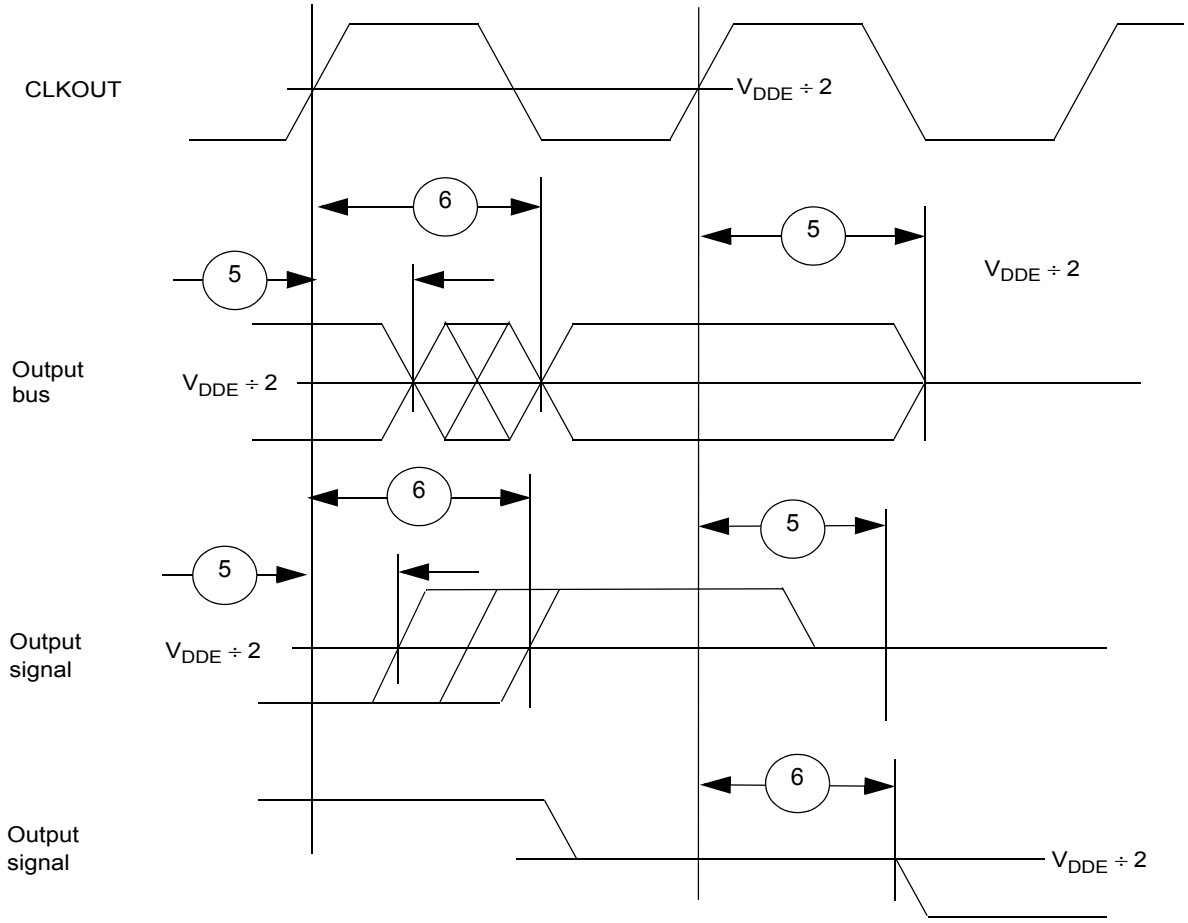

Figure 13. Synchronous Output Timing

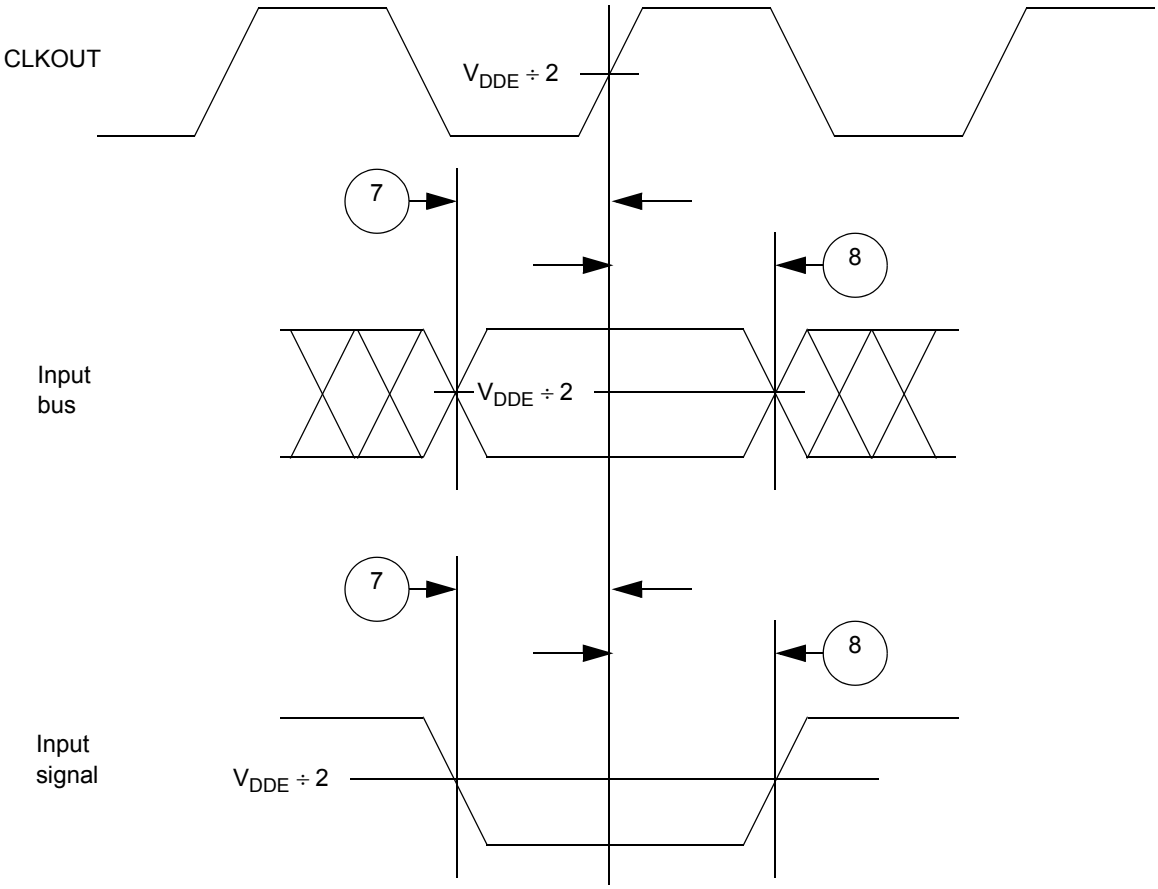

Figure 14. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Signals)

Table 23. External Interrupt Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	IRQ pulse-width low	t_{IPWL}	3	—	t_{CYC}
2	IRQ pulse-width high	T_{IPWH}	3	—	t_{CYC}
3	IRQ edge-to-edge time [2]	t_{ICYC}	6	—	t_{CYC}

1 IRQ timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

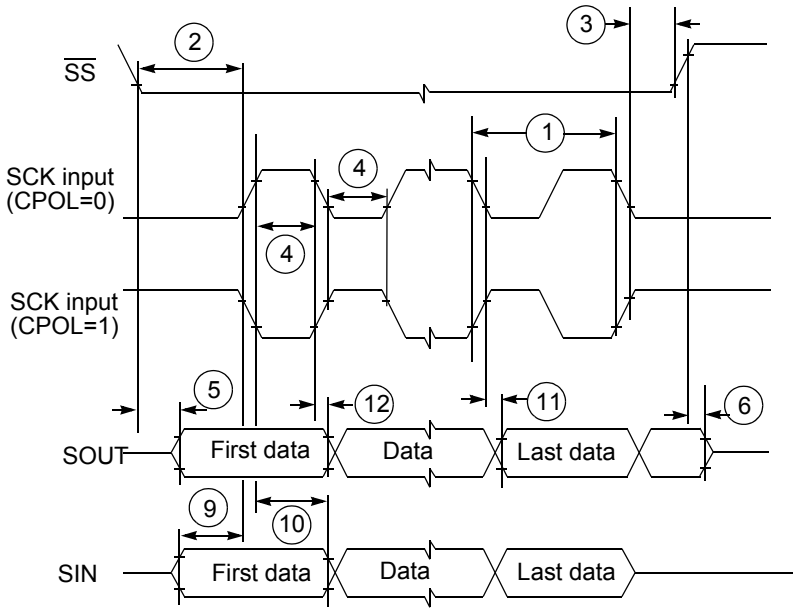

Figure 20. DSPI Classic SPI Timing—Slave, CPHA = 0

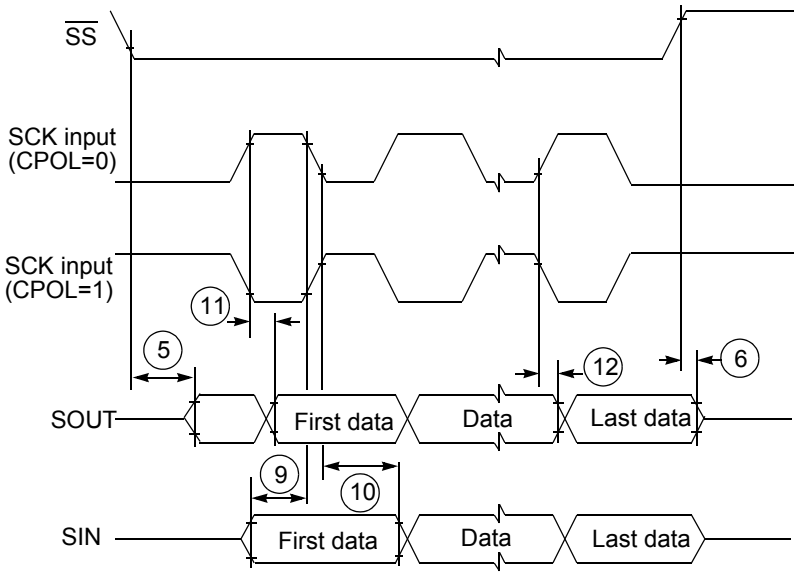

Figure 21. DSPI Classic SPI Timing—Slave, CPHA = 1

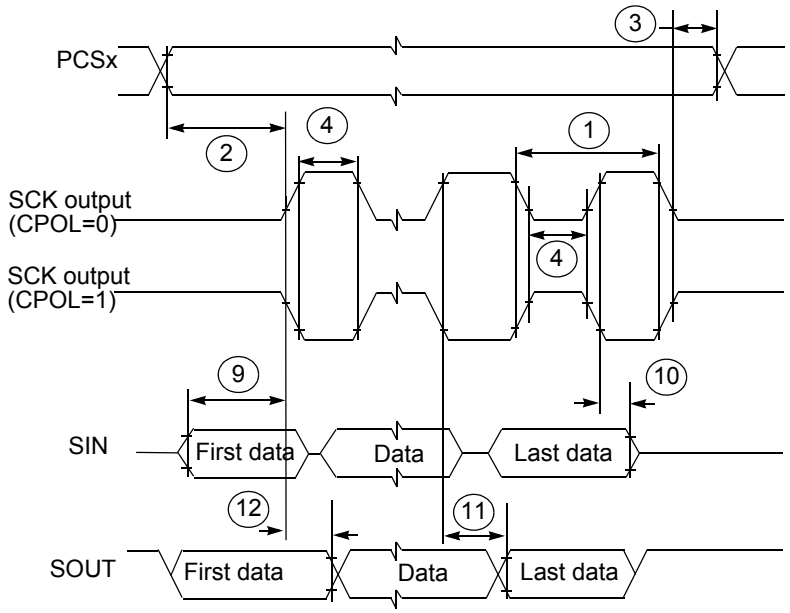

Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 0

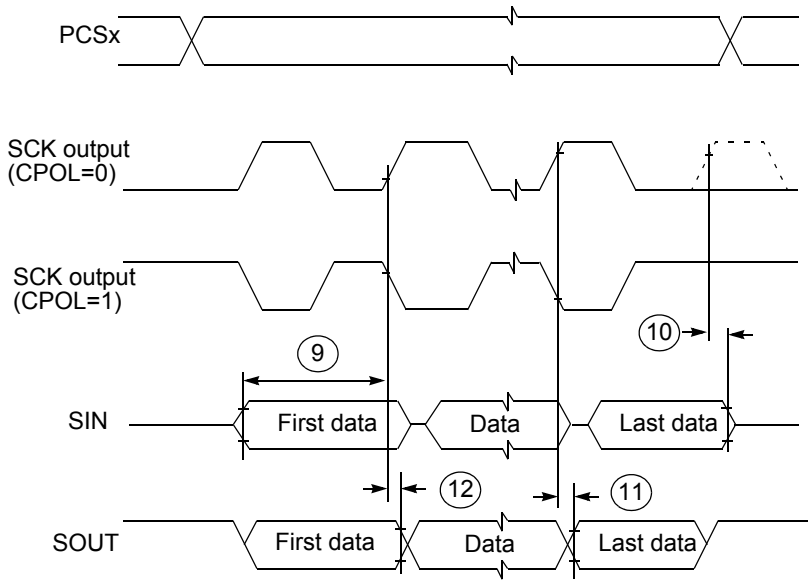

Figure 23. DSPI Modified Transfer Format Timing—Master, CPHA = 1

3.14.2 MII FEC Transmit Signal Timing FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, FEC_TX_CLK

The transmitter functions correctly up to the FEC_TX_CLK maximum frequency of 25 MHz plus one percent. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

The transmit outputs (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER) can be programmed to transition from either the rising- or falling-edge of TX_CLK, and the timing is the same in either case. These options allow the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the device reference manual for details of this option and how to enable it.

Table 29 lists MII FEC transmit channel timings.

Table 29. MII FEC Transmit Signal Timing

Spec	Characteristic	Min.	Max	Unit
5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	25	ns
7	FEC_TX_CLK pulse-width high	35%	65%	FEC_TX_CLK period
8	FEC_TX_CLK pulse-width low	35%	65%	FEC_TX_CLK period

Figure 29 shows MII FEC transmit signal timings listed in Table 29.

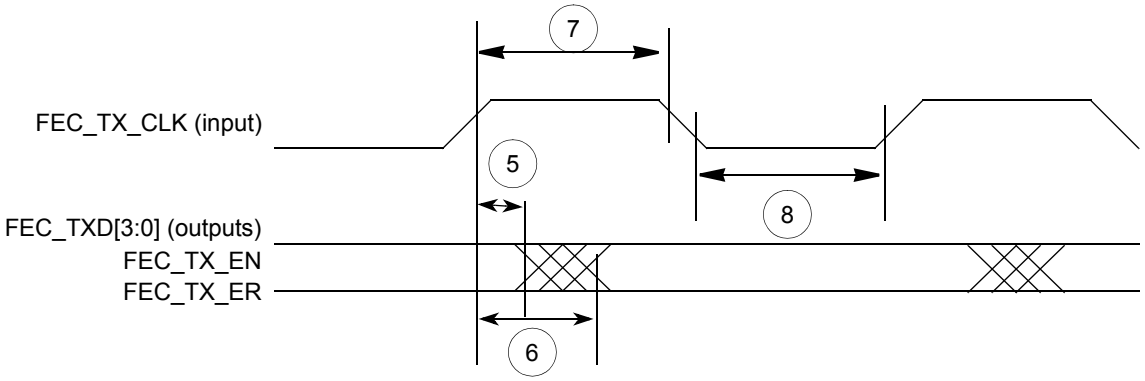

Figure 29. MII FEC Transmit Signal Timing Diagram

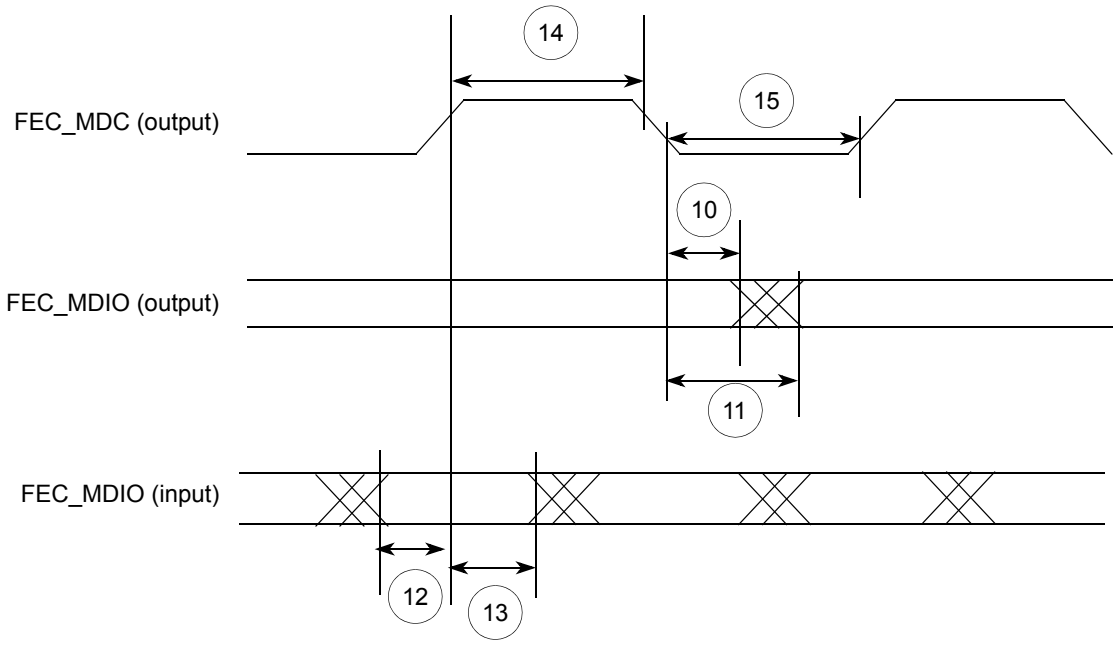

Figure 31. MII FEC Serial Management Channel Timing Diagram

4 Mechanicals

4.1 MPC5566 416 PBGA Pinout

Figure 32, Figure 33, and Figure 34 show the pinout for the MPC5566 416 PBGA package. The alternate Fast Ethernet Controller (FEC) signals are multiplexed with the data calibration bus signals.

NOTE

The MPC5500 devices are pin compatible for software portability and use the primary function names to label the pins in the BGA diagram. Although some devices do not support all the primary functions shown in the BGA diagram, the muxed and GPIO signals on those pins remain available. See the signals chapter in the device reference manual for the signal muxing.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VSTBY	AN37	AN11	VDDA1	AN16	AN1	AN5	VRH	AN23	AN27	AN28	AN35	VSSA0	AN15	ETRIG 1	ETPUB 18	ETPUB 20	ETPUB 24	ETPUB 27	GPIO 205	MDO11	MDO8	VDD	VDD33	VSS	A
B	VDD	VSS	AN36	AN39	AN19	AN20	AN0	AN4	REF BYPC	AN22	AN26	AN31	AN32	VSSA0	AN14	ETRIG 0	ETPUB 21	ETPUB 25	ETPUB 28	ETPUB 31	MDO10	MDO7	MDO4	MDO0	VSS	VDDE7	B
C	VDD33	VDD	VSS	AN8	AN17	VSSA1	AN21	AN3	AN7	VRL	AN25	AN30	AN33	VDDA0	AN13	ETPUB 19	ETPUB 22	ETPUB 26	ETPUB 30	MDO9	MDO6	MDO3	MDO1	VSS	VDDE7	VDD	C
D	ETPUA 30	ETPUA 31	VDD	VSS	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34	VDDEH 9	AN12	ETPUB 16	ETPUB 17	ETPUB 23	ETPUB 29	MDO5	MDO2	VDDEH 8	VSS	VDDE7	TCK	TDI	D
E	ETPUA 28	ETPUA 29	VDDEH 1	VDD																			VDDE7	TMS	TDO	TEST	E
F	ETPUA 24	ETPUA 27	ETPUA 26	VDDEH 1																			MSEO0	JCOMP	EVTI	EVTO	F
G	ETPUA 23	ETPUA 22	ETPUA 25	ETPUA 21																			MSEO1	MCKO	GPIO 204	ETPUB 15	G
H	ETPUA 20	ETPUA 19	ETPUA 18	ETPUA 17																			RDY	GPIO 203	ETPUB 14	ETPUB 13	H
J	ETPUA 16	ETPUA 15	ETPUA 14	ETPUA 13																			VDDEH 6	ETPUB 12	ETPUB 11	ETPUB 9	J
K	ETPUA 12	ETPUA 11	ETPUA 10	ETPUA 9						VSS	VSS	VSS	VSS	VDDE7	VDDE7	VDDE7	VDDE7						ETPUB 10	ETPUB 8	ETPUB 7	ETPUB 5	K
L	ETPUA 8	ETPUA 7	ETPUA 6	ETPUA 5						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDE7						ETPUB 6	ETPUB 4	ETPUB 3	ETPUB 2	L
M	ETPUA 4	ETPUA 3	ETPUA 2	ETPUA 1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VDDE7						TCRCLK B	ETPUB 1	ETPUB 0	SINB	M
N	BDIP	TEA	ETPUA 0	TCRCLK A						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VDDE7						SOUTB	PCSB3	PCSB0	PCSB1	N
P	CS3	CS2	CS1	CS0						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						PCSA3	PCSB4	SCKB	PCSB2	P
R	WE3	WE2	WE1	WE0						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						PCSB5	SOUTA	SINA	SCKA	R
T	VDDE2	TSIZ0	RD_WR	VDDE2						VDDE2	VSS	VDDE2	VDDE2	VDDE2	VDDE2	VSS	VSS						PCSA1	PCSA0	PCSA2	VPP	T
U	ADDR 16	TSIZ1	TA	VDD33						VSS	VDDE2	VDDE2	VDDE2	VDDE2	VDDE2	VSS	VSS						PCSA4	TXDA	PCSA5	VFLASH	U
V	ADDR 18	ADDR 17	TS	ADDR 8																			CNTXC	RXDA	RSTOUT	RST CFG	V
W	ADDR 20	ADDR 19	ADDR 9	ADDR 10																			RXDB	CNRXC	TXDB	RESET	W
Y	ADDR 22	ADDR 21	ADDR 11	VDDE2						Note:	NC	No connect. AC22 & AD23 reserved											WKP CFG	BOOT CFG1	VRC VSS	VSS SYN	Y
AA	ADDR 24	ADDR 23	ADDR 13	ADDR 12																			VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL	AA
AB	VDDE2	ADDR 25	ADDR 15	ADDR 14																			VDD	VRC CTL	PLL CFG0	XTAL	AB
AC	ADDR 26	ADDR 27	ADDR 31	VSS	VDD	DATA 26	DATA 28	VDDE2	DATA 30	DATA 31	DATA 8	DATA 10	VDDE2	DATA 12	DATA 14	EMIOS 2	EMIOS 8	EMIOS 12	EMIOS 21	VDDEH 4	VDDE5	NC	VSS	VDD	VRC33	VDD SYN	AC
AD	ADDR 28	ADDR 30	VSS	VDD	DATA 24	DATA 25	DATA 27	DATA 29	VDD33	GPIO 207	DATA 9	DATA 11	DATA 13	DATA 15	EMIOS 3	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC	VSS	VDD	VDD33	AD
AE	ADDR 29	VSS	VDD	DATA 17	DATA 19	DATA 21	DATA 23	DATA 0	DATA 2	DATA 4	DATA 6	OE	BR	BG	EMIOS 1	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD	AE
AF	VSS	VDD	DATA 16	DATA 18	VDDE2	DATA 20	DATA 22	GPIO 206	DATA 1	DATA 3	VDDE2	DATA 5	DATA 7	BB	EMIOS 0	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 32. MPC5566 416 Package

Table 34. Global and Text Changes Between Rev. 0.0 and 1.0 (continued)

Location	Description of Changes
Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33:"	Added the following text directly before this section and after Table 8 *Pin Status for Medium / Slow Pads During the Power-on Sequence*: 'The values in Table 7 and Table 8 do not include the effect of the weak pull devices on the output pins during power up. Before exiting the internal POR state, the voltage on the pins goes to high-impedance until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak pull devices (up or down) are enabled as defined in the device *Reference Manual*. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}. To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.'
Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)"	Deleted the underscore in ORed_POR to become ORed POR.

The following table lists the information that changed in the figures or tables between Rev. 0.0 and 1.0.

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0

Location	Description of Changes
Figure 1, MPC5500 Family Part Numbers:	• Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text. • Changed Qualification Status by adding ', general market flow' to the M designator, and added an 'S' designator with the description of 'Fully spec. qualified, automotive flow.

Table 1, Orderable Part Numbers:	• Added a 144 MHz system frequency option for:
	  • MPC5566MVR144, Pb-Free (lead free), nominal 144, maximum 147
	  • MPC5566MZP144, SnPb (leaded), nominal 144, maximum 147
	• Changed the 132 MHz maximum operating frequency to 135 MHz.
	• Reordered rows to group devices by lead-free package types in descending frequency order, and leaded package types.
	• Footnote 1 added that reads: All devices are PPC5566, rather than MPC5566 or SPC5566, until product qualifications are complete. Not all configurations are available in the PPC parts.
	• Footnote 2 added that reads: The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.
	• Changed footnote 3 from '132 MHz allows only 128 MHz + 2% FM' to '135 MHz parts allow for 132 MHz systems clock + 2% FM'; and added '147 MHz parts allow for 144 MHz systems clock + 2% FM.

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 22, Bus Operation Timing:	• Added a column to the table for 72 MHz minimum and maximum bus frequencies. • Spec 1: 72 MHz Min. column = 13.3. • Specs 5 and 6: *CLKOUT positive edge to output signals invalid of high*: Corrected format to show the bus timing values for various frequencies with EBTS bit = 0 and EBTS bit = 1. • Specs 5, and 6: Added the $\overline{BB}$ signal for arbitration. Added the following calibration signals: CAL_ADDR[9:30], CAL_$\overline{CS}$[0:3], CAL_DATA[0:15], CAL_$\overline{OE}$, CAL_RD_$\overline{WR}$, CAL_$\overline{TS}$, CAL_$\overline{WE}$/$\overline{BE}$[0:1]. • Spec 5: EBI and Calibration sections, 72 MHz Min column, EBTS = 0 is 1.0, EBTS = 1 is 1.5. • Spec 6: EBI section, 72 MHz Max column, EBTS = 0 is 5.0, EBTS = 1 is 6.0. • Spec 6a: Calibration section, 72 MHz Max column, EBTS = 0 is 6.0, EBTS = 1 is 7.0 • Specs 7 and 8: Added the $\overline{BB}$ signal for arbitration. Added the following calibration signals: CAL_ADDR[9:30], CAL_DATA[0:15], CAL_RD_$\overline{WR}$, CAL_$\overline{TS}$.
Table 23, External Interrupt Timing:	• Footnote 1: Deleted '. . F_{SYS} = 132 MHz', 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and ' .and CL = 200 pF with SRC = 0b11.' • Deleted second figure after table 'External Interrupt Setup Timing.'
Table 24, eTPU Timing	• Footnote 1: Deleted '. . .F_{SYS} = 132 MHz', 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and 'and CL = 200 pF with SRC = 0b11.' • Deleted second figure, '*eTPU Input/Output Timing*' after this table. • Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).'
Table 25, eMIOS Timing:	• Deleted (MTS) from the heading, table, and footnotes. • Footnote 1: Deleted '. . .F_{SYS} = 132 MHz, 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and 'and CL = 200 pF with SRC = 0b11.' • Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).'
Figure 17, eMIOS Timing: Added figure.	
Table 26, DSPI Timing:	• Added 144 MHz column to the table. • Spec1:*SCK Cycle Time*: changes to values: 80 MHz, min. = 24.4; 112 MHz, min. = 17.5, max = 2.1; 132 MHz, min. = 14.8, max = 1.8; 144 MHz, min. = 13.6, max = 1.6. • Spec1:*SCK Cycle Time*: Added footnote 4 to the 144 MHz min. and max values that reads: Preliminary. Specification pending final characterization • Spec 2, *PCS to SCK delay*, 144 MHz, min. TBD • Spec 3, *After SCK delay*, 144 MHz, min. TBD • Spec 9, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. TBD • Spec 10, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. TBD • Spec 11, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, max TBD • Spec 12, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. TBD • Added to beginning of footnote 1 'All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate.' • Footnote 1: Deleted 'V_{DD} = 1.35–1.65 V' and 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V.

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