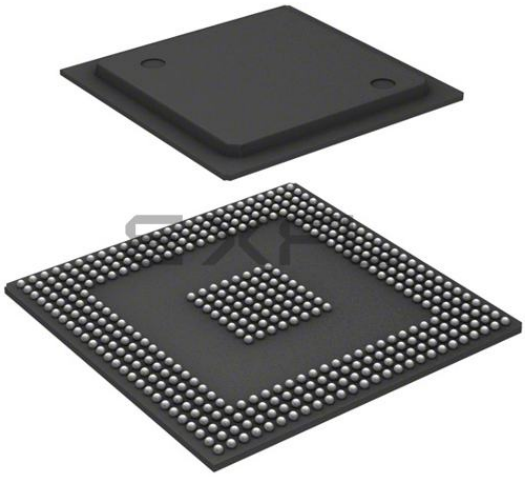

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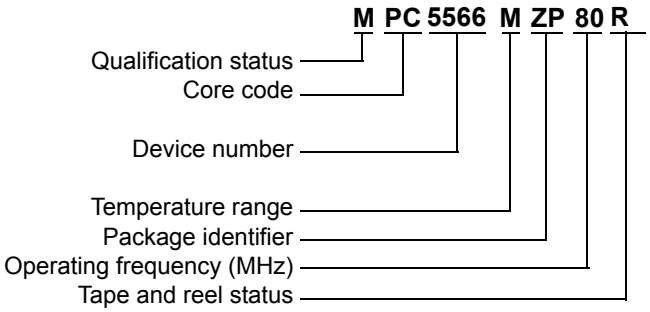
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5566mzp144r

2 Ordering Information



Temperature Range
M = –40° C to 125° C

Package Identifier
ZP = 416PBGA SnPb
VR = 416PBGA Pb-free

Operating Frequency
80 = 80 MHz
112 = 112 MHz
132 = 132 MHz
144 = 144 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to Table 1.

Figure 1. MPC5500 Family Part Number Example

Unless noted in this data sheet, all specifications apply from T_L to T_H.

Table 1. Orderable Part Numbers

Freescale Part Number[1]	Package Description	Speed (MHz)		Operating Temperature [2]	
		Nominal	Max. [3] (f_{MAX})	Min. (T_L)	Max. (T_H)
MPC5566MVR144	MPC5566 416 package Lead-free (PbFree)	144	147	–40° C	125° C
MPC5566MVR132		132	135		
MPC5566MVR112		112	114		
MPC5566MVR80		80	82		
MPC5566MZP144	MPC5566 416 package Leaded (SnPb)	144	147	–40° C	125° C
MPC5566MZP132		132	135		
MPC5566MZP112		112	114		
MPC5566MZP80		80	82		

1 All devices are PPC5566, rather than MPC5566 or SPC5566, until product qualifications are complete. Not all configurations are available in the PPC parts.

2 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

3 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; 135 MHz parts allow for 132 MHz system clock + 2% FM; and 147 MHz parts allow for 144 MHz system clock + 2% FM.

3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Rd.
San Jose, CA., 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.3 Package

The MPC5566 is available in packaged form. Read the package options in Section 2, “Ordering Information.” Refer to Section 4, “Mechanicals,” for pinouts and package drawings.

3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications [1]

Spec	Characteristic	Minimum	Typical	Maximum	Unit
1	Scan range	0.15	—	1000	MHz
2	Operating frequency	—	—	f_{MAX}	MHz
3	V_{DD} operating voltages	—	1.5	—	V
4	V_{DDSYN}, V_{RC33}, V_{DD33}, V_{FLASH}, V_{DDE} operating voltages	—	3.3	—	V
5	V_{PP}, V_{DDEH}, V_{DDA} operating voltages	—	5.0	—	V
6	Maximum amplitude	—	—	14 [2] 32 [3]	dBuV
7	Operating temperature	—	—	25	°C

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

2 Measured with the single-chip EMI program.

3 Measured with the expanded EMI program.

3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings [1, 2]

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	Ω
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins) 750 (corner pins)	V
Number of pulses per pin: Positive pulses (HBM) Negative pulses (HBM)	 — —	 1 1	 — —
Interval of pulses	—	1	second

1 All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

3.6 Voltage Regulator Controller (V_{RC}) and Power-On Reset (POR) Electrical Specifications

The following table lists the V_{RC} and POR electrical specifications:

Table 6. V_{RC} and POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V (V_{DD}) POR [1]	Negated (ramp up) Asserted (ramp down)	V_{POR15}	1.1 1.1	1.35 1.35	V
2	3.3 V (V_{DDSYN}) POR [1]	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	V_{POR33}	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	$\overline{\text{RESET}}$ pin supply (V_{DDEH6}) POR [1, 2]	Negated (ramp up) Asserted (ramp down)	V_{POR5}	2.0 2.0	2.85 2.85	V
4	V_{RC33} voltage	Before V_{RC} allows the pass transistor to start turning on	V_{TRANS_START}	1.0	2.0	V
5		When V_{RC} allows the pass transistor to completely turn on [3, 4]	V_{TRANS_ON}	2.0	2.85	V
6		When the voltage is greater than the voltage at which the V_{RC} keeps the 1.5 V supply in regulation [5, 6]	$V_{VRC33REG}$	3.0	—	V
7	Current can be sourced by V_{RCCTL} at Tj:	–40° C 25° C 150° C	I_{VRCCTL} [7]	11.0 9.0 7.5	— — —	mA mA mA
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V

1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

3.7.1 Input Value of Pins During POR Dependent on V_{DD33}

When powering up the device, V_{DD33} must not lag the latest V_{DDSYN} *or* $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} *or* the $\overline{\text{RESET}}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification applies during power up only. V_{DD33} has no lead or lag requirements when powering down.

3.7.2 Power-Up Sequence (V_{RC33} Grounded)

The 1.5 V V_{DD} power supply must rise to 1.35 V before the 3.3 V V_{DDSYN} power supply and the $\overline{\text{RESET}}$ power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, V_{DD} must be within specification before the 3.3 V POR and the $\overline{\text{RESET}}$ POR negate.

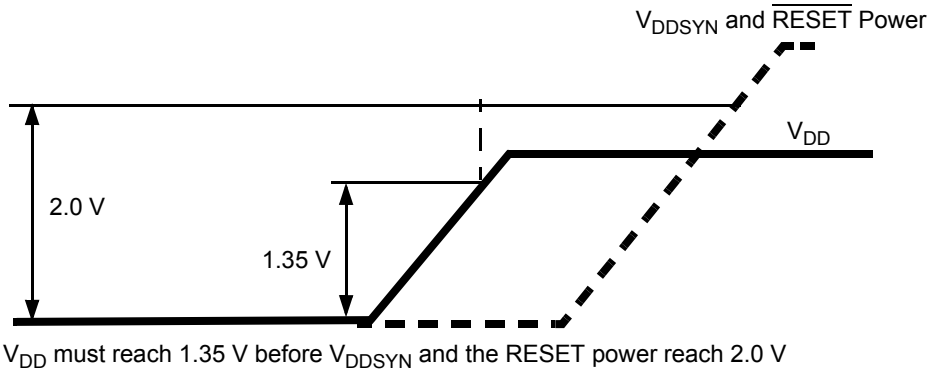


Figure 3. Power-Up Sequence (V_{RC33} Grounded)

3.7.3 Power-Down Sequence (V_{RC33} Grounded)

The only requirement for the power-down sequence with V_{RC33} grounded is if V_{DD} decreases to less than its operating range, V_{DDSYN} or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the V_{DD} power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly. See Table 6, footnote 1.

3.8 DC Electrical Specifications

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min	Max.	Unit
1	Core supply voltage (average DC RMS voltage)	V_{DD}	1.35	1.65	V
2	Input/output supply voltage (fast input/output) [1]	V_{DDE}	1.62	3.6	V
3	Input/output supply voltage (slow and medium input/output)	V_{DDEH}	3.0	5.25	V
4	3.3 V input/output buffer voltage	V_{DD33}	3.0	3.6	V
5	Voltage regulator control input voltage	V_{RC33}	3.0	3.6	V
6	Analog supply voltage [2]	V_{DDA}	4.5	5.25	V
8	Flash programming voltage [3]	V_{PP}	4.5	5.25	V
9	Flash read voltage	V_{FLASH}	3.0	3.6	V
10	SRAM standby voltage [4]	V_{STBY}	0.8	1.2	V
11	Clock synthesizer operating voltage	V_{DDSYN}	3.0	3.6	V
12	Fast I/O input high voltage	V_{IH_F}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
13	Fast I/O input low voltage	V_{IL_F}	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
14	Medium and slow I/O input high voltage	V_{IH_S}	$0.65 \times V_{DDEH}$	$V_{DDEH} + 0.3$	V
15	Medium and slow I/O input low voltage	V_{IL_S}	$V_{SS} - 0.3$	$0.35 \times V_{DDEH}$	V
16	Fast input hysteresis	V_{HYS_F}	$0.1 \times V_{DDE}$		V
17	Medium and slow I/O input hysteresis	V_{HYS_S}	$0.1 \times V_{DDEH}$		V
18	Analog input voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$	V
19	Fast output high voltage (I_{OH_F} = –2.0 mA)	V_{OH_F}	$0.8 \times V_{DDE}$	—	V
20	Slow and medium output high voltage I_{OH_S} = –2.0 mA I_{OH_S} = –1.0 mA	V_{OH_S}	$0.80 \times V_{DDEH}$ $0.85 \times V_{DDEH}$	—	V
21	Fast output low voltage (I_{OL_F} = 2.0 mA)	V_{OL_F}	—	$0.2 \times V_{DDE}$	V
22	Slow and medium output low voltage I_{OL_S} = 2.0 mA I_{OL_S} = 1.0 mA	V_{OL_S}	—	 $0.20 \times V_{DDEH}$ $0.15 \times V_{DDEH}$	V
23	Load capacitance (fast I/O) [5] DSC (SIU_PCR[8:9]) = 0b00 = 0b01 = 0b10 = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
24	Input capacitance (digital pins)	C_{IN}	—	7	pF
25	Input capacitance (analog pins)	C_{IN_A}	—	10	pF
26	Input capacitance: (Shared digital and analog pins AN[12]_MA[0]_$\overline{SDS}$, AN[13]_MA[1]_SDO, AN[14]_MA[2]_SDI, and AN[15]_FCK)	C_{IN_M}	—	12	pF

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} [13]	I_{DD_33}	—	2 + (values derived from procedure of footnote [13])	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} (V_{DDA0} + V_{DDA1})	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH}, V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA
30	Operating current V_{DDE} supplies: [14]				
	V_{DDEH1}	I_{DD1}	—	Refer to footnote [14]	mA
	V_{DDE2}	I_{DD2}	—		mA
	V_{DDE3}	I_{DD3}	—		mA
	V_{DDEH4}	I_{DD4}	—		mA
	V_{DDE5}	I_{DD5}	—		mA
	V_{DDEH6}	I_{DD6}	—		mA
	V_{DDE7}	I_{DD7}	—		mA
	V_{DDEH8}	I_{DD8}	—		mA
	V_{DDEH9}	I_{DD9}	—		mA
31	Fast I/O weak pullup current [15]	I_{ACT_F}			
	1.62–1.98 V		10	110	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
	Fast I/O weak pulldown current [15]				
	1.62–1.98 V		10	100	µA
	2.25–2.75 V		20	130	µA
	3.00–3.60 V		20	170	µA
32	Slow and medium I/O weak pullup/down current [15]	I_{ACT_S}			
	3.0–3.6 V		10	150	µA
	4.5–5.5 V		20	170	µA
33	I/O input leakage current [16]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [17]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [18]	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	V_{SSA} – 0.1	V_{SSA} + 0.1	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	V_{DDA} – 0.1	V_{DDA} + 0.1	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

Table 18. Derated Pad AC Specifications (V_{DDEH} = 3.3 V, V_{DDE} = 3.3 V) [1] (continued)

Spec	Pad	SRC/DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [3, 5] (ns)	Load Drive (pF)
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9500	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 3.0–3.6 V; V_{DDEH} = 3.0–3.6 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and guaranteed by design (not tested).

3 The output delay, and the rise and fall, are calculated to 20% or 80% of the respective signal.

4 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

5 This parameter is guaranteed by characterization rather than 100% tested.

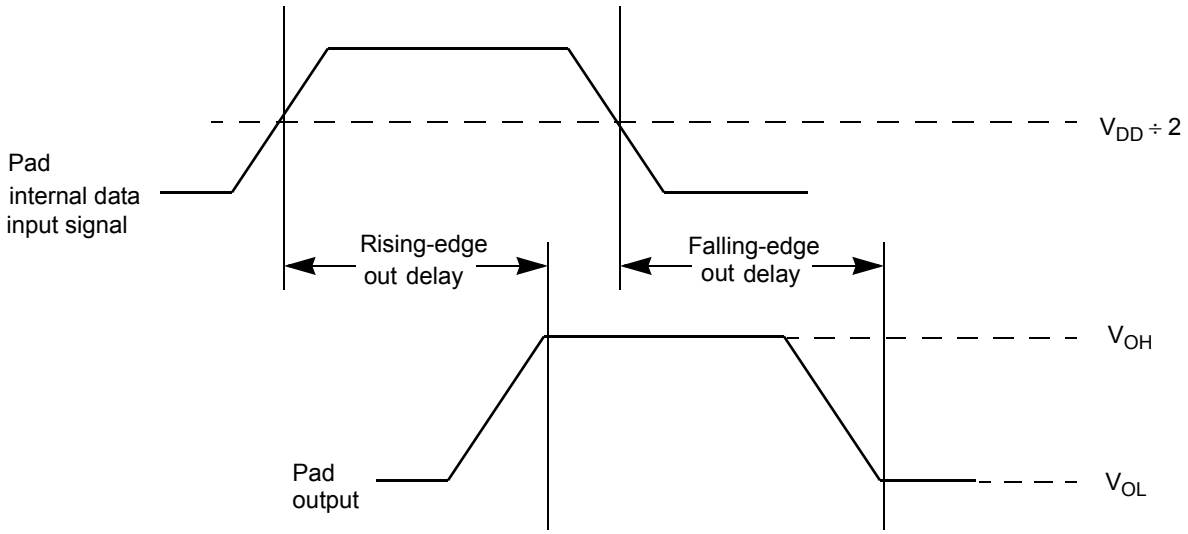


Figure 4. Pad Output Delay

3.13 AC Timing

3.13.1 Reset and Configuration Pin Timing

Table 19. Reset and Configuration Pin Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	$\overline{\text{RESET}}$ pulse width	t_{RPW}	10	—	t_{CYC}
2	$\overline{\text{RESET}}$ glitch detect pulse width	t_{GPW}	2	—	t_{CYC}

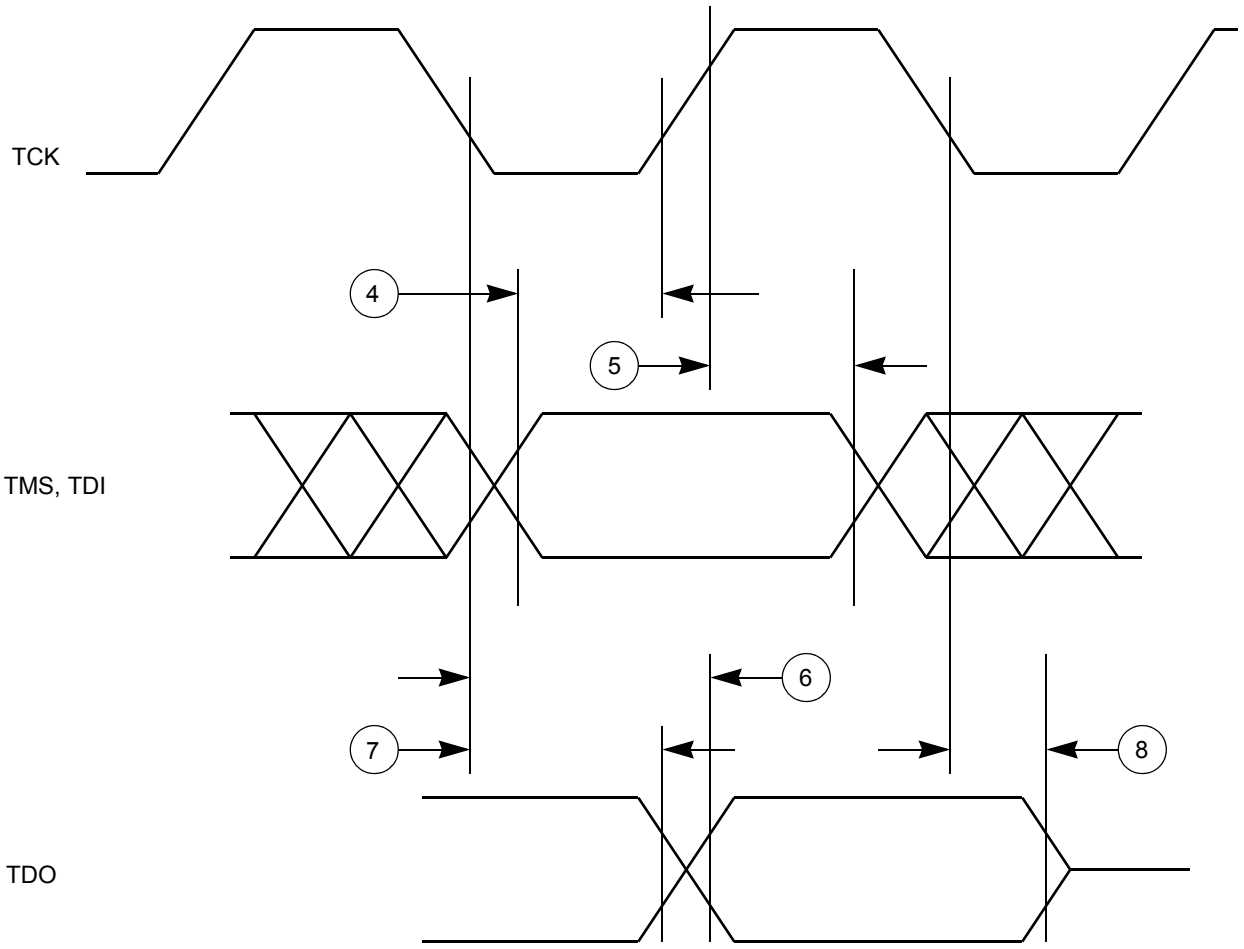


Figure 7. JTAG Test Access Port Timing

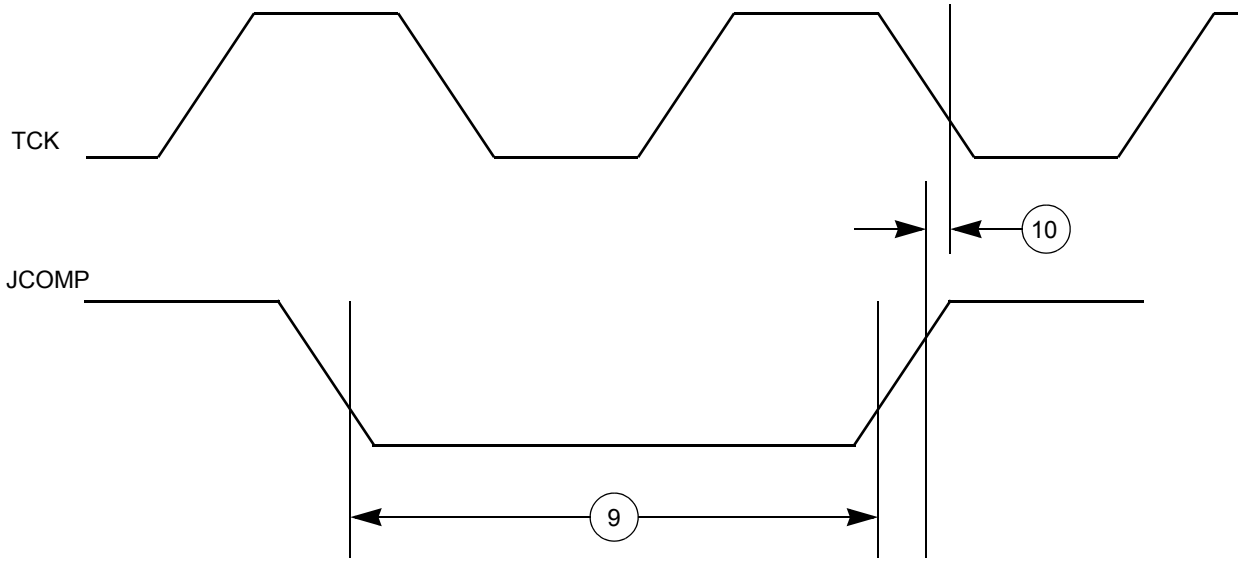


Figure 8. JTAG JCOMP Timing

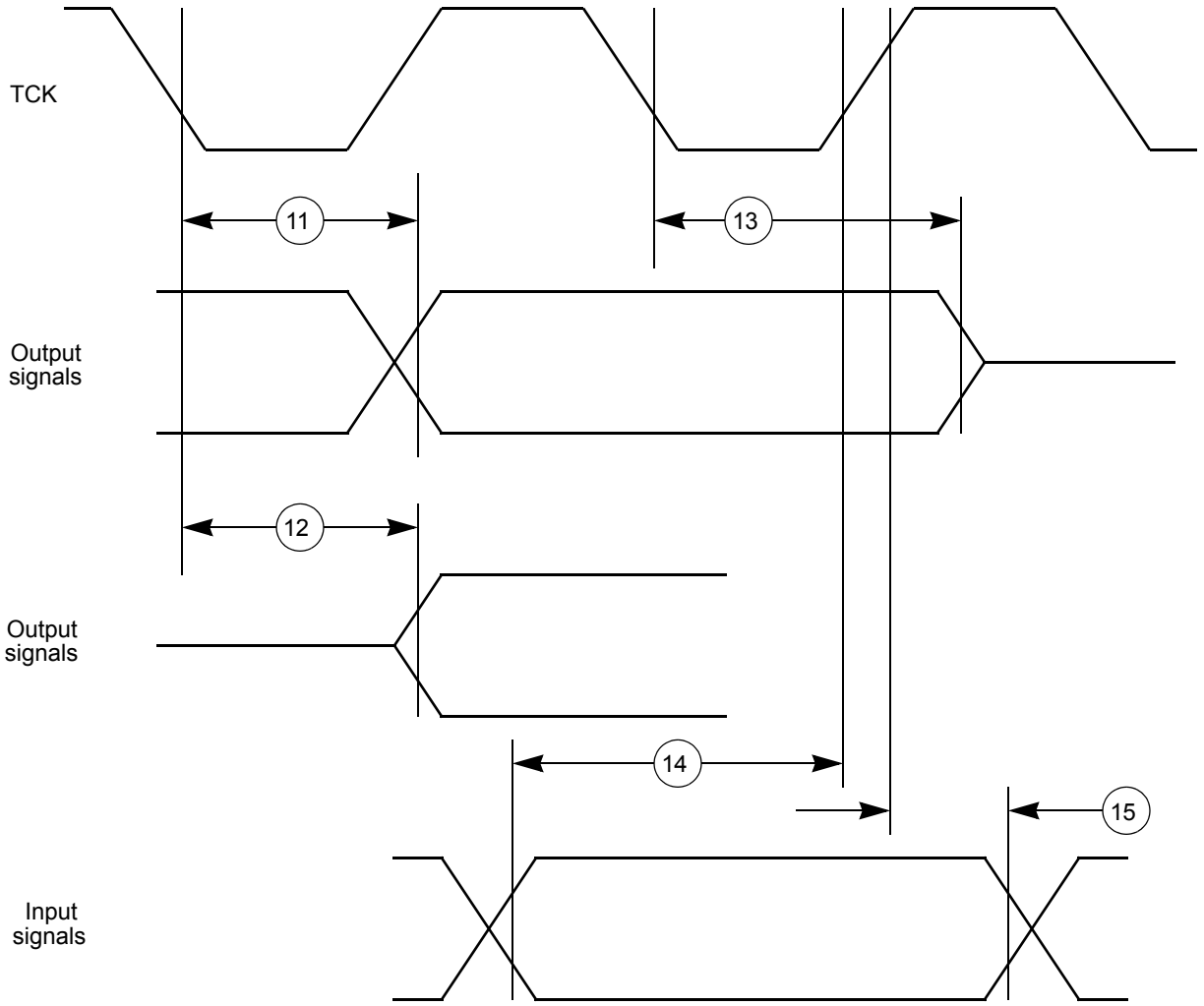


Figure 9. JTAG Boundary Scan Timing

3.13.3 Nexus Timing

Table 21. Nexus Debug Port Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	MCKO cycle time	t_{MCYC}	1 [2]	8	t_{CYC}
2	MCKO duty cycle	t_{MDC}	40	60	%
3	MCKO low to MDO data valid [3]	t_{MDOV}	–1.5	3.0	ns
4	MCKO low to $\overline{\text{MSEO}}$ data valid [3]	t_{MSEOV}	–1.5	3.0	ns
5	MCKO low to $\overline{\text{EVTO}}$ data valid [3]	t_{EVTOV}	–1.5	3.0	ns
6	$\overline{\text{EVTI}}$ pulse width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ pulse width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK cycle time	t_{TCYC}	4 [4]	—	t_{CYC}
9	TCK duty cycle	t_{TDC}	40	60	%
10	TDI, TMS data setup time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS data hold time	t_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK low to TDO data valid V_{DDE} = 2.25–3.0 V V_{DDE} = 3.0–3.6 V	t_{JOV}	 0 0	 12 10	 ns ns
13	$\overline{\text{RDY}}$ valid to MCKO [5]	—	—	—	—

1 JTAG specifications apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.35–1.65 V, V_{DDE} = 2.25–3.6 V, V_{DD33} and V_{DDSYN} = 3.0–3.6 V, T_A = T_L to T_H, and CL = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 82 MHz.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until the next MCKO low cycle occurs.

4 Limit the maximum frequency to approximately 16 MHz (V_{DDE} = 2.25–3.0 V) or 20 MHz (V_{DDE} = 3.0–3.6 V) to meet the timing specification for t_{JOV} of [0.2 x t_{JCYC}] as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO and is guaranteed by design to function correctly.

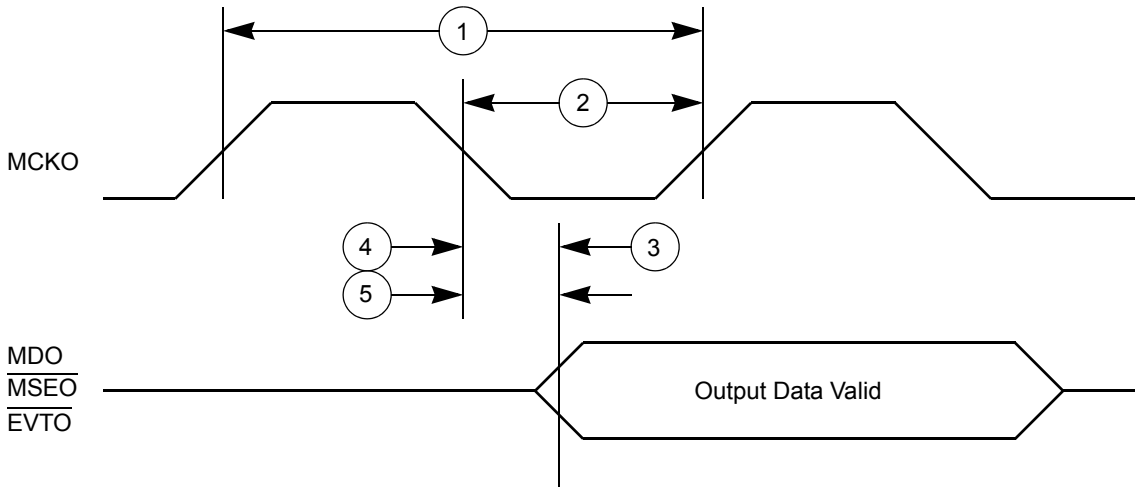


Figure 10. Nexus Output Timing

3.13.4 External Bus Interface (EBI) Timing

Table 22 lists the timing information for the external bus interface (EBI).

Table 22. Bus Operation Timing [1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]								Unit	Notes
			40 MHz		56 MHz		67 MHz		72 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
1	CLKOUT period	T_C	25.0	—	17.9	—	15.2	—	13.3	—	ns	Signals are measured at 50% V_{DDE}.
2	CLKOUT duty cycle	t_{CDC}	45%	55%	45%	55%	45%	55%	45%	55%	T_C	
3	CLKOUT rise time	t_{CRT}	—	— [4]	—	— [4]	—	— [4]	—	— [4]	ns	
4	CLKOUT fall time	t_{CFT}	—	— [4]	—	— [4]	—	— [4]	—	— [4]	ns	
5	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) External bus interface CS[0:3] ADDR[8:31] DATA[0:31] BDIP BG [5] BR [7] BB OE RD_WR TA TEA TS TSIZ[0:1] WE/BE[0:3]	t_{COH}	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.
	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) Calibration bus interface CAL_CS[0:3] CAL_ADDR[9:30] CAL_DATA[0:15] CAL_OE CAL_RD_WR CAL_TS CAL_WE/BE[0:1]	t_{CCOH}	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.

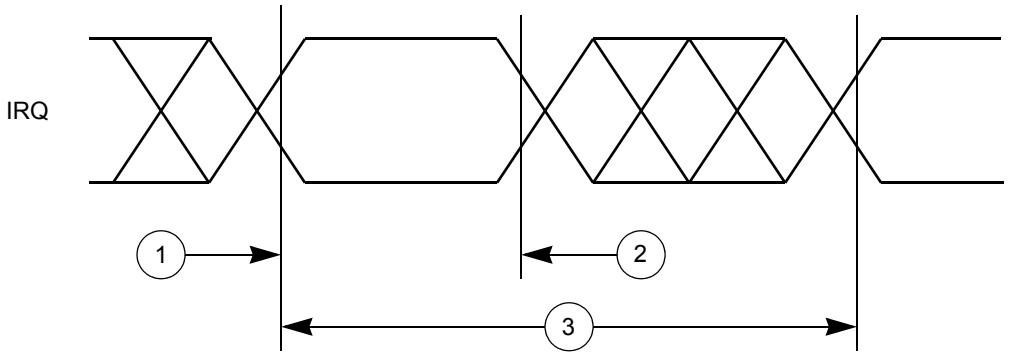


Figure 15. External Interrupt Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing [1]

Spec	Characteristic	Symbol	Min.	Max	Unit
1	eTPU input channel pulse width	t_{ICPW}	4	—	t_{CYC}
2	eTPU output channel pulse width	t_{OCPW}	2 [2]	—	t_{CYC}

1 eTPU timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

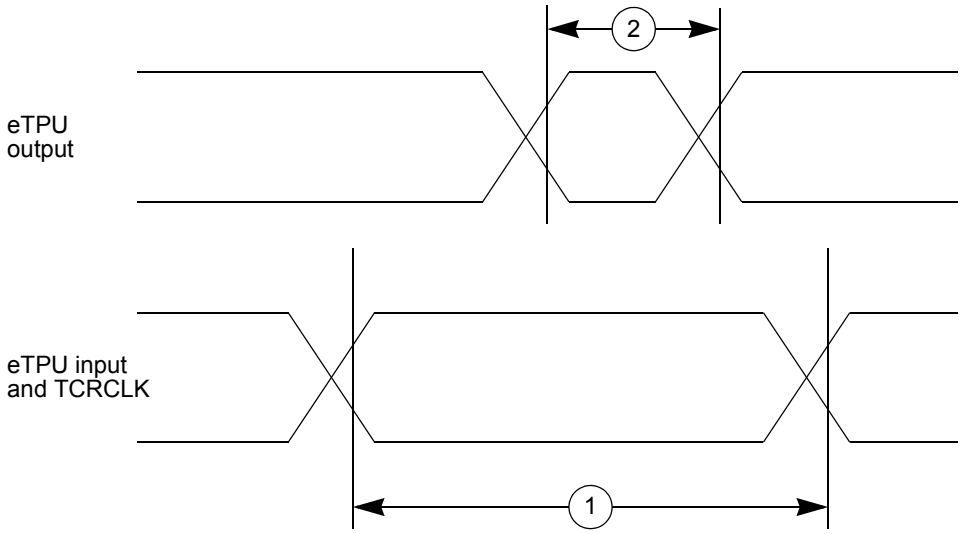
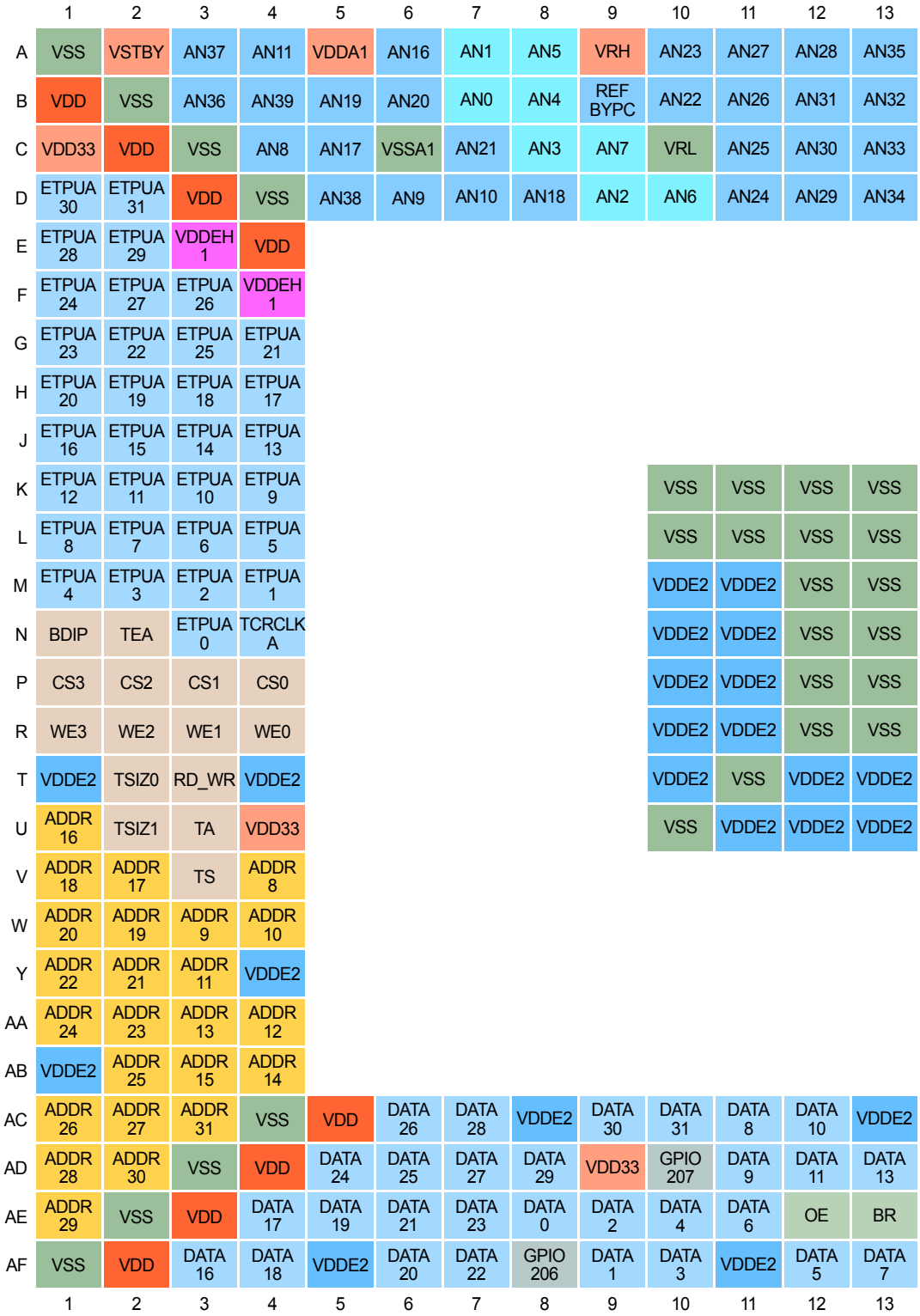


Figure 16. eTPU Timing



	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	VSTBY	AN37	AN11	VDDA1	AN16	AN1	AN5	VRH	AN23	AN27	AN28	AN35
B	VDD	VSS	AN36	AN39	AN19	AN20	AN0	AN4	REF BYPC	AN22	AN26	AN31	AN32
C	VDD33	VDD	VSS	AN8	AN17	VSSA1	AN21	AN3	AN7	VRL	AN25	AN30	AN33
D	ETPUA 30	ETPUA 31	VDD	VSS	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34
E	ETPUA 28	ETPUA 29	VDDEH 1	VDD									
F	ETPUA 24	ETPUA 27	ETPUA 26	VDDEH 1									
G	ETPUA 23	ETPUA 22	ETPUA 25	ETPUA 21									
H	ETPUA 20	ETPUA 19	ETPUA 18	ETPUA 17									
J	ETPUA 16	ETPUA 15	ETPUA 14	ETPUA 13									
K	ETPUA 12	ETPUA 11	ETPUA 10	ETPUA 9						VSS	VSS	VSS	VSS
L	ETPUA 8	ETPUA 7	ETPUA 6	ETPUA 5						VSS	VSS	VSS	VSS
M	ETPUA 4	ETPUA 3	ETPUA 2	ETPUA 1						VDDE2	VDDE2	VSS	VSS
N	BDIP	TEA	ETPUA 0	TCRCLK A						VDDE2	VDDE2	VSS	VSS
P	CS3	CS2	CS1	CS0						VDDE2	VDDE2	VSS	VSS
R	WE3	WE2	WE1	WE0						VDDE2	VDDE2	VSS	VSS
T	VDDE2	TSIZ0	RD_WR	VDDE2						VDDE2	VSS	VDDE2	VDDE2
U	ADDR 16	TSIZ1	TA	VDD33						VSS	VDDE2	VDDE2	VDDE2
V	ADDR 18	ADDR 17	TS	ADDR 8									
W	ADDR 20	ADDR 19	ADDR 9	ADDR 10									
Y	ADDR 22	ADDR 21	ADDR 11	VDDE2									
AA	ADDR 24	ADDR 23	ADDR 13	ADDR 12									
AB	VDDE2	ADDR 25	ADDR 15	ADDR 14									
AC	ADDR 26	ADDR 27	ADDR 31	VSS	VDD	DATA 26	DATA 28	VDDE2	DATA 30	DATA 31	DATA 8	DATA 10	VDDE2
AD	ADDR 28	ADDR 30	VSS	VDD	DATA 24	DATA 25	DATA 27	DATA 29	VDD33	GPIO 207	DATA 9	DATA 11	DATA 13
AE	ADDR 29	VSS	VDD	DATA 17	DATA 19	DATA 21	DATA 23	DATA 0	DATA 2	DATA 4	DATA 6	OE	BR
AF	VSS	VDD	DATA 16	DATA 18	VDDE2	DATA 20	DATA 22	GPIO 206	DATA 1	DATA 3	VDDE2	DATA 5	DATA 7
	1	2	3	4	5	6	7	8	9	10	11	12	13

Figure 33. MPC5566 416 Package Left Side (view 1 of 2)

4.2 MPC5566 416-Pin Package Dimensions

The package drawings of the MPC5566 416 pin TEPBGA package are shown in Figure 36.

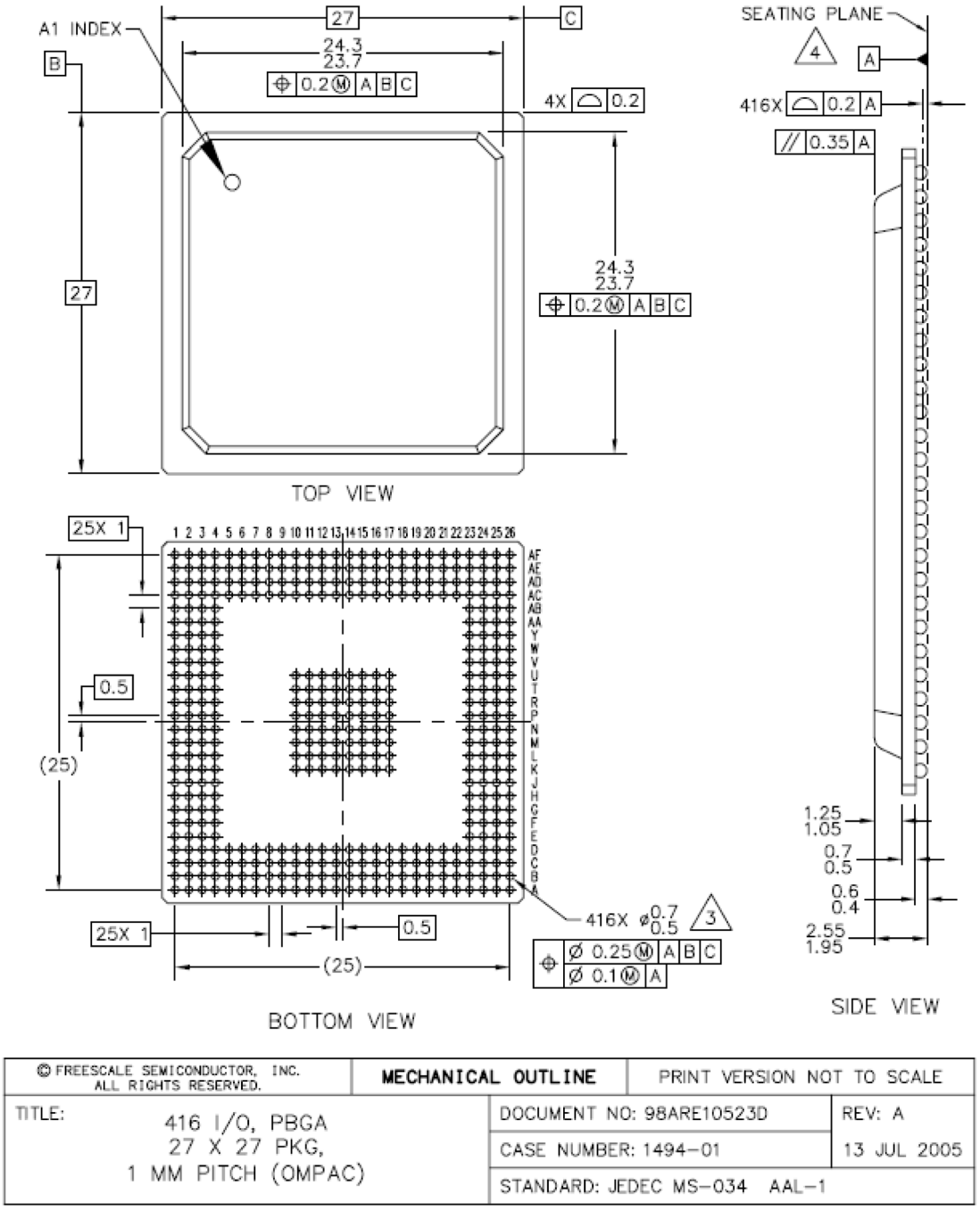


Figure 36. MPC5566 416 TEPBGA Package

Table 34. Global and Text Changes Between Rev. 0.0 and 1.0 (continued)

Location	Description of Changes
Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33:"	Added the following text directly before this section and after Table 8 *Pin Status for Medium / Slow Pads During the Power-on Sequence*: 'The values in Table 7 and Table 8 do not include the effect of the weak pull devices on the output pins during power up. Before exiting the internal POR state, the voltage on the pins goes to high-impedance until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak pull devices (up or down) are enabled as defined in the device *Reference Manual*. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}. To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.'
Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)"	Deleted the underscore in ORed_POR to become ORed POR.

The following table lists the information that changed in the figures or tables between Rev. 0.0 and 1.0.

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0

Location	Description of Changes
Figure 1, MPC5500 Family Part Numbers:	• Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text. • Changed Qualification Status by adding ', general market flow' to the M designator, and added an 'S' designator with the description of 'Fully spec. qualified, automotive flow.

Table 1, Orderable Part Numbers:	• Added a 144 MHz system frequency option for:
	  • MPC5566MVR144, Pb-Free (lead free), nominal 144, maximum 147
	  • MPC5566MZP144, SnPb (leaded), nominal 144, maximum 147
	• Changed the 132 MHz maximum operating frequency to 135 MHz.
	• Reordered rows to group devices by lead-free package types in descending frequency order, and leaded package types.
	• Footnote 1 added that reads: All devices are PPC5566, rather than MPC5566 or SPC5566, until product qualifications are complete. Not all configurations are available in the PPC parts.
	• Footnote 2 added that reads: The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.
	• Changed footnote 3 from '132 MHz allows only 128 MHz + 2% FM' to '135 MHz parts allow for 132 MHz systems clock + 2% FM'; and added '147 MHz parts allow for 144 MHz systems clock + 2% FM.

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 5, ESD Characteristics: Added (Electromagnetic Static Discharge) in the table title.	

Table 6, VCR/POR Electrical Specifications:	• Added footnote 1 to specs 1, 2, and 3 that reads: On power up, assert $\overline{\text{RESET}}$ before V_{POR15}, V_{POR33}, and V_{POR5} negate (internal POR). RESET must remain asserted until the power supplies are within the operating conditions as specified in Table 9 *DC Electrical Specifications*. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.
	• Subscript all symbol names that appear after the first underscore character.
	• Specs 7 and 10: added 'at Tj ' at the end of the first line in the second column: Characteristic.
	• Removed 'Tj ' after '150 C' in the last line, second column: Characteristic.
	• Spec 10, second column, second line:
	Added cross-reference to footnote 6: 'I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.' Changed '(@ V_{DD} = 1.35 V, $f_{sys} = f_{MAX}$)' to '(@ $f_{sys} = f_{MAX}$).'
	• Footnote 10: Deleted 'Preliminary value. Final specification pending characterization."
	• Added to Spec 2:
	3.3 V (V_{DDSYN}) POR negated (ramp down) Min 0.0 Max 0.30 V
	3.3 V (V_{DDSYN}) POR asserted (ramp up) Min 0.0 Max 0.30 V
	• Added new footnote 1 to both lines in Spec 3: " V_{IL_S} (Table 9, Spec 15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.
	• Spec 5: Changed old Footnote 1 (now footnote 2): 'User must be able to supply full operating current for the 1.5V supply when the 3.3V supply reaches this range." to 'Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range."
	• Spec 3: Added new footnote 3 for both lines: 'It is possible to reach the current limit during ramp up--do not treat this event as a short circuit current.'
	• Spec 10:
	  • Changed the minimum values of: -40 C = 60; 25 C = 65.
	  • Added old footnote 5 new footnote 6.
	  • Added a new footnote 7, 'Refer to Table 1 for the maximum operating frequency.'
	  • Rewrote old footnote 7(new footnote 9) to: Represents the worst-case external transistor BETA. It is measured on a per part basis and calculated as (I_{DD} ÷ I_{VRCCTL}).
	• Deleted old footnote 8: 'Preliminary value. Final specification pending characterization.'

Table 7, Power Sequence Pin Status for Fast Pads:	• Changed title to *Pin Status for Fast Pads During the Power Sequence* • Changed preceding paragraph From: Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies depending on power. Prior to exiting POR, the pads are in a high impedance state (Hi-Z). To: There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up/down varies depending on which supplies are powered. • Deleted the 'Comment' column. • Added a POR column after the V_{DD} column. • Added row 2:' V_{DDE}, Low, Low, Asserted, High' and row 5: V_{DDE}, V_{DD33}, V_{DD}, Asserted, Hi-Z.
Table 8, Power Sequence Pin Status for Medium/Slow Pads:	• Changed title to *Pin Status for Medium and Slow Pads During the Power Sequence* • Updated preceding paragraph. • Deleted the 'Comment' column. • Added a POR column after the V_{DD} column. • Added row 3:' V_{DDEH}, V_{DD}, Asserted, Hi-Z.'