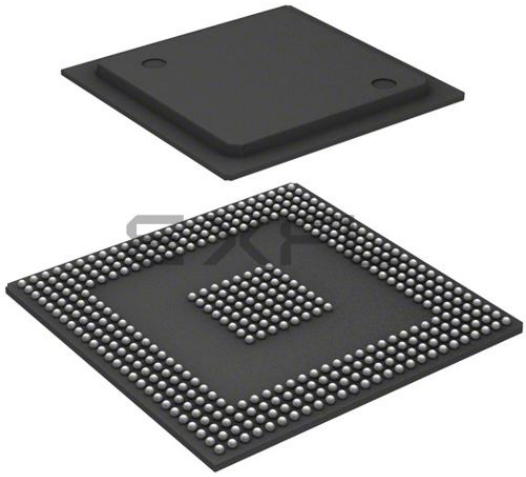

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5566mzp80

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage [2]	V_{DD}	–0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	–0.3	6.5	V
4	Flash read voltage	V_{FLASH}	–0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	–0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	–0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	–0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	–0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	–0.3	5.5	V
10	I/O supply voltage (fast I/O pads) [3]	V_{DDE}	–0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) [3]	V_{DDEH}	–0.3	6.5	V
12	DC input voltage [4] V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	 –1.0 [5] –1.0 [5]	 6.5 [6] 4.6 [7]	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	–0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} – V_{DDA}$	$–V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} – V_{RL}$	–0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} – V_{DDA}$	–5.5	5.5	V
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C

Table 6. V_{RC} and POR Electrical Specifications (continued)

Spec	Characteristic		Symbol	Min.	Max.	Units
9	Absolute value of slew rate on power supply pins		—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$) [6, 7, 8, 9]	– 40° C	BETA [10]	60	—	—
		25° C		65	—	—
		150° C		85	500	—

1 The internal POR signals are V_{POR15}, V_{POR33}, and V_{POR5}. On power up, assert $\overline{RESET}$ before the internal POR negates. $\overline{RESET}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert $\overline{RESET}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.

2 V_{IL_S} (Table 9, Spec15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.

3 Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

4 It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

5 At peak current for device.

6 Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the V_{RCCTL} package signal to the base of the external pass transistor and between the emitter of the pass transistor to the V_{DD} package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). V_{RCCTL} must have a nominal 1 μF phase compensation capacitor to ground. V_{DD} must have a 20 μF (nominal) bulk capacitor (greater than 4 μF over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 μF, two 0.1 μF, and one 1 μF capacitors around the package on the V_{DD} supply signals.

7 I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.

8 Refer to Table 1 for the maximum operating frequency.

9 Values are based on I_{DD} from high-use applications as explained in the I_{DD} Electrical Specification.

10 BETA represents the worst-case external transistor. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).

3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and V_{DDSYN} or the $\overline{RESET}$ power supplies is required if using an external 1.5 V power supply with V_{RC33} tied to ground (GND). To avoid power-sequencing, V_{RC33} must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," and Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)."

Power sequencing requires that V_{DD33} must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33."

Although power sequencing is not required between V_{RC33} and V_{DDSYN} during power up, V_{RC33} must not lead V_{DDSYN} by more than 600 mV or lag by more than 100 mV for the V_{RC} stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by V_{RC33}. If V_{RC33} lags V_{DDSYN} by more than 100 mV, the increase in current consumed can drop V_{DD} low enough to assert the 1.5 V POR again. Oscillations are possible when the

1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
41	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
42	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	–50	50	mV
43	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	–100	100	mV
43a	V_{RC33} to V_{DDSYN} differential voltage	$V_{RC33} - V_{DDSYN}$	–0.1	0.1 [19]	V
44	Analog input differential signal range (with common mode 2.5 V)	V_{IDIFF}	–2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L$ to $T_H)$	T_L	T_H	°C
46	Slew rate on power-supply pins	—	—	50	V/ms

1 V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if SIU_ECCR[EBTS] = 1.

2 $| V_{DDA0} - V_{DDA1} |$ must be < 0.1 V.

3 V_{PP} can drop to 3.0 V during read operations.

4 If standby operation is not required, connect V_{STBY} to ground.

5 Applies to CLKOUT, external bus pins, and Nexus pins.

6 Maximum average RMS DC current.

7 Eight-way cache enabled (L1CSR0[CORG] = 0b0).

8 Average current measured on automotive benchmark.

9 Peak currents can be higher on specialized code.

10 High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an ‘idle’ loop that crosses cache lines is run from cache. Write code to avoid this condition.

11 Four-way cache enabled (L1CSR0[CORG] = 0b1) or (L1CSR0[CORG] = 0b0 with L1CSR0[WAM] = 0b1, L1CSR0[WID] = 0b1111, L1CSR0[WDD] = 0b1111, L1CSR0[AWID] = 0b1, and L1CSR0[AWDD] = 0b1).

12 The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, “Power-Up/Down Sequencing”, Figure 2.

13 Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to Table 11 for values to calculate the power dissipation for a specific operation.

14 Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

15 Absolute value of current, measured at V_{IL} and V_{IH}.

16 Weak pullup/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

17 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 °C to 12 °C, in the ambient temperature range of 50 °C to 125 °C. Applies to pad types: pad_a and pad_ae.

18 V_{SSA} refers to both V_{SSA0} and V_{SSA1}. $| V_{SSA0} - V_{SSA1} |$ must be < 0.1 V.

19 Up to 0.6 V during power up and power down.

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current ($T_A = T_L$ to T_H)[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

1 These values are estimates from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: [1] Crystal reference External reference Dual controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys} \div 2$	MHz
2	System frequency [2]	f_{sys}	$f_{ICO(MIN)} \div 2^{RFD}$	f_{MAX} [3]	MHz
3	System clock period	t_{CYC}	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency [4]	f_{LOR}	100	1000	kHz
5	Self-clocked mode (SCM) frequency [5]	f_{SCM}	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode [6] All other modes [dual controller (1:1), bypass, external reference]	V_{IHEXT} V_{IHEXT}	V_{XTAL} + 0.4 V $(V_{DDE5} \div 2)$ + 0.4 V	— —	V V
7	EXTAL input low voltage crystal mode [7] All other modes [dual controller (1:1), bypass, external reference]	V_{ILEXT} V_{ILEXT}	— —	V_{XTAL} – 0.4 V $(V_{DDE5} \div 2)$ – 0.4 V	V V
8	XTAL current [8]	I_{XTAL}	2	6	mA
9	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L) - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [9]	pF
13	Discrete load capacitance to connect to XTAL	C_{L_XTAL}	—	$(2 \times C_L) - C_{S\_XTAL} - C_{PCB\_XTAL}$ [9]	pF
14	PLL lock time [10]	t_{lpll}	—	750	µs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) [11, 12]	t_{skew}	–2	2	ns
16	Duty cycle of reference	t_{DC}	40	60	%
17	Frequency unLOCK range	f_{UL}	–4.0	4.0	% f_{SYS}
18	Frequency LOCK range	f_{LCK}	–2.0	2.0	% f_{SYS}

Table 12. FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at f_{SYS} max: [13, 14] Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	C_{JITTER}	 — —	 5.0 0.01	% f_{CLKOUT}
20	Frequency modulation range limit [15] (do not exceed f_{sys} maximum)	C_{MOD}	0.8	2.4	$\%f_{SYS}$
21	ICO frequency $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ [16] $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$	f_{ico}	48	f_{MAX}	MHz
22	Predivider output frequency (to PLL)	f_{PREDIV}	4	20 [17]	MHz

1 Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

2 All internal registers retain data at 0 Hz.

3 Up to the maximum frequency rating of the device (refer to Table 1).

4 Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

5 The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below f_{LOR}. SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

6 Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). (V_{extal} – V_{xtal}) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

7 Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). (V_{xtal} – V_{extal}) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

8 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

9 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

10 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

11 PLL is operating in 1:1 PLL mode.

12 V_{DDE} = 3.0–3.6 V.

13 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

14 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

15 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

16 $f_{sys} = f_{ico} \div (2^{RFD})$.

17 Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

3.13.4 External Bus Interface (EBI) Timing

Table 22 lists the timing information for the external bus interface (EBI).

Table 22. Bus Operation Timing [1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]								Unit	Notes
			40 MHz		56 MHz		67 MHz		72 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
1	CLKOUT period	T_C	25.0	—	17.9	—	15.2	—	13.3	—	ns	Signals are measured at 50% V_{DDE}.
2	CLKOUT duty cycle	t_{CDC}	45%	55%	45%	55%	45%	55%	45%	55%	T_C	
3	CLKOUT rise time	t_{CRT}	—	— [4]	—	— [4]	—	— [4]	—	— [4]	ns	
4	CLKOUT fall time	t_{CFT}	—	— [4]	—	— [4]	—	— [4]	—	— [4]	ns	
5	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) External bus interface CS[0:3] ADDR[8:31] DATA[0:31] BDIP BG [5] BR [7] BB OE RD_WR TA TEA TS TSIZ[0:1] WE/BE[0:3]	t_{COH}	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.
	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) Calibration bus interface CAL_CS[0:3] CAL_ADDR[9:30] CAL_DATA[0:15] CAL_OE CAL_RD_WR CAL_TS CAL_WE/BE[0:1]	t_{CCOH}	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.

Table 22. Bus Operation Timing [1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]								Unit	Notes
			40 MHz		56 MHz		67 MHz		72 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
6	CLKOUT positive edge to output signal *valid* (output delay) External bus interface CS[0:3] ADDR[8:31] DATA[0:31] BDIP BG [5] BR [7] BB OE RD_WR TA TEA TS TSIZ[0:1] WE/BE[0:3]	t_{COV}	—	10.0 [6] 11.0	—	7.5 [6] 8.5	—	6.0 [6] 7.0	—	5.0 [6] 6.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.
6a	CLKOUT positive edge to output signal valid (output delay) Calibration bus interface CAL_CS[0:3] CAL_ADDR[9:30] CAL_DATA[0:15] CAL_OE CAL_RD_WR CAL_TS CAL_WE/BE[0:1]	t_{CCOV}	—	11.0 [6] 12.0	—	8.5 [6] 9.5	—	7.0 [6] 8.0	—	6.0 [6] 7.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.
7	Input signal valid to CLKOUT positive edge (setup time) External bus interface ADDR[8:31] DATA[0:31] BG [7] BR [5] BB RD_WR TA TEA TS TSIZ[0:1]	t_{CIS}	10.0	—	7.0	—	5.0	—	4.0	—	ns	

Table 22. Bus Operation Timing [1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]								Unit	Notes
			40 MHz		56 MHz		67 MHz		72 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
7a	Input signal valid to CLKOUT positive edge (setup time) Calibration bus interface CAL_ADDR[9:30] CAL_DATA[0:15] CAL_RD_WR CAL_TS	t_{CCIS}	11.0	—	8.0	—	6.0	—	4.0	—	ns	
8	CLKOUT positive edge to input signal invalid (hold time) External bus interface ADDR[8:31] DATA[0:31] BG [7] BR [5] BB RD_WR TA TEA TS TSIZ[0:1]	t_{CIH}	1.0	—	1.0	—	1.0	—	1.0	—	ns	
	CLKOUT positive edge to input signal invalid (hold time) Calibration bus interface CAL_ADDR[9:30] CAL_DATA[0:15] CAL_RD_WR CAL_TS	t_{CCIH}	1.0	—	1.0	—	1.0	—	1.0	—	ns	

1 EBI timing specified at V_{DDE} = 1.6–3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and CL = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM): 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; 135 MHz parts allow for 132 MHz system clock + 2% FM; and 147 MHz parts allow for 144 MHz system clock + 2% FM.

3 The external bus is limited to half the speed of the internal bus.

4 Refer to fast pad timing in Table 17 and Table 18 (different values for 1.8 V and 3.3 V).

5 Internal arbitration.

6 EBTS = 0 timings are tested and valid at V_{DDE} = 2.25–3.6 V only; EBTS = 1 timings are tested and valid at V_{DDE} = 1.6–3.6 V.

7 External arbitration.

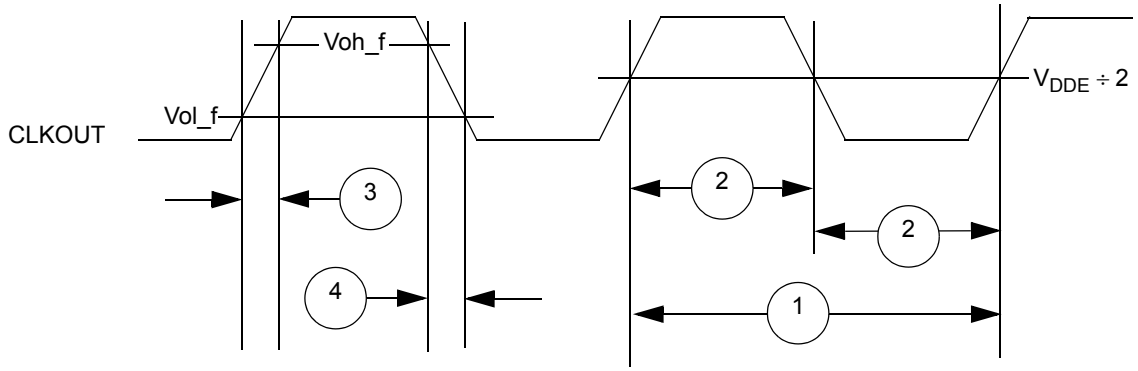

Figure 12. CLKOUT Timing

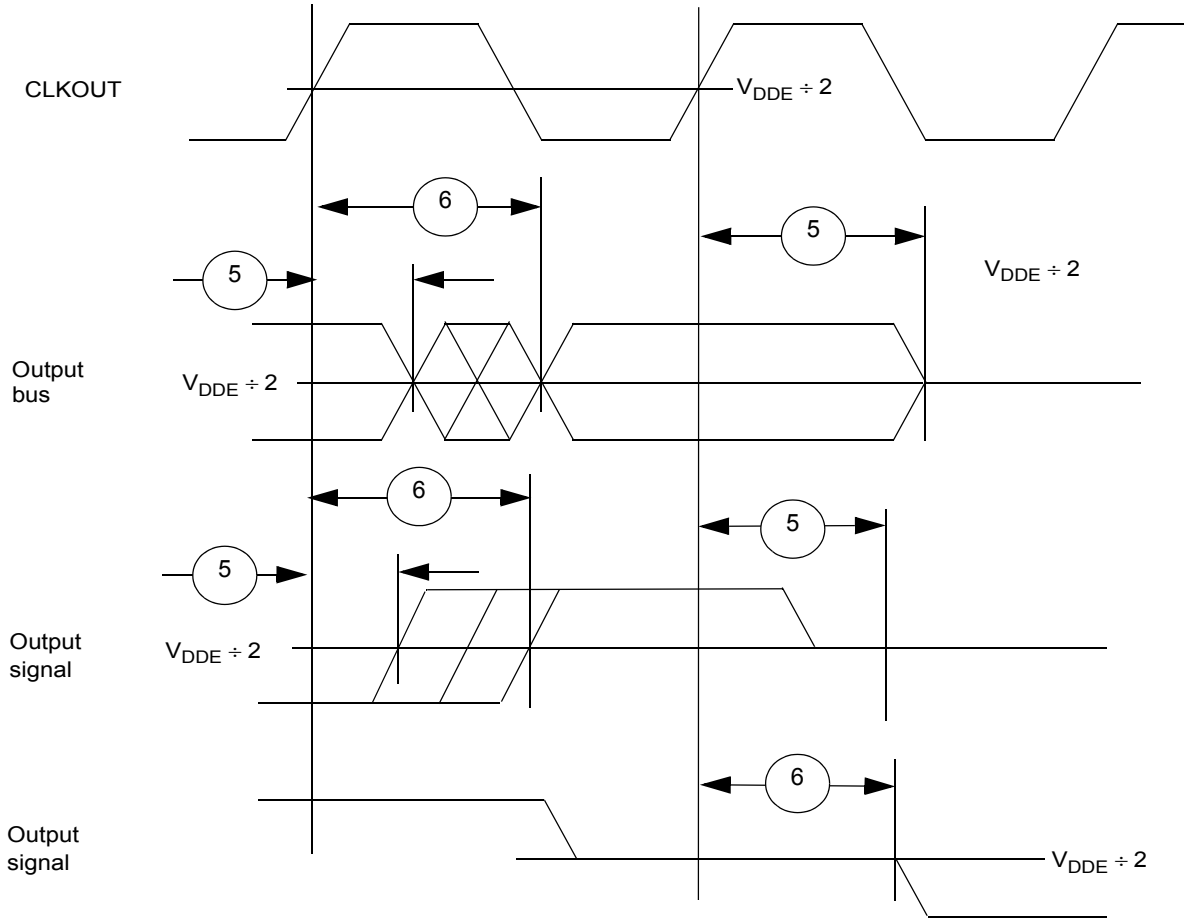

Figure 13. Synchronous Output Timing

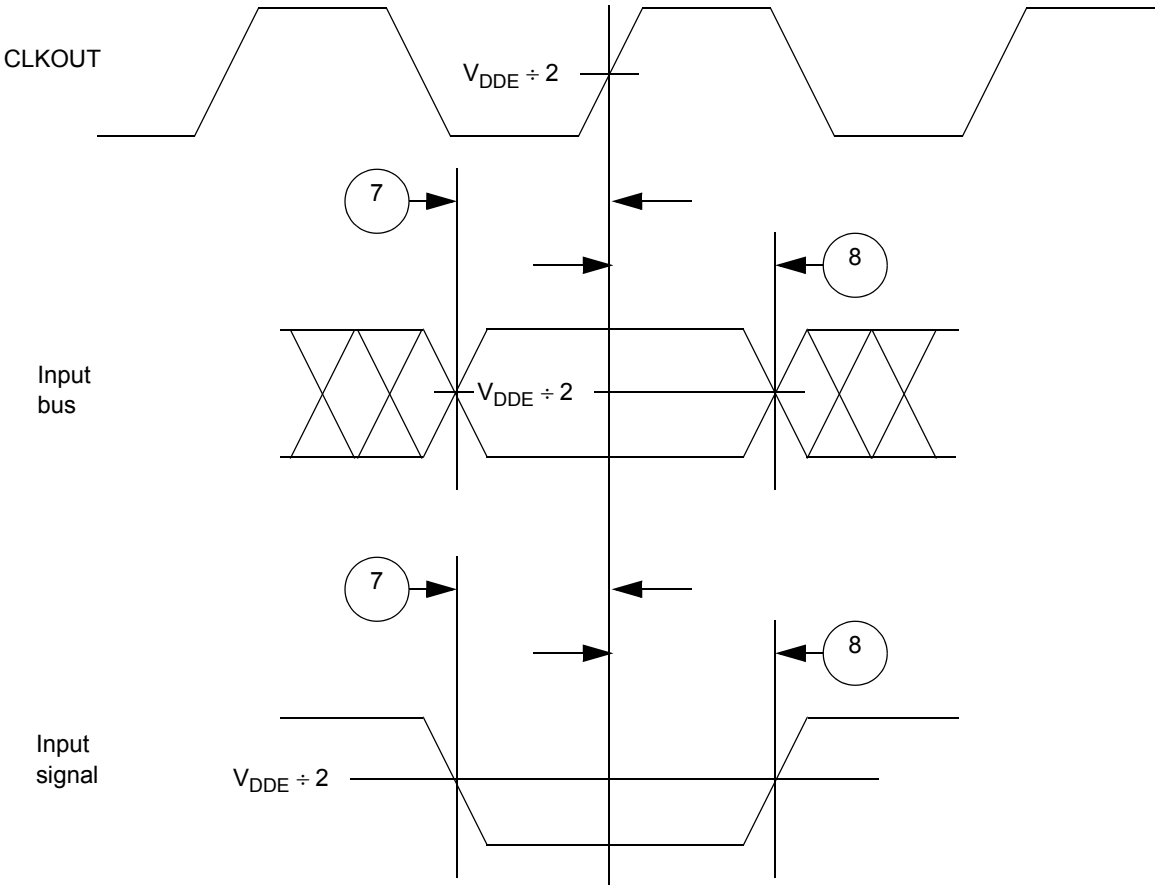

Figure 14. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Signals)

Table 23. External Interrupt Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	IRQ pulse-width low	t_{IPWL}	3	—	t_{CYC}
2	IRQ pulse-width high	T_{IPWH}	3	—	t_{CYC}
3	IRQ edge-to-edge time [2]	t_{ICYC}	6	—	t_{CYC}

1 IRQ timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

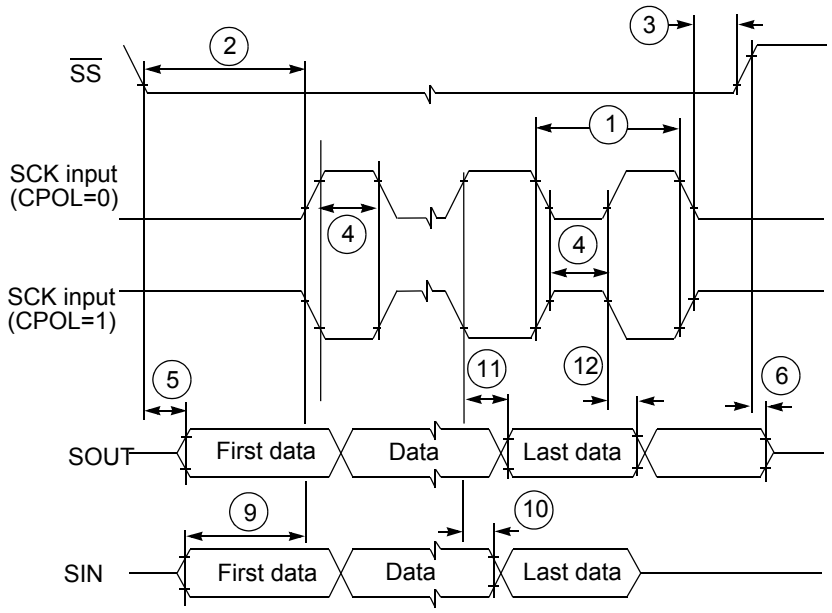

Figure 24. DSPI Modified Transfer Format Timing—Slave, CPHA = 0

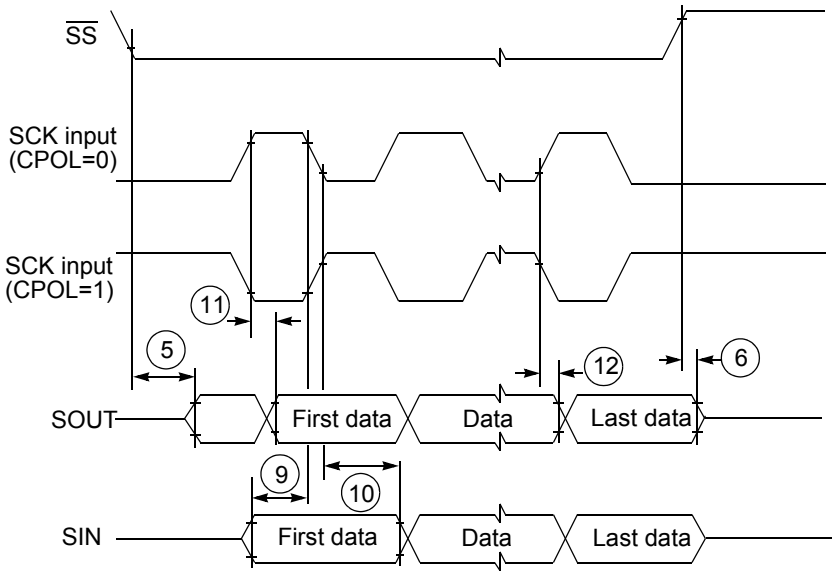

Figure 25. DSPI Modified Transfer Format Timing—Slave, CPHA = 1

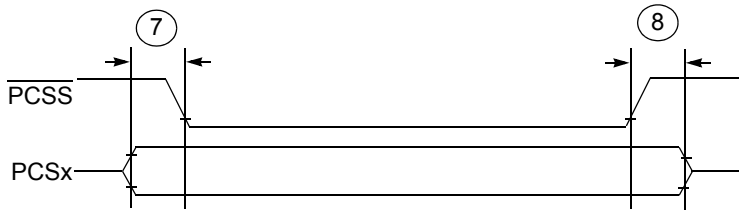

Figure 26. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

3.13.9 eQADC SSI Timing

Table 27. EQADC SSI Timing Characteristics

Spec	Rating	Symbol	Minimum	Typical	Maximum	Unit
2	FCK period ($t_{FCK} = 1 \div f_{FCK}$) [1, 2]	t_{FCK}	2	—	17	t_{SYS_CLK}
3	Clock (FCK) high time	t_{FCKHT}	$t_{SYS\_CLK} - 6.5$	—	$9 \times (t_{SYS\_CLK} + 6.5)$	ns
4	Clock (FCK) low time	t_{FCKLT}	$t_{SYS\_CLK} - 6.5$	—	$8 \times (t_{SYS\_CLK} + 6.5)$	ns
5	SDS lead / lag time	t_{SDS_LL}	–7.5	—	+7.5	ns
6	SDO lead / lag time	t_{SDO_LL}	–7.5	—	+7.5	ns
7	EQADC data setup time (inputs)	t_{EQ_SU}	22	—	—	ns
8	EQADC data hold time (inputs)	t_{EQ_HO}	1	—	—	ns

1 $\overline{SS}$ timing specified at V_{DDEH} = 3.0–5.25 V, $T_A = T_L$ to T_H, and CL = 25 pF with SRC = 0b11. Maximum operating frequency varies depending on track delays, master pad delays, and slave pad delays.

2 FCK duty cycle is not 50% when it is generated through the division of the system clock by an odd number.

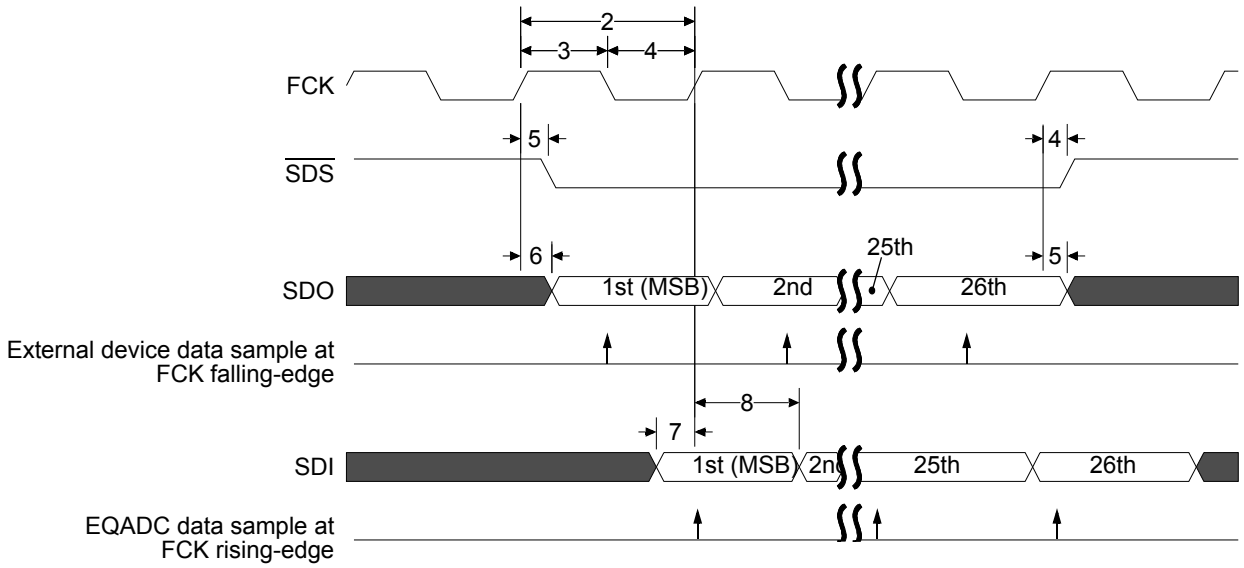

Figure 27. EQADC SSI Timing

4.2 MPC5566 416-Pin Package Dimensions

The package drawings of the MPC5566 416 pin TEPBGA package are shown in Figure 36.

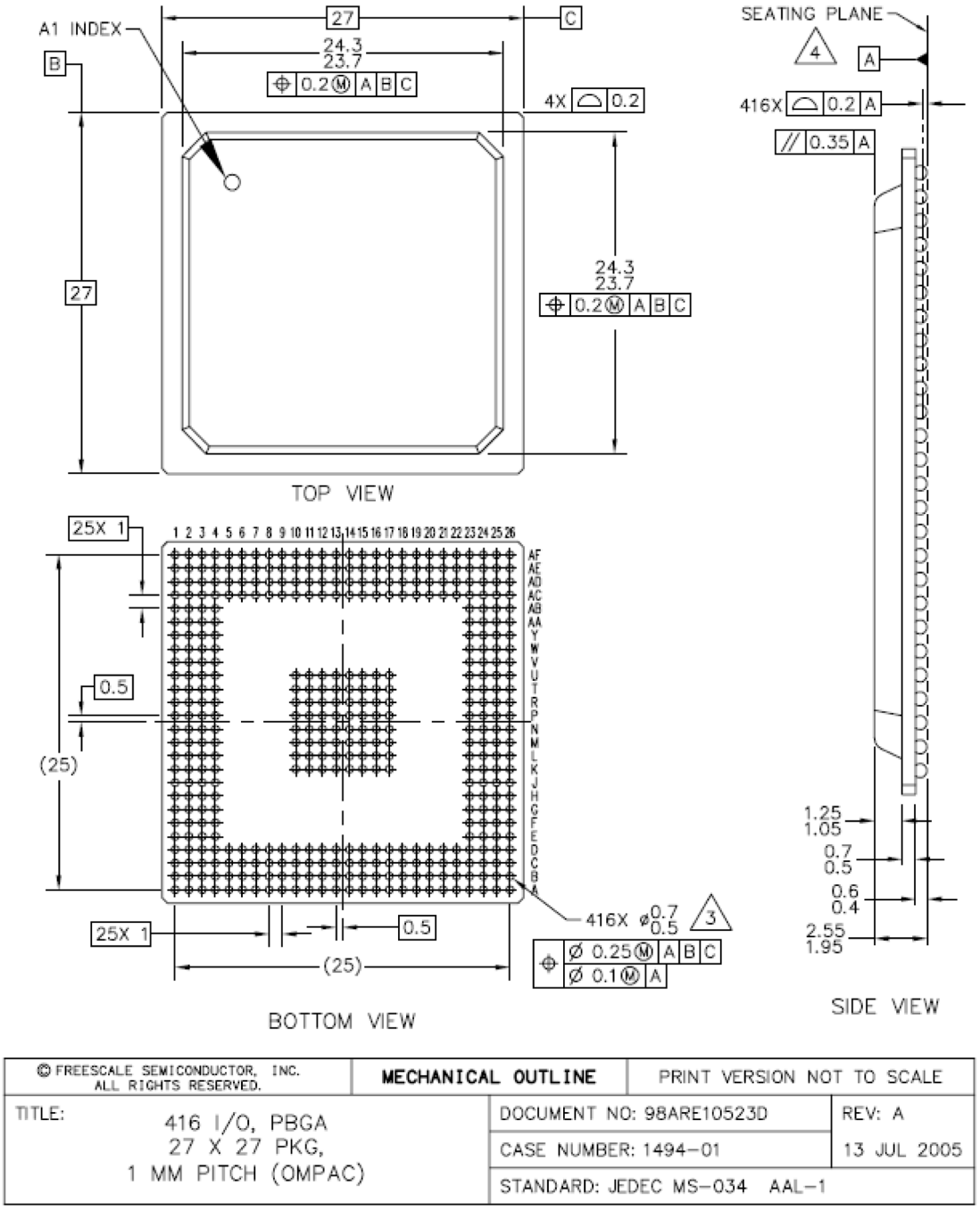

Figure 36. MPC5566 416 TEPBGA Package

5 Revision History for the MPC5566 Data Sheet

The history of revisions made to this data sheet are listed and described in this section. The information that has changed from a previous revision of this document to the current revision is listed for each revision and are grouped in the following categories:

- Global and text changes
- Table and figure changes

Within each category, the information that has changed is listed in sequential order.

5.1 Information Changed Between Revisions 2.0 and 3.0

The following table lists the information that changed in the tables between Rev. 2.0 and 3.0. Click the links to see the change.

Table 32. Changes Between Rev. 2.0 and 3.0

Location	Description of Changes
Section 3.7, "Power-Up/Down Sequencing"	Added the following paragraph in Section 3.7, "Power-Up/Down Sequencing" "During initial power ramp-up, when Vstby is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until VDD is applied. This current will not reoccur until Vstby is lowered below Vstby min. specification".
	Moved Figure 2 (fISTBY Worst-case Specifications) to Section 3.7, "Power-Up/Down Sequencing".
Section 3.8, "DC Electrical Specifications	In Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)) for Spec 27d the Characteristic "Refer to Figure 3 for an interpolation of this data" changed to "RAM standby current".
	Changed the footnote attached to IDD_STBY to "The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, "Power-Up/Down Sequencing",Figure 2 (fISTBY Worst-case Specifications).
	Removed the footnote "Figure 3 shows an illustration of the IDD_STBY values interpolated for these temperature values".

5.2 Information Changed Between Revisions 1.0 and 2.0

The following table lists the information that changed in the tables between Rev. 1.0 and 2.0. Click the links to see the change.

Table 33. Changes Between Rev. 1.0 and 2.0

Location	Description of Changes
Table 3, MPC5566 Thermal Characteristics:	Changed for production purposes, footnote 1 from: Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other *components on the board*, and board thermal resistance. to: Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other *board components*, and board thermal resistance.
Table 6, VCR/POR Electrical Specifications:	Added footnote 1 to specs 1, 2, and 3 that reads: On power up, assert $\overline{\text{RESET}}$ before V_{POR15}, V_{POR33}, and V_{POR5} negate (internal POR). RESET must remain asserted until the power supplies are within the operating conditions as specified in Table 9 *DC Electrical Specifications*. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.
Table 9, DC Electrical Specifications:	• Added footnote that reads: V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if EBTS = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if EBTS =1. • Removed footnote to specs 27a, b, and c on the max values that read: “Preliminary. Specification pending final characterization.” • Removed footnote to specs 27a, b, and c on the max values that read: “Specification pending final characterization.”
Table 16, Flash BIU Settings vs. Frequency of Operation:	• Removed footnote 9 in columns APC and RWSC for 147 MHz row that read: Preliminary setting. Final setting pending characterization.
Table 22, Bus Operation Timing:	• External Bus Frequency in the table heading: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM, 135 MHz parts allow for 132 MHz system clock + 2% FM; and 147 MHz parts allow for 144 MHz system clock + 2% FM. • Spec 1: Changed the values in Min. columns: 40 MHz from 25 to 24.4; 56 MHz from 17.9 to 17.5 • Specs 7 and 8: Removed from external bus interface: $\overline{\text{BDIP}}$, $\overline{\text{OE}}$, TSIZ[0:1], and $\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3].
Table 26, DSPI Timing:	• Table Title: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM, 135 MHz parts allow for 132 MHz system clock + 2% FM; and 147 MHz parts allow for 144 MHz system clock + 2% FM. • Removed footnote that reads: “Specification pending final characterization.” • Spec 2, *PCS to SCK delay*, 144 MHz, min. 12 • Spec 3, *After SCK delay*, 144 MHz, min. 11 • Spec 9, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. 7 • Spec 10, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. 11 • Spec 11, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, max. 12 • Spec 12, *Master (MTFE = 1, CPHA = 0)*, 144 MHz, min. 1

Table 34. Global and Text Changes Between Rev. 0.0 and 1.0 (continued)

Location	Description of Changes
Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33:"	Added the following text directly before this section and after Table 8 *Pin Status for Medium / Slow Pads During the Power-on Sequence*: 'The values in Table 7 and Table 8 do not include the effect of the weak pull devices on the output pins during power up. Before exiting the internal POR state, the voltage on the pins goes to high-impedance until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak pull devices (up or down) are enabled as defined in the device *Reference Manual*. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}. To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.'
Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)"	Deleted the underscore in ORed_POR to become ORed POR.

The following table lists the information that changed in the figures or tables between Rev. 0.0 and 1.0.

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0

Location	Description of Changes
Figure 1, MPC5500 Family Part Numbers:	• Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text. • Changed Qualification Status by adding ', general market flow' to the M designator, and added an 'S' designator with the description of 'Fully spec. qualified, automotive flow.

Table 1, Orderable Part Numbers:	• Added a 144 MHz system frequency option for:
	  • MPC5566MVR144, Pb-Free (lead free), nominal 144, maximum 147
	  • MPC5566MZP144, SnPb (leaded), nominal 144, maximum 147
	• Changed the 132 MHz maximum operating frequency to 135 MHz.
	• Reordered rows to group devices by lead-free package types in descending frequency order, and leaded package types.
	• Footnote 1 added that reads: All devices are PPC5566, rather than MPC5566 or SPC5566, until product qualifications are complete. Not all configurations are available in the PPC parts.
	• Footnote 2 added that reads: The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.
	• Changed footnote 3 from '132 MHz allows only 128 MHz + 2% FM' to '135 MHz parts allow for 132 MHz systems clock + 2% FM'; and added '147 MHz parts allow for 144 MHz systems clock + 2% FM.

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 9, DC Electrical Specifications:	• Spelled out meaning of the slash '/' as 'and' as well as 'I/O' as 'input/output.' Sentence still very confusing. Deleted 'input/output' from the specs to improve clarity. • Spec 20, column 2, *Characteristics*,' Slow and medium output high voltage (I_{OH_S} = –2.0 mA):' Created a left-justified second line and moved 'I_{OH_S} = –2.0 mA' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OH_S} = –1.0 mA.' • Spec 20, column 4, *Min*: Added a blank line before and after '0.80 × V_{DDEH}' and put '0.85 × V_{DDEH}' on the last line. • Spec 22, column 2, '*Slow and medium output low voltage (I_{OL_S} = 2.0 mA)*:' Created a left-justified second line and moved 'I_{OL_S} = 2.0 mA.' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OL_S} = 1.0 mA.' • Spec 22, column 5, *Max*: Added a blank line before and after '0.20 × V_{DDEH}' and put '0.15 × V_{DDEH}' on the last line. • Spec 26: Changed 'AN[12]_MA[1]_SDO' to 'AN[13]_MA[1]_SDO'. • Added footnote 10 to specs 27a, b, and c on the 4-way cache line that reads: Four-way cache enabled (L1CSR0[CORG] = 0b1) or (L1CSR0[CORG] = 0b0 with L1CSR0[WAM] = 0b1, L1CSR0[WID] = 0b1111, L1CSR0[WDD] = 0b1111, L1CSR0[AWID] = 0b1, and L1CSR0[AWDD] = 0b1). • Added footnote 11 to specs 27a, b, and c on the max numeric values: "Preliminary. Specification pending final characterization." • Added footnote 12 to specs 27a, b, and c on the max TBD values: "Specification pending final characterization." • Spec 27a: *Operating current 1.5 V supplies @ 132 MHz*: Changed 132 MHz to 135 MHz. Changed maximum values for 8-way cache: All 8-way cache max values have footnote 18. -- 1.65 typical = 630 -- 1.35 typical = 500 -- 1.65 high = 785 -- 1.35 high = 630 Changed 4-way cache with footnote 10: -- 1.65 high = 685 -- 1.35 high = TBD with footnote 19. • Spec 27b, *Operating current 1.5 V supplies @ 114 MHz*: Changed maximum values for 8-way cache. All 8-way cache max values have footnote 18: -- 1.65 typical = 600 -- 1.35 typical = 450 -- 1.65 high = 680 -- 1.35 high = 500 Changed 4-way cache values: -- 1.65 high = TBD with footnote 19 -- 1.35 high = TBD with footnote 19 • Spec 27c, *Operating current 1.5 V supplies @ 82 MHz*: Changed maximum values for 8-way cache: All 8-way cache max values have footnote 18. -- 1.65 typical = 490, -- 1.35 typical = 360, -- 1.65 high = 520, -- 1.35 high = 390. Changed 4-way cache values: -- 1.65 high = TBD with footnote 19 -- 1.35 high = TBD with footnote 19

Table 35. Table and Figure Changes Between Rev. 0.0 and Rev. 1.0 (continued)

Location	Description of Changes
Table 27, EQADC SSI Timing Characteristics:	• Deleted from table title '(Pads at 3.3 V or 5.0 V)' • Deleted 1st line in table 'CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.' • Spec 1: FCK frequency -- removed. • Combined footnotes 1 and 2, and moved the new footnote to Spec 2. Moved old footnote 3 that is now footnote 2 to Spec 2. • Footnote 1, deleted 'V_{DD} = 1.35–1.65 V' and 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V.' Changed 'CL = 50 pF' to 'CL = 25 pF.' • Footnote 2: added 'cycle' after 'duty' to read: FCK duty cycle is not 50% when . . . .
Figure 35, MPC5566 416 Package: Deleted the version number and date.	