**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | H8/300H |
| Core Size | 16-Bit |
| Speed | 25MHz |
| Connectivity | SCI, SmartCard |
| Peripherals | DMA, PWM, WDT |
| Number of I/O | 70 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BFQFP |
| Supplier Device Package | 100-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df3068fbl25v |

| Type | Symbol | Pin No. FP-100B TFP-100B | I/O | Name and Function |
|---|---|---|---|---|
| I/O ports | $P6_7$ to $P6_0$ | 61, 72 to 69, 60 to 58 | Input/ output | **Port 6:** Eight input/output pins. The direction of each pin can be selected in the port 6 data direction register (P6DDR). |
| | $P7_7$ to $P7_0$ | 85 to 78 | Input | **Port 7:** Eight input pins |
| | $P8_4$ to $P8_0$ | 91 to 87 | Input/ output | **Port 8:** Five input/output pins. The direction of each pin can be selected in the port 8 data direction register (P8DDR). |
| | $P9_5$ to $P9_0$ | 17 to 12 | Input/ output | **Port 9:** Six input/output pins. The direction of each pin can be selected in the port 9 data direction register (P9DDR). |
| | $PA_7$ to $PA_0$ | 100 to 93 | Input/ output | **Port A:** Eight input/output pins. The direction of each pin can be selected in the port A data direction register (PADDR). |
| | $PB_7$ to $PB_0$ | 9 to 2 | Input/ output | **Port B:** Eight input/output pins. The direction of each pin can be selected in the port B data direction register (PBDDR). |

| Interrupt Source | Origin | Vector Number | Vector Address* Advanced Mode | Vector Address* Normal Mode | IPR | Priority |
|---|---|---|---|---|---|---|
| IMIA2 (compare match/ input capture A2) | 16-bit timer channel 2 | 32 | H'0080 to H'0083 | H'0040 to H'0041 | IPRA0 | High |
| IMIB2 (compare match/ input capture B2) | | 33 | H'0084 to H'0087 | H'0042 to H'0043 | | |
| OVI2 (overflow 2) | | 34 | H'0088 to H'008B | H'0044 to H'0045 | | |
| Reserved | — | 35 | H'008C to H'008F | H'0046 to H'0047 | | |
| CMIA0 (compare match A0) | 8-bit timer channel 0/1 | 36 | H'0090 to H'0093 | H'0048 to H'0049 | IPRB7 | |
| CMIB0 (compare match B0) | | 37 | H'0094 to H'0097 | H'004A to H'004B | | |
| CMIA1/CMIB1 (compare match A1/B1) | | 38 | H'0098 to H'009B | H'004C to H'004D | | |
| TOVI0/TOVI1 (overflow 0/1) | | 39 | H'009C to H'009F | H'004E to H'004F | | |
| CMIA2 (compare match A2) | 8-bit timer channel 2/3 | 40 | H'00A0 to H'00A3 | H'0050 to H'0051 | IPRB6 | |
| CMIB2 (compare match B2) | | 41 | H'00A4 to H'00A7 | H'0052 to H'0053 | | |
| CMIA3/CMIB3 (compare match A3/B3) | | 42 | H'00A8 to H'00AB | H'0054 to H'0055 | | |
| TOVI2/TOVI3 (overflow 2/3) | | 43 | H'00AC to H'00AF | H'0056 to H'0057 | | |
| DEND0A | DMAC | 44 | H'00B0 to H'00B3 | H'0058 to H'0059 | IPRB5 | |
| DEND0B | | 45 | H'00B4 to H'00B7 | H'005A to H'005B | | |
| DEND1A | | 46 | H'00B8 to H'00BB | H'005C to H'005D | | |
| DEND1B | | 47 | H'00BC to H'00BF | H'005E to H'005F | | |
| Reserved | — | 48 | H'00C0 to H'00C3 | H'0060 to H'0061 | — | |
| | | 49 | H'00C4 to H'00C7 | H'0062 to H'0063 | | |
| | | 50 | H'00C8 to H'00CB | H'0064 to H'0065 | | |
| | | 51 | H'00CC to H'00CF | H'0066 to H'0067 | | Low |

Note: * Lower 16 bits of the address.

### 6.2.2 Access State Control Register (ASTCR)

ASTCR is an 8-bit readable/writable register that selects whether each area is accessed in two states or three states.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | AST7 | AST6 | AST5 | AST4 | AST3 | AST2 | AST1 | AST0 |
| Initial value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Bits selecting number of states for access to each area

ASTCR is initialized to H'FF by a reset and in hardware standby mode. It is not initialized in software standby mode.

**Bits 7 to 0—Area 7 to 0 Access State Control (AST7 to AST0):** These bits select whether the corresponding area is accessed in two or three states.

| Bits 7 to 0<br>AST7 to AST0 | Description | |
|---|---|---|
| 0 | Areas 7 to 0 are accessed in two states | |
| 1 | Areas 7 to 0 are accessed in three states | (Initial value) |

ASTCR specifies the number of states in which external areas are accessed. On-chip memory and registers are accessed in a fixed number of states that does not depend on ASTCR settings. These settings are therefore meaningless in the single-chip modes (modes 6 and 7).

When the corresponding area is designated as DRAM space by bits DRAS2 to DRAS0 in DRAM control register A (DRCRA), the number of access states does not depend on the AST bit setting. When an AST bit is cleared to 0, programmable wait insertion is not performed.

**Table 6.3 Bus Specifications for Each Area (Basic Bus Interface)**

| ABWCR | ASTCR | WCRH/WCRL | | Bus Specifications (Basic Bus Interface) | | |
|---|---|---|---|---|---|---|
| ABWn | ASTn | Wn1 | Wn0 | Bus Width | Access States | Program Wait States |
| 0 | 0 | — | — | 16 | 2 | 0 |
| | 1 | 0 | 0 | | 3 | 0 |
| | | | 1 | | | 1 |
| | | 1 | 0 | | | 2 |
| | | | 1 | | | 3 |
| 1 | 0 | — | — | 8 | 2 | 0 |
| | 1 | 0 | 0 | | 3 | 0 |
| | | | 1 | | | 1 |
| | | 1 | 0 | | | 2 |
| | | | 1 | | | 3 |

Note: n = 7 to 0

### 6.3.3 Memory Interfaces

The H8/3068F memory interfaces comprise a basic bus interface that allows direct connection of ROM, SRAM, and so on; a DRAM interface that allows direct connection of DRAM; and a burst ROM interface that allows direct connection of burst ROM. The interface can be selected independently for each area.

An area for which the basic bus interface is designated functions as normal space, an area for which the DRAM interface is designated functions as DRAM space, and area 0 for which the burst ROM interface is designated functions as burst ROM space.

### 6.3.5 Address Output Method

The H8/3068F provides a choice of two address update methods: either the same method as in the previous H8/300H Series (address update mode 1), or a method in which address update is restricted to external space accesses or self-refresh cycles (address update mode 2).

Figure 6.5 shows examples of address output in these two update modes.

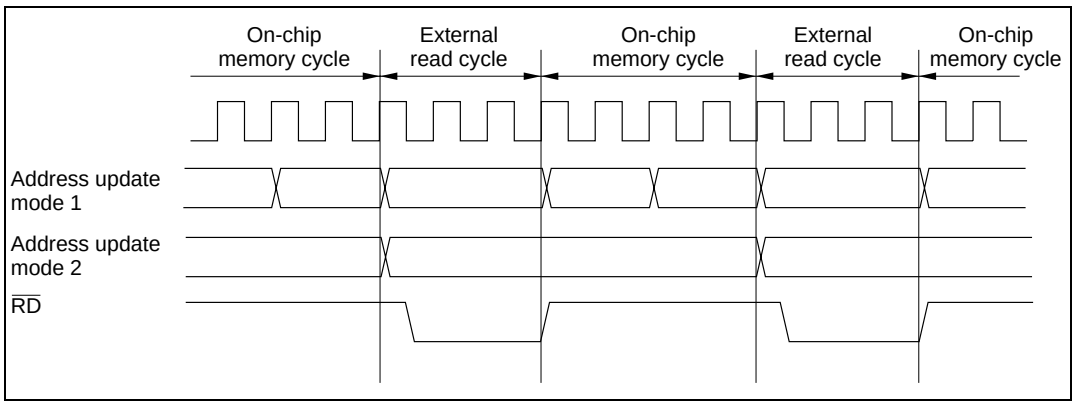



**Figure 6.5 Sample Address Output in Each Address Update Mode (Basic Bus Interface, 3-State Space)**

**Address Update Mode 1:** Address update mode 1 is compatible with the previous H8/300H Series. Addresses are always updated between bus cycles.

**Address Update Mode 2:** In address update mode 2, address updating is performed only in external space accesses or self-refresh cycles. In this mode, the address can be retained between an external space read cycle and an instruction fetch cycle (on-chip memory) by placing the program in on-chip memory. Address update mode 2 is therefore useful when connecting a device that requires address hold time with respect to the rise of the $\overline{RD}$ strobe.

Switching between address update modes 1 and 2 is performed by means of the ADRCTL bit in ADRCR. The initial value of ADRCR is the address update mode 1 setting, providing compatibility with the previous H8/300H Series.

## 8.2 Port 1

### 8.2.1 Overview

Port 1 is an 8-bit input/output port also used for address output, with the pin configuration shown in figure 8.1. The pin functions differ between the expanded modes with on-chip ROM disabled, expanded modes with on-chip ROM enabled, and single-chip mode. In modes 1 to 4 (expanded modes with on-chip ROM disabled), they are address bus output pins ($A_7$ to $A_0$).

In modes 5 (expanded modes with on-chip ROM enabled), settings in the port 1 data direction register (P1DDR) can designate pins for address bus output ($A_7$ to $A_0$) or generic input. In mode 6 and 7 (single-chip mode), port 1 is a generic input/output port.

When DRAM is connected to area 2, 3, 4, 5, $A_7$ to $A_0$ output row and column addresses in read and write cycles. For details see section 6.5, DRAM Interface.

Pins in port 1 can drive one TTL load and a 90-pF capacitive load. They can also drive an LED or a darlington transistor pair.

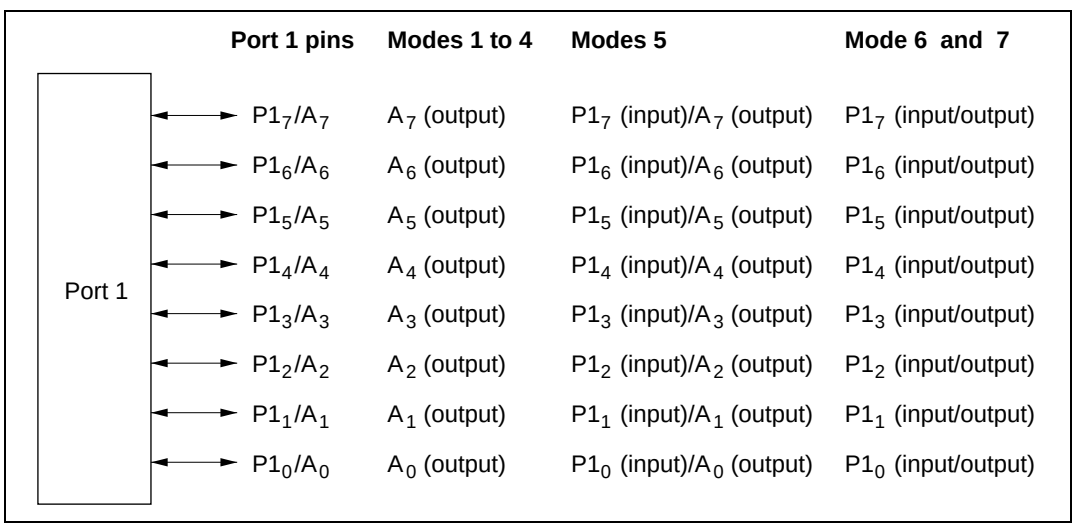



**Figure 8.1 Port 1 Pin Configuration**

### 9.5.3 Interrupt Sources

Each 16-bit timer channel can generate a compare match/input capture A interrupt, a compare match/input capture B interrupt, and an overflow interrupt. In total there are nine interrupt sources of three kinds, all independently vectored. An interrupt is requested when the interrupt request flag are set to 1.

The priority order of the channels can be modified in interrupt priority registers A (IPRA). For details see section 5, Interrupt Controller.

Table 9.6 lists the interrupt sources.

**Table 9.6 16-bit timer Interrupt Sources**

| Channel | Interrupt Source | Description | Priority* |
|---|---|---|---|
| 0 | IMIA0 | Compare match/input capture A0 | High |
| | IMIB0 | Compare match/input capture B0 | |
| | OVI0 | Overflow 0 | |
| 1 | IMIA1 | Compare match/input capture A1 | |
| | IMIB1 | Compare match/input capture B1 | |
| | OVI1 | Overflow 1 | |
| 2 | IMIA2 | Compare match/input capture A2 | |
| | IMIB2 | Compare match/input capture B2 | |
| | OVI2 | Overflow 2 | Low |

Note: * The priority immediately after a reset is indicated. Inter-channel priorities can be changed by settings in IPRA.

**Bit 7—Watchdog Timer Reset (WRST):** During watchdog timer operation, this bit indicates that TCNT has overflowed and generated a reset signal. This reset signal resets the entire H8/3068F chip internally.

| Bit 7 WRST | Description |
|---|---|
| 0 | [Clearing condition]<br>Reset signal at $\overline{RES}$ pin.<br>Read WRST when WRST =1, then write 0 in WRST. (Initial value) |
| 1 | [Setting condition]<br>Set when TCNT overflow generates a reset signal during watchdog timer operation |

**Bit 6—Reserved**

**Bits 5 to 0—Reserved:** These bits cannot be modified and are always read as 1.

### 12.2.4 Notes on Register Access

The watchdog timer's TCNT, TCSR, and RSTCSR registers differ from other registers in being more difficult to write. The procedures for writing and reading these registers are given below.

**Writing to TCNT and TCSR:** These registers must be written by a word transfer instruction. They cannot be written by byte instructions. Figure 12.2 shows the format of data written to TCNT and TCSR. TCNT and TCSR both have the same write address. The write data must be contained in the lower byte of the written word. The upper byte must contain H'5A (password for TCNT) or H'A5 (password for TCSR). This transfers the write data from the lower byte to TCNT or TCSR.

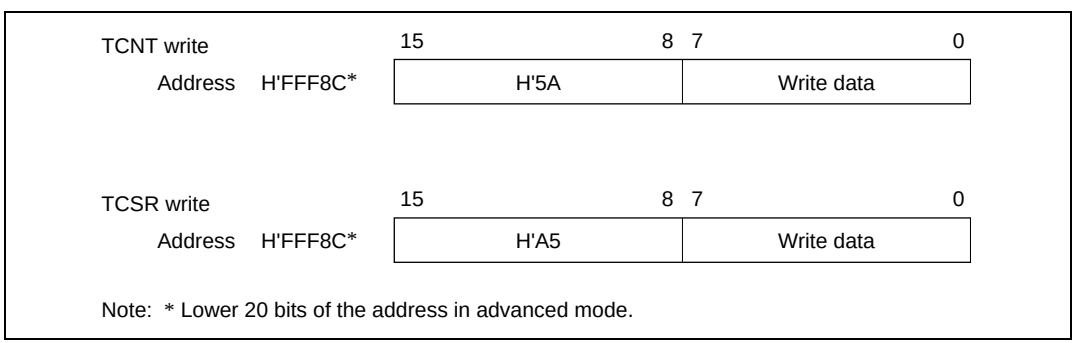



**Figure 12.2 Format of Data Written to TCNT and TCSR**

**Synchronous mode**

Serial data communication is synchronized with a clock signal. The SCI can communicate with other chips having a synchronous communication function.

There is a single serial data communication format.

— Data length: 8 bits

— Receive error detection: overrun errors

- Full-duplex communication

  The transmitting and receiving sections are independent, so the SCI can transmit and receive simultaneously. The transmitting and receiving sections are both double-buffered, so serial data can be transmitted and received continuously.
- The following settings can be made for the serial data to be transferred:

  — LSB-first or MSB-first transfer

  — Inversion of data logic level
- Built-in baud rate generator with selectable bit rates
- Selectable transmit/receive clock sources: internal clock from baud rate generator, or external clock from the SCK pin
- Four types of interrupts

  Transmit-data-empty, transmit-end, receive-data-full, and receive-error interrupts are requested independently. The transmit-data-empty and receive-data-full interrupts from SCI0 can activate the DMA controller (DMAC) to transfer data.

Features of the smart card interface are listed below.

- Asynchronous communication
  — Data length: 8 bits
  — Parity bits generated and checked
  — Error signal output in receive mode (parity error)
  — Error signal detect and automatic data retransmit in transmit mode
  — Supports both direct convention and inverse convention
- Built-in baud rate generator with selectable bit rates
- Three types of interrupts

  Transmit-data-empty, receive-data-full, and transmit/receive-error interrupts are requested independently. The transmit-data-empty and receive-data-full interrupts can activate the DMA controller (DMAC) to transfer data.

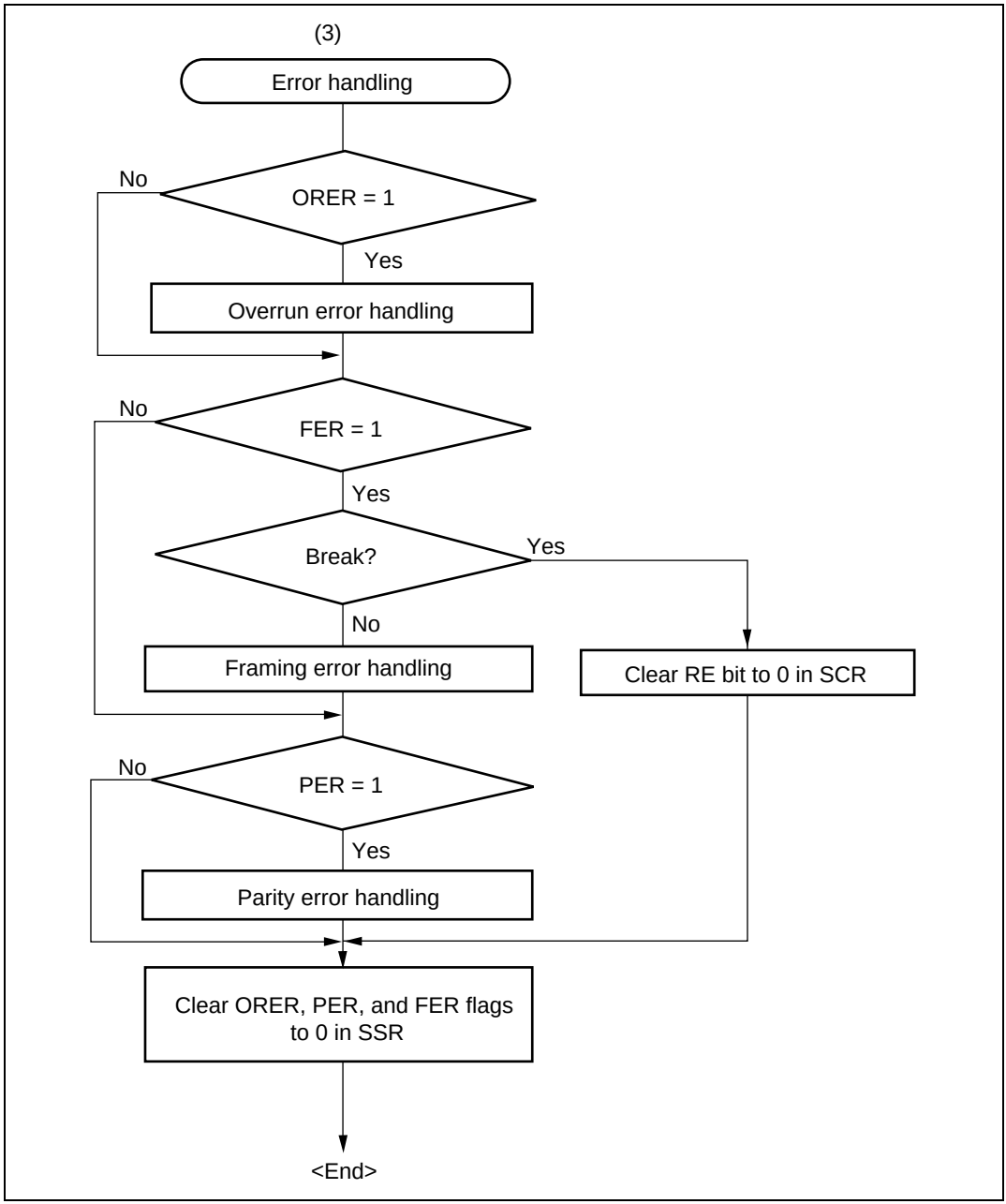
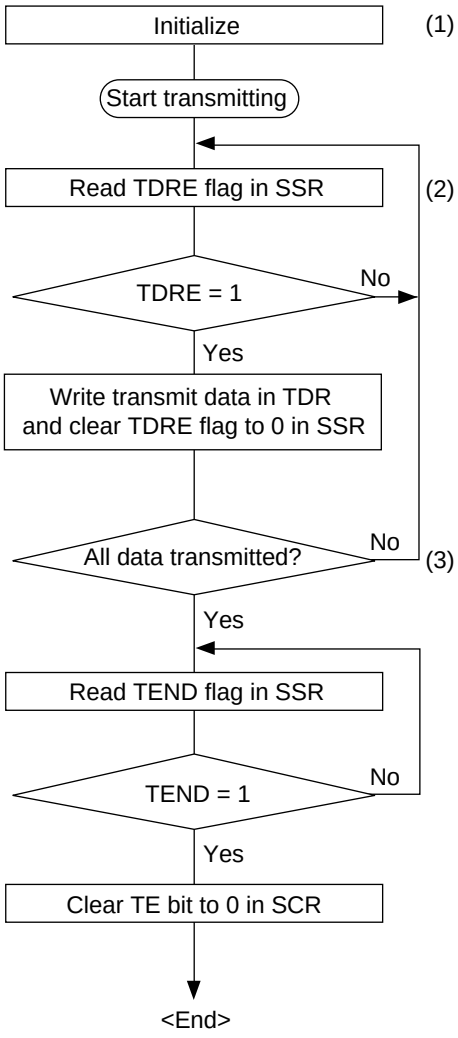



**Figure 13.7 Sample Flowchart for Receiving Serial Data (2)**

- Transmitting Serial Data (Synchronous Mode): Figure 13.16 shows a sample flowchart for transmitting serial data and indicates the procedure to follow.




(1) SCI initialization: the transmit data output function of the TxD pin is selected automatically.

(2) SCI status check and transmit data write: read SSR, check that the TDRE flag is 1, then write transmit data in TDR and clear the TDRE flag to 0.

(3) To continue transmitting serial data: after checking that the TDRE flag is 1, indicating that data can be written, write data in TDR, then clear the TDRE flag to 0. When the DMAC is activated by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE flag is checked and cleared automatically.

**Figure 13.16 Sample Flowchart for Serial Transmitting**

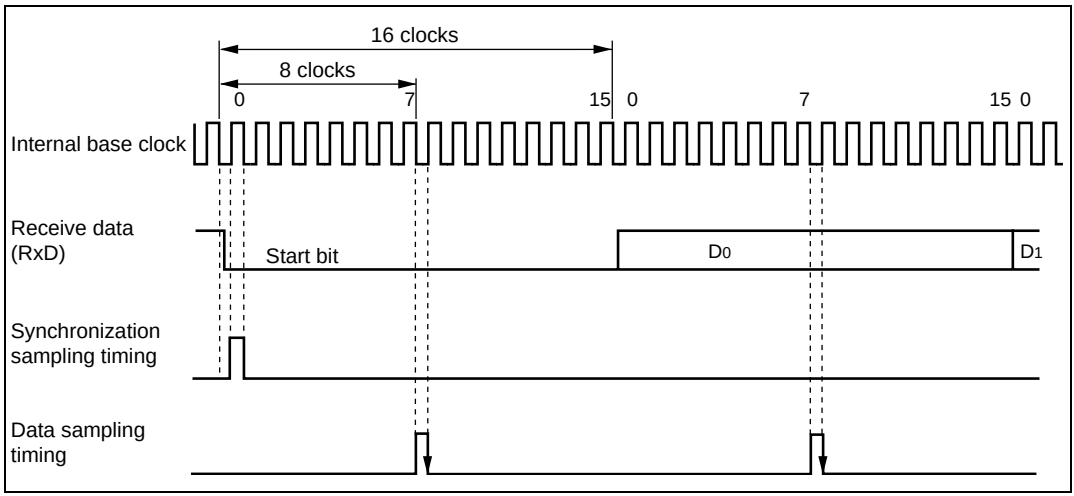



**Figure 13.21 Receive Data Sampling Timing in Asynchronous Mode**

The receive margin in asynchronous mode can therefore be expressed as shown in equation (1).

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\,F - \frac{|D - 0.5|}{N}\,(1 + F) \right| \times 100\% \quad \ldots\ldots\ldots (1)$$

M: Receive margin (%)
N: Ratio of clock frequency to bit rate (N = 16)
D: Clock duty cycle (L = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute deviation of clock frequency

From equation (1), if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation (2).

$$D = 0.5,\ F = 0$$

$$M = (0.5 - \frac{1}{2 \times 16}) \times 100\%$$

$$= 46.875\% \quad \ldots\ldots\ldots (2)$$

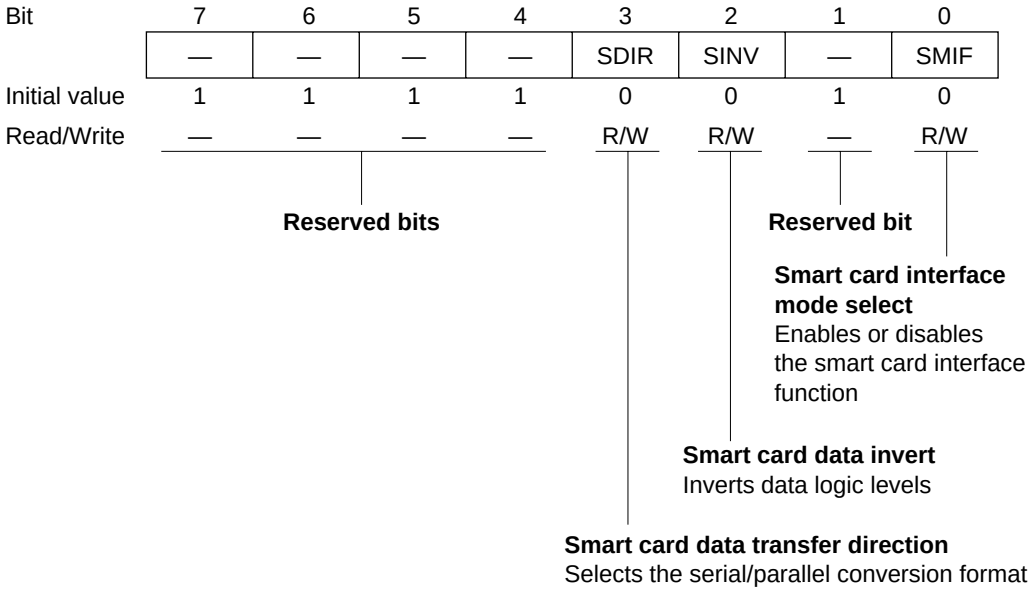
This is a theoretical value. A reasonable margin to allow in system designs is 20% to 30%.

## 14.2 Register Descriptions

This section describes the new or modified registers and bit functions in the smart card interface.

### 14.2.1 Smart Card Mode Register (SCMR)

SCMR is an 8-bit readable/writable register that selects smart card interface functions.

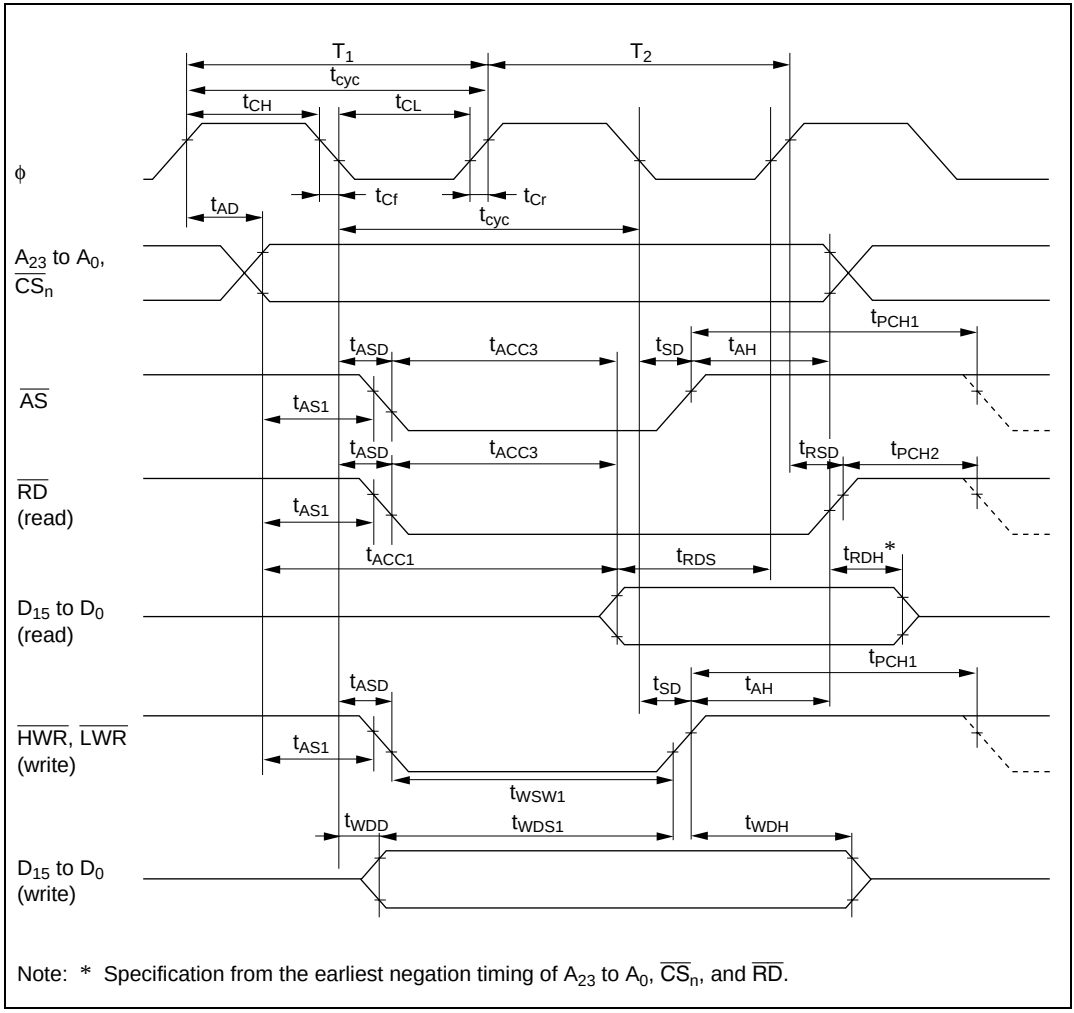



SCMR is initialized to H'F2 by a reset and in standby mode.

**Bits 7 to 4—Reserved:** Read-only bits, always read as 1.

**Bit 3—Smart Card Data Transfer Direction (SDIR):** Selects the serial/parallel conversion format.*[1]

| Bit 3 SDIR | Description | |
|---|---|---|
| 0 | TDR contents are transmitted LSB-first | (Initial value) |
| | Receive data is stored LSB-first in RDR | |
| 1 | TDR contents are transmitted MSB-first | |
| | Receive data is stored MSB-first in RDR | |




Note: * Specification from the earliest negation timing of $A_{23}$ to $A_0$, $\overline{CS}_n$, and $\overline{RD}$.

**Figure 21.8 Basic Bus Cycle: Two-State Access**

| DRCRA—DRAM Control Register A | H'EE026 | DRAM interface |
|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DRAS2 | DRAS1 | DRAS0 | — | BE | RDM | SRFMD | RFSHE |
| Initial value | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | — | R/W | R/W | R/W | R/W |

Refresh pin enable

| | |
|---|---|
| 0 | $\overline{\text{RFSH}}$ pin refresh signal output is disabled |
| 1 | $\overline{\text{RFSH}}$ pin refresh signal output is enabled |

Self-refresh mode

| | |
|---|---|
| 0 | DRAM self-refreshing is disabled in software standby mode |
| 1 | DRAM self-refreshing is enabled in software standby mode |

RAS down mode

| | |
|---|---|
| 0 | DRAM interface: RAS up mode selected |
| 1 | DRAM interface: RAS down mode selected |

Burst access enable

| | |
|---|---|
| 0 | Burst disabled (always full access) |
| 1 | DRAM space access performed in fast page mode |

DRAM area select

| DRAS2 | DRAS1 | DRAS0 | Area 5 | Area 4 | Area 3 | Area 2 |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Normal | Normal | Normal | Normal |
| | | 1 | Normal | Normal | Normal | DRAM space ($\overline{\text{CS}}_2$) |
| | 1 | 0 | Normal | Normal | DRAM space ($\overline{\text{CS}}_3$) | DRAM space ($\overline{\text{CS}}_2$) |
| | | 1 | Normal | Normal | DRAM space($\overline{\text{CS}}_2$)* | |
| 1 | 0 | 0 | Normal | DRAM space ($\overline{\text{CS}}_4$) | DRAM space ($\overline{\text{CS}}_3$) | DRAM space ($\overline{\text{CS}}_2$) |
| | | 1 | DRAM space ($\overline{\text{CS}}_5$) | DRAM space ($\overline{\text{CS}}_4$) | DRAM space ($\overline{\text{CS}}_3$) | DRAM space ($\overline{\text{CS}}_2$) |
| | 1 | 0 | DRAM space($\overline{\text{CS}}_4$)* | | DRAM space($\overline{\text{CS}}_2$)* | |
| | | 1 | DRAM space($\overline{\text{CS}}_2$)* | | | |

Note: * A single $\overline{\text{CSn}}$ pin serves as a common $\overline{\text{RAS}}$ output pin for a number of areas. Unused $\overline{\text{CSn}}$ pins can be used as input/output ports.

| P2PCR—Port 2 Input Pull-Up Control Register | H'EE03C | Port 2 |
|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | $P2_7PCR$ | $P2_6PCR$ | $P2_5PCR$ | $P2_4PCR$ | $P2_3PCR$ | $P2_2PCR$ | $P2_1PCR$ | $P2_0PCR$ |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Port 2 input pull-up control 7 to 0

| | |
|---|---|
| 0 | Input pull-up transistor is off |
| 1 | Input pull-up transistor is on |

Note: Valid when the corresponding P2DDR bit is cleared to 0 (designating generic input).

| TISRA—Timer Interrupt Status Register A | H'FFF64 | 16-bit timer (all channels) |
|---|---|---|

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | IMIEA2 | IMIEA1 | IMIEA0 | — | IMFA2 | IMFA1 | IMFA0 |
| Initial value: | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Read/Write: | — | R/W | R/W | R/W | — | R/(W)* | R/(W)* | R/(W)* |

Input capture/compare match flag A0

| | |
|---|---|
| 0 | [Clearing conditions] (Initial value)<br>Read IMFA0 when IMFA0=1, then write 0 in IMFA0<br>DMAC activated by IMIA0 interrupt. |
| 1 | [Setting conditions]<br>TCNT0=GRA0 when GRA0 functions as an output compare register.<br>TCNT0 value is transferred to GRA0 by an input capture signal when GRA0 functions as an input capture register. |

Input capture/compare match flag A1

| | |
|---|---|
| 0 | [Clearing conditions] (Initial value)<br>Read IMFA1 when IMFA1=1, then write 0 in IMFA1<br>DMAC activated by IMIA1 interrupt. |
| 1 | [Setting conditions]<br>TCNT1=GRA1 when GRA1 functions as an output compare register.<br>TCNT1 value is transferred to GRA1 by an input capture signal when GRA1 functions as an input capture register. |

Input capture/compare match flag A2

| | |
|---|---|
| 0 | [Clearing conditions] (Initial value)<br>Read IMFA2 when IMFA2=1, then write 0 in IMFA2<br>DMAC activated by IMIA2 interrupt. |
| 1 | [Setting conditions]<br>TCNT2=GRA2 when GRA2 functions as an output compare register.<br>TCNT2 value is transferred to GRA2 by an input capture signal when GRA2 functions as an input capture register. |

Input capture/compare match interrupt enable A0

| | | |
|---|---|---|
| 0 | IMIA0 interrupt requested by IMFA0 flag is disabled | (Initial value) |
| 1 | IMIA0 interrupt requested by IMFA0 is enabled | |

Input capture/compare match interrupt enable A1

| | | |
|---|---|---|
| 0 | IMIA1 interrupt requested by IMFA1 flag is disabled | (Initial value) |
| 1 | IMIA1 interrupt requested by IMFA1 is enabled | |

Input capture/compare match interrupt enable A2

| | | |
|---|---|---|
| 0 | IMIA2 interrupt requested by IMFA2 flag is disabled | (Initial value) |
| 1 | IMIA2 interrupt requested by IMFA2 is enabled | |

Note: * Only 0 can be written, to clear the flag.

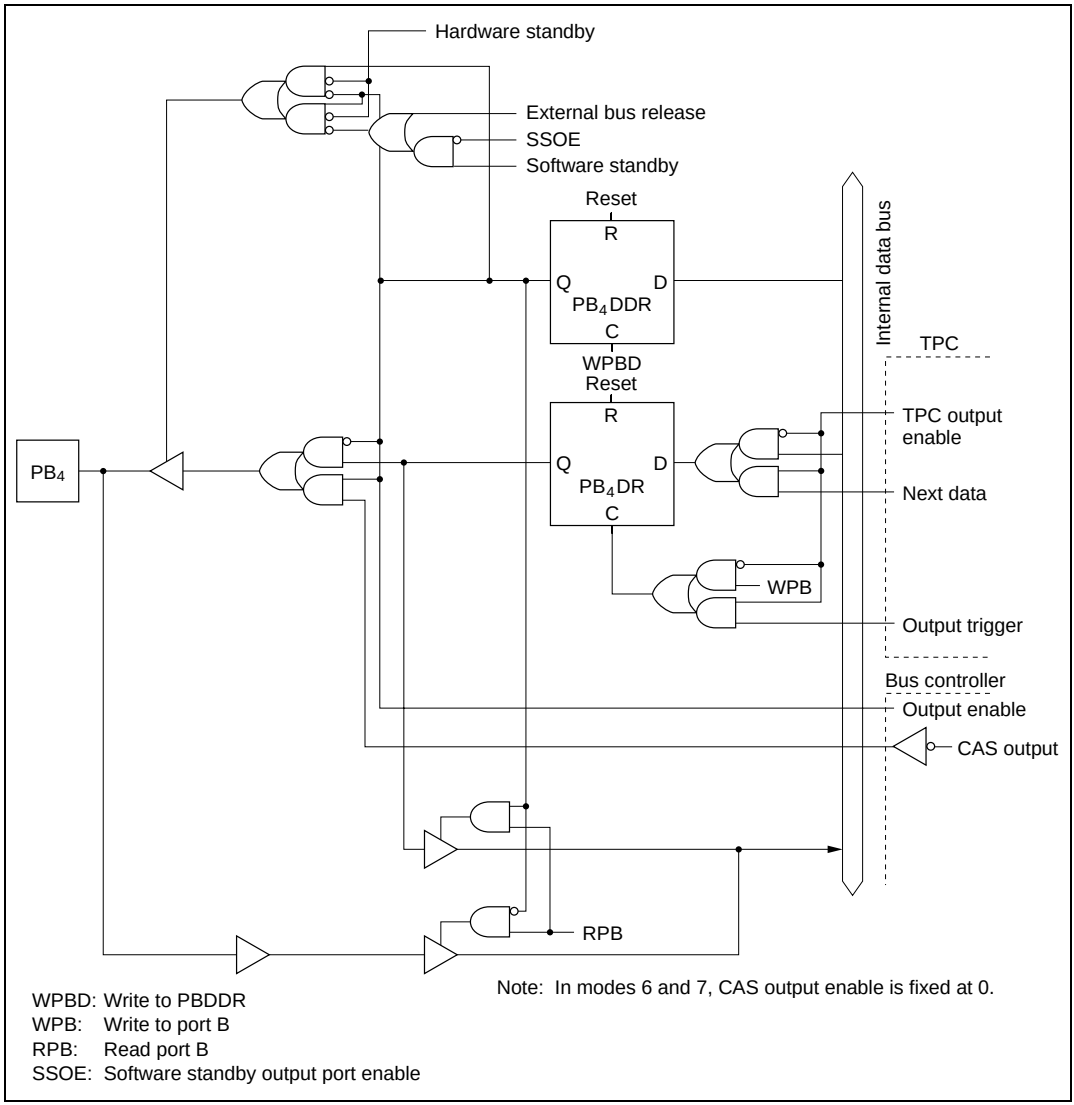
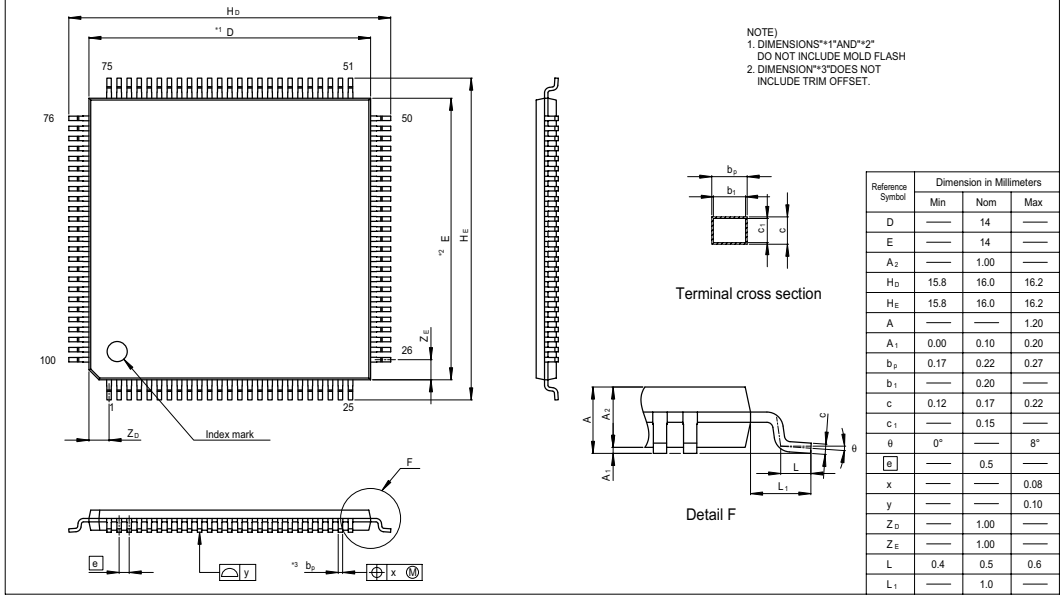



**Figure C.11 (e) Port B Block Diagram (Pin $PB_4$)**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TQFP100-14x14-0.50 | PTQP0100KA-A | TFP-100B/TFP-100BV | 0.5g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 14 | — |
| E | — | 14 | — |
| $A_2$ | — | 1.00 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.20 |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.12 | 0.17 | 0.22 |
| $c_1$ | — | 0.15 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.00 | — |
| $Z_E$ | — | 1.00 | — |
| L | 0.4 | 0.5 | 0.6 |
| $L_1$ | — | 1.0 | — |

**Figure G.2 Package Dimensions (TFP-100B)**