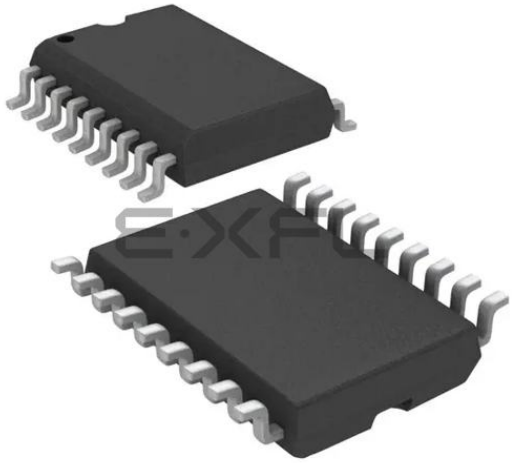

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c717-e-so

3.3 PORTB and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

EXAMPLE 3-2: Initializing PORTB

```
BCF     STATUS, RP0 ;
CLRF    PORTB       ; Initialize PORTB by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                    ; RB<5:4> as outputs
                    ; RB<7:6> as inputs
MOVLW   0x30        ; Set RB<1:0> as analog
                      inputs
MOVWF   ANSEL       ;
BCF     STATUS, RP0 ; Return to Bank 0
```

Each of the PORTB pins has an internal pull-up, which can be individually enabled from the WPUB register. A single global enable bit can turn on/off the enabled pull-ups. Clearing the $\overline{\text{RBPU}}$ bit, (OPTION_REG<7>), enables the weak pull-up resistors. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Each of the PORTB pins, if configured as input, also has an interrupt-on-change feature, which can be individually selected from the IOCB register. The RBIE bit in the INTCON register functions as a global enable bit to turn on/off the interrupt-on-change feature. The selected inputs are compared to the old value latched on the last read of PORTB. The "mismatch" outputs are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

a) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 5-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

5.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

5.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 5-2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS<2:0> bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

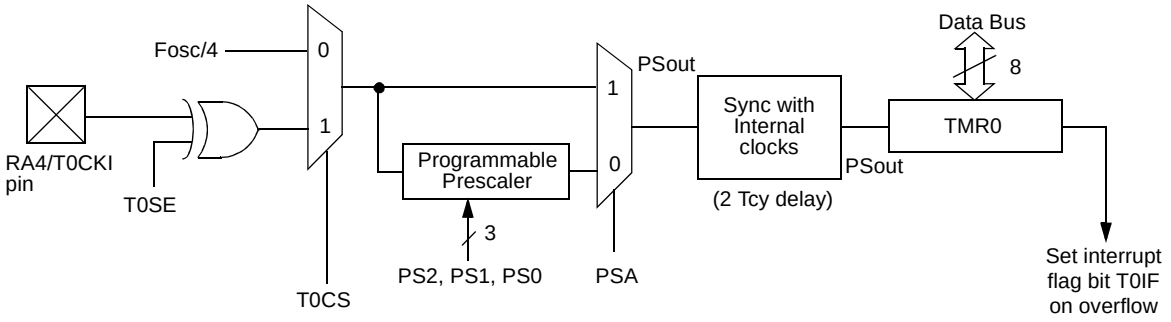
Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. `CLRF 1, MOVWF 1, BSF 1, x....etc`.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT.

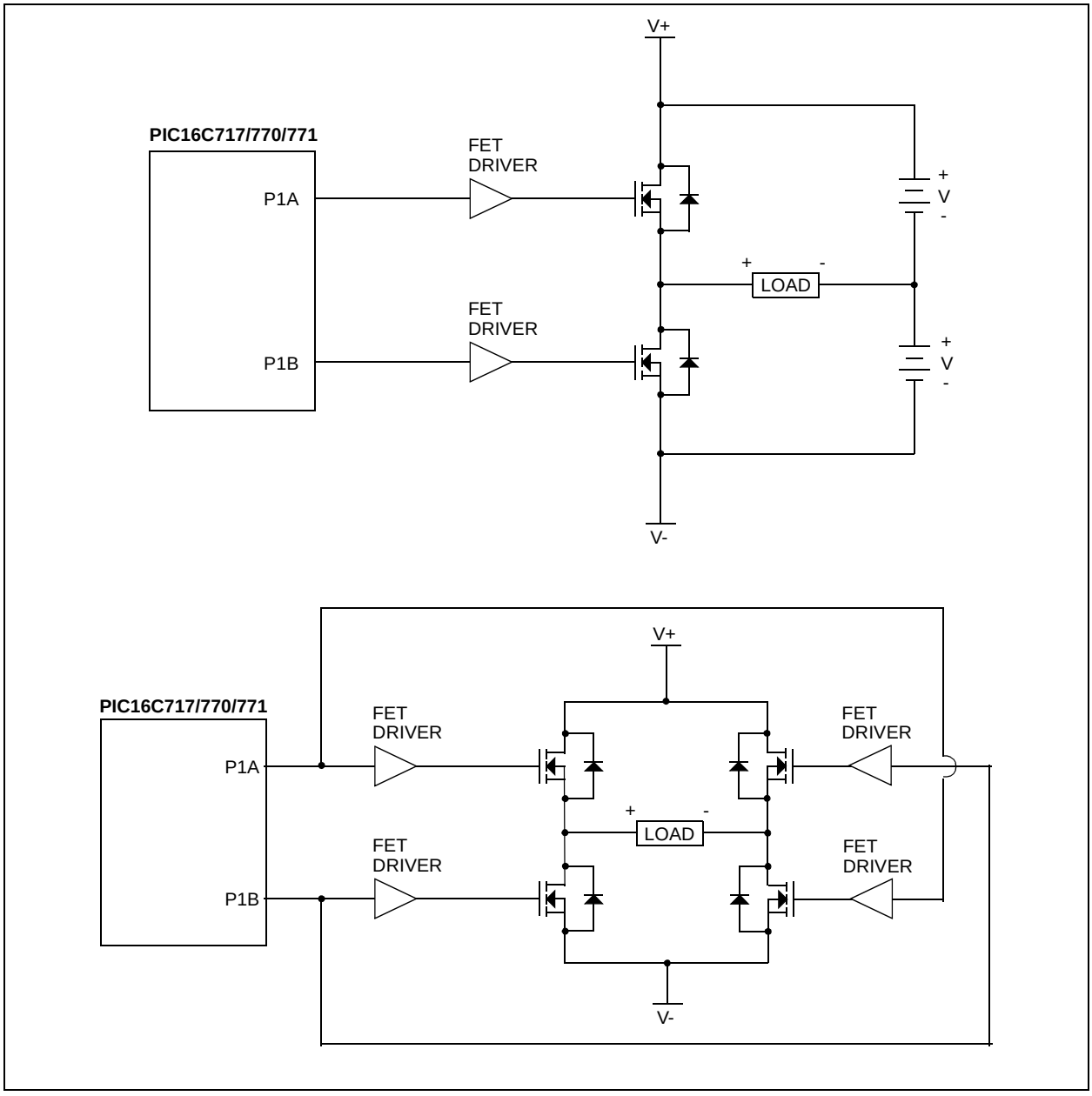
Note:	Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 5-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS<2:0> (OPTION_REG<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 5-2 for detailed block diagram).

FIGURE 8-7: EXAMPLE OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit, BF (SSPSTAT<0>), indicates when the SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the MSSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 9-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

EXAMPLE 9-1: Loading the SSPBUF (SSPSR) Register

```
      BSF   STATUS, RP0    ;Specify Bank 1
LOOP  BTFSS SSPSTAT, BF    ;Has data been
                           ;received
                           ;(xmit complete)?
      GOTO  LOOP           ;No
      BCF   STATUS, RP0    ;Specify Bank 0
      MOVF  SSPBUF, W      ;Save SSPBUF...
      MOVWF RXDATA         ;...in user RAM
      MOVF  TXDATA, W      ;Get next TXDATA
      MOVWF SSPBUF         ;New data to xmit
```

The SSPSR is not directly readable or writable, and can only be accessed by addressing the SSPBUF register. Additionally, the MSSP STATUS register (SSPSTAT) indicates the various status conditions.

9.1.2 ENABLING SPI I/O

To enable the serial port, MSSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON registers, and then set bit SSPEN. This configures the SDI, SDO, SCK and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- SDI is automatically controlled by the SPI module
- SDO must have TRISB<5> cleared
- SCK (Master mode) must have TRISB<2> cleared
- SCK (Slave mode) must have TRISB<2> set
- $\overline{SS}$ must have TRISB<1> set, and ANSEL<5> cleared

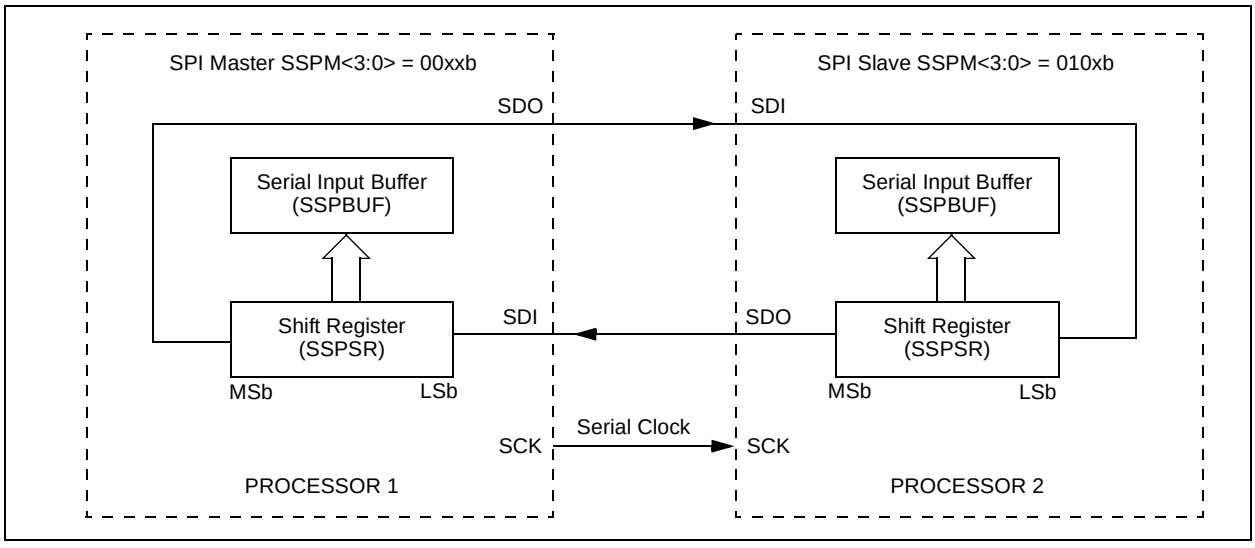
Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

9.1.3 TYPICAL CONNECTION

Figure 9-2 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (SSPCON<4>), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

FIGURE 9-2: SPI MASTER/SLAVE CONNECTION



9.2.14 ACKNOWLEDGE SEQUENCE TIMING

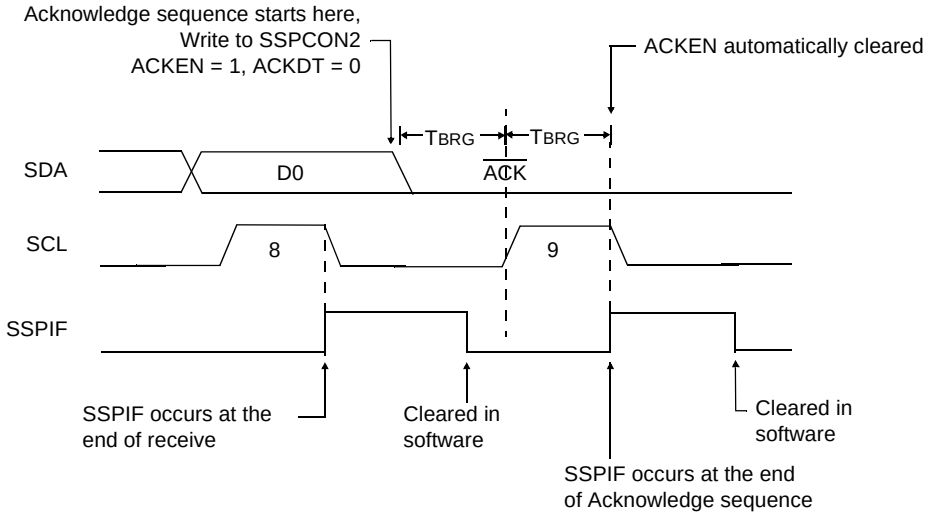
An Acknowledge sequence is enabled by setting the Acknowledge sequence enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit ACKDT (SSPCON2<5>) is presented on the SDA pin. If the user wishes to generate an Acknowledge (ACK), then the ACKDT bit should be cleared. Otherwise, the user should set the ACKDT bit (NACK) before starting an Acknowledge sequence. The baud rate generator is then loaded from SSPADD<6:0> and counts for one rollover period (TBRG). The SCL pin is then de-asserted (pulled high). When the SCL pin is sampled high (clock arbitration), the baud rate generator is reloaded and counts for another TBRG. At the completion of the TBRG period, the following events occur (see Figure 9-20):

- The SCL pin is pulled low.
- The ACKEN bit is automatically cleared.
- The baud rate generator is turned off.
- The MSSP module goes into IDLE mode.

9.2.14.1 WCOL STATUS FLAG

If the user writes the SSPBUF when an Acknowledge sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 9-20: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one baud rate generator period.

10.1 Bandgap Voltage Reference

The bandgap module generates a stable voltage reference of over a range of temperatures and device supply voltages. This module is enabled anytime any of the following are enabled:

- Brown-out Reset
- Low-voltage Detect
- Either of the internal analog references (VRH, VRL)

Whenever the above are all disabled, the bandgap module is disabled and draws no current.

10.2 Internal VREF for A/D Converter

The bandgap output voltage is used to generate two stable references for the A/D converter module. These references are enabled in software to provide the user with the means to turn them on and off in order to minimize current consumption. Each reference can be individually enabled.

The VRH reference is enabled with control bit VRHEN (REFCON<7>). When this bit is set, the gain amplifier is enabled. After a specified start-up time a stable reference of 4.096V nominal is generated and can be used by the A/D converter as a reference input.

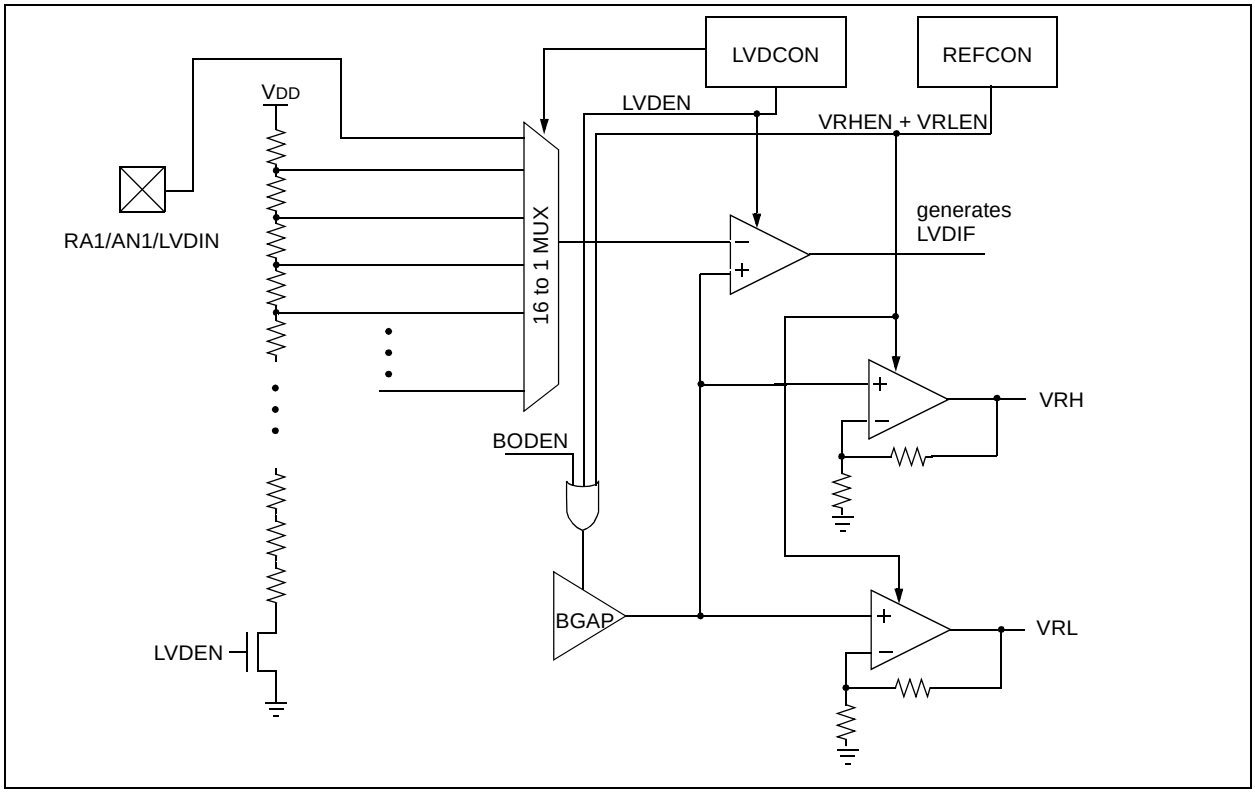
The VRL reference is enabled by setting control bit VRLEN (REFCON<6>). When this bit is set, the gain amplifier is enabled. After a specified start-up time a stable reference of 2.048V nominal is generated and can be used by the A/D converter as a reference input.

Each voltage reference is available for external use via VRL and VRH pins.

Each reference, if enabled, can be output on an external pin by setting the VRHOEN (high reference output enable) or VRLOEN (low reference output enable) control bit. If the reference is not enabled, the VRHOEN and VRLOEN bits will have no effect on the corresponding pin. The device specific pin can then be used as general purpose I/O.

Note:	If VRH or VRL is enabled and the other reference (VRL or VRH), the BOR, and the LVD modules are not enabled, the bandgap will require a start-up time before the bandgap reference is stable. Before using the internal VRH or VRL reference, ensure that the bandgap reference voltage is stable by monitoring the BGST bit in the LVDCON register. The voltage references will not be reliable until the bandgap is stable as shown by BGST being set.

FIGURE 10-1: BLOCK DIAGRAM OF LVD AND VOLTAGE REFERENCE CIRCUIT



REGISTER 11-2: A/D CONTROL REGISTER 1 (ADCON1: 9Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG2	VCFG1	VCFG0	Reserved	Reserved	Reserved	Reserved
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6-4 **VCFG<2:0>:** Voltage Reference Configuration bits

	A/D V_{REF+}	A/D V_{REF-}
000	AV_{DD}(1)	AV_{SS}(2)
001	External V_{REF+}	External V_{REF-}
010	Internal VRH	Internal VRL
011	External V_{REF+}	AV_{SS}(2)
100	Internal VRH	AV_{SS}(2)
101	AV_{DD}(1)	External V_{REF-}
110	AV_{DD}(1)	Internal VRL
111	Internal VRL	AV_{SS}

bit 3-0 **Reserved:** Do not use.

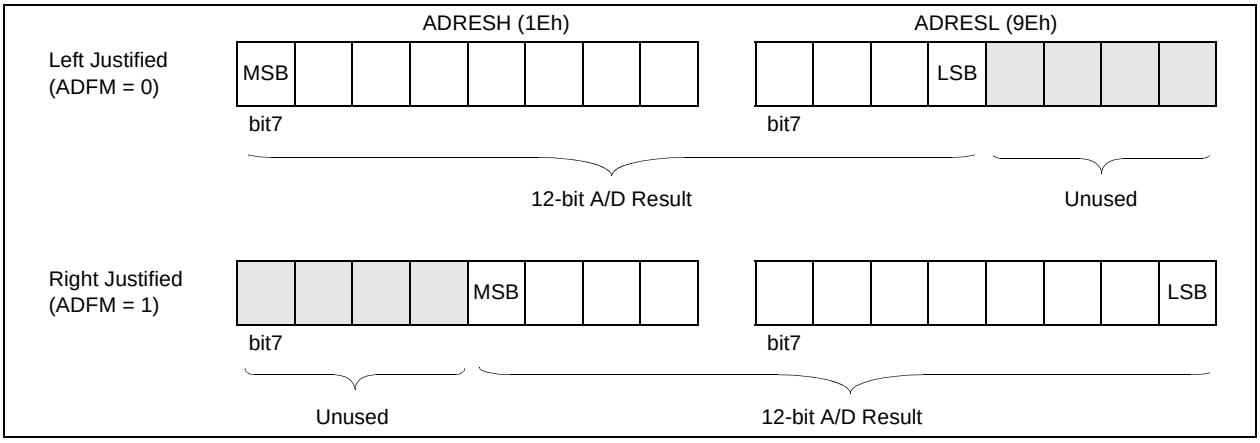
Note 1: This parameter is V_{DD} for the PIC16C717.
2: This parameter is V_{SS} for the PIC16C717.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The value that is in the ADRESH and ADRESL registers are not modified for a Power-on Reset. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

The A/D conversion results can be left justified (ADFM bit cleared), or right justified (ADFM bit set). Figure 11-1 through Figure 11-2 show the A/D result data format of the PIC16C717/770/771.

FIGURE 11-1: PIC16C770/771 12-BIT A/D RESULT FORMATS



11.4 A/D Conversions

Example 11-1 shows an example that performs an A/D conversion. The port pins are configured as analog inputs. The analog reference V_{REF+} is the device AV_{DD} and the analog reference V_{REF-} is the device AV_{SS}. The A/D interrupt is enabled and the A/D conversion clock is T_{RC}. The conversion is performed on the AN0 channel.

EXAMPLE 11-1: PERFORMING AN A/D CONVERSION

```
    BSF     STATUS, RP0    ;Select Bank 1
    CLRF    ADCON1         ;Configure A/D Voltage Reference
    MOVLW   0x01
    MOVWF   ANSEL          ;disable AN0 digital input buffer
    MOVWF   TRISA          ;RA0 is input mode
    BSF     PIE1, ADIE     ;Enable A/D interrupt
    BCF     STATUS, RP0    ;Select Bank 0
    MOVLW   0xC1           ;RC clock, A/D is on,
                           ;Ch 0 is selected
    MOVWF   ADCON0         ;
    BCF     PIR1, ADIF     ;Clear A/D Int Flag
    BSF     INTCON, PEIE   ;Enable Peripheral
    BSF     INTCON, GIE    ;Enable All Interrupts
;
; Ensure that the required sampling time for the
; selected input channel has lapsed. Then the
; conversion may be started.
    BSF     ADCON0, GO     ;Start A/D Conversion
            :              ;The ADIF bit will be
                           ;set and the GO/DONE bit
            :              ;cleared upon completion-
                           ;of the A/D conversion.
; Wait for A/D completion and read ADRESH:ADRESL for result.
```

11.6 A/D Sample Requirements

11.6.1 RECOMMENDED SOURCE IMPEDANCE

The maximum recommended impedance for analog sources is 2.5 kΩ. This value is calculated based on the maximum leakage current of the input pin. The leakage current is 100 nA max., and the analog input voltage cannot be varied by more than 1/4 LSb or 250 μV due to leakage. This places a requirement on the input impedance of 250 μV/100 nA = 2.5 kΩ.

11.6.2 SAMPLING TIME CALCULATION

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-5. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 11-5. **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed) this sampling must be done before the conversion can be started.

To calculate the minimum sampling time, Equation 11-2 may be used. This equation assumes that 1/4 LSb error is used (16384 steps for the A/D). The 1/4 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

The CHOLD is assumed to be 25 pF for the 12-bit A/D.

EXAMPLE 11-2: A/D SAMPLING TIME EQUATION

$$V_{HOLD} = V_{REF} - \frac{V_{REF}}{16384}$$

$$V_{REF} - \frac{V_{REF}}{16384} = (V_{REF})\left(1 - e^{\left(\frac{-T_C}{C_{HOLD}(R_{IC} + R_{SS} + R_S)}\right)}\right)$$

$$V_{REF}\left(1 - \frac{1}{16384}\right) = (V_{REF})\left(1 - e^{\left(\frac{-T_C}{C_{HOLD}(R_{IC} + R_{SS} + R_S)}\right)}\right)$$

Solving for TC:

$$T_C = -C_{HOLD}(1k + R_{SS} + R_S)\ln\left(\frac{1}{16384}\right)$$

Figure 11-3 shows the calculation of the minimum time required to charge CHOLD. This calculation is based on the following system assumptions:

CHOLD = 25 pF

RS = 2.5 kΩ

1/4 LSb error

VDD = 5V → RSS = 10 kΩ (worst case)

Temp (system Max.) = 50°C

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (**CHOLD**) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 2.5 kΩ. This is required to meet the pin leakage specification.

TABLE 12-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Power-on Reset or Brown-out Reset	$\overline{\text{MCLR}}$ Reset or WDT Reset	Wake-up via WDT or Interrupt
P1DEL	0000 0000	0000 0000	uuuu uuuu
REFCON	0000 ----	0000 ----	uuuu ----
LVDCON	--00 0101	--00 0101	--uu uuuu
ANSEL	--11 1111	--11 1111	--uu uuuu
ADRESL	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	0000 0000	0000 0000	uuuu uuuu
PMDATL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMADRL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMDATH	--xx xxxx	--uu uuuu	--uu uuuu
PMADRH	---- xxxx	---- uuuu	---- uuuu
PMCON1	1--- ---0	1--- ---0	1--- ---0

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

2: See Table 12-5 for RESET value for specific condition.

FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})

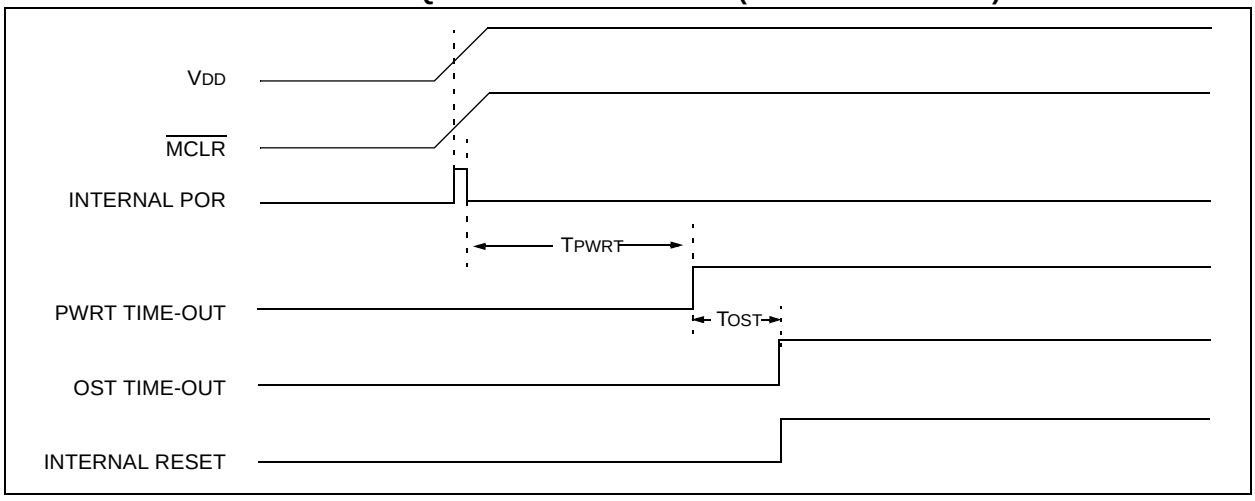
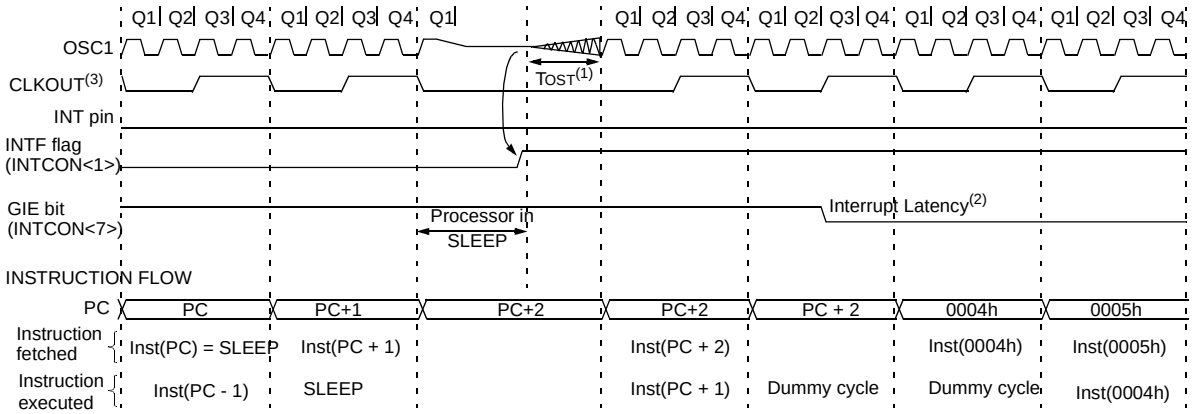


FIGURE 12-12: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: TOST = 1024TOSC (drawing not to scale) This delay applies to LP, XT and HS modes only.
2: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
3: CLKOUT is not available in these osc modes, but shown here for timing reference.

12.14 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices. Code protected devices are not reprogrammable.

12.15 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 Least Significant bits of the ID location are used.

12.16 In-Circuit Serial Programming (ICSP™)

PIC16CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For complete details of serial programming, please refer to the In-Circuit Serial Programming (ICSP™) Guide, (DS30277).

RETFIE **Return from Interrupt**

Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

RETLW **Return with Literal in W**

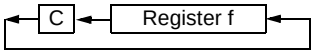
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RETURN **Return from Subroutine**

Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

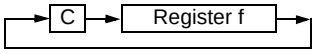
RLF **Rotate Left f through Carry**

Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



RRF **Rotate Right f through Carry**

Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



SLEEP

Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 12.8 for more details.

NOTES:

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PIC16LC717/770/771			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16C717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IPD	**Power-down Current(3)**					
D020D		**PIC16LC7XX**		0.3	2.0	µA	VDD = 3V, -40°C to 85°C
D020E					5.0		VDD = 3V, -40°C to 125°C
D020F				0.1	1.5	µA	VDD = 2.5V, -40°C to 85°C
D020G					3.0		VDD = 2.5V, -40°C to 125°C
D020		**PIC16C7XX**		1.4	4.0	µA	VDD = 5.5V, -40°C to 85°C
D020A					8.0		VDD = 5.5V, -40°C to 125°C
D020B				1.0	3.5	µA	VDD = 4V, -40°C to 85°C
D020C					6.0		VDD = 4V, -40°C to 125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active Operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

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FIGURE 15-6: EXTERNAL CLOCK TIMING

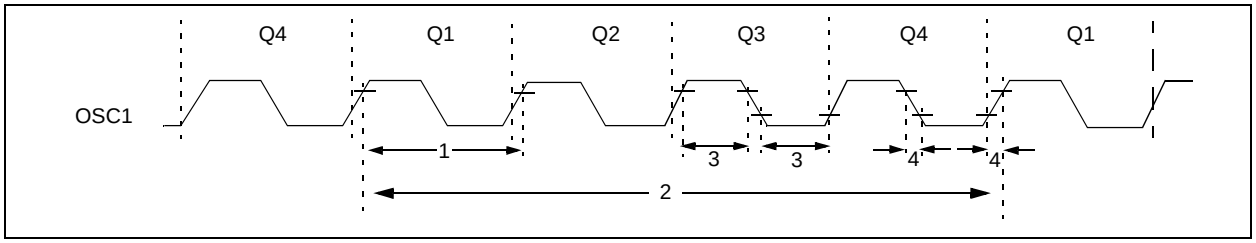

TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency **(Note 1)**	DC	—	4	MHz	XT mode
			DC	—	20	MHz	EC mode
			DC	—	20	MHz	HS mode
			DC	—	200	kHz	LP mode
		Oscillator Frequency **(Note 1)**	0.1*	—	4	MHz	XT mode
			4*	—	20	MHz	HS mode
			5*	—	200	kHz	LP mode
1	TOSC	External CLKIN Period **(Note 1)**	250	—	—	ns	XT mode
			50	—	—	ns	EC mode
			50	—	—	ns	HS mode
			5	—	—	µs	LP mode
		Oscillator Period **(Note 1)**	250	—	10,000*	ns	XT mode
			50	—	250*	ns	HS mode
			5	—	—	µs	LP mode
2	TCY	Instruction Cycle Time **(Note 1)**	200	TCY	DC	ns	TCY = 4/FOSC
3*	TosL, TosH	External Clock in (OSC1) High or Low Time	100	—	—	ns	XT mode
			2.5	—	—	µs	LP mode
			15	—	—	ns	HS mode
							EC mode
4*	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT mode
			—	—	50	ns	LP mode
			—	—	15	ns	HS mode
							EC mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Max. Frequency" values with a square wave applied to the OSC1/CLKIN pin.

When an external clock input is used, the "Min." frequency (or Max. TCY) limit is "DC" (no clock) for all devices.

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15.4.2 LOW VOLTAGE DETECT MODULE (LVD)

FIGURE 15-13: LOW VOLTAGE DETECT CHARACTERISTICS

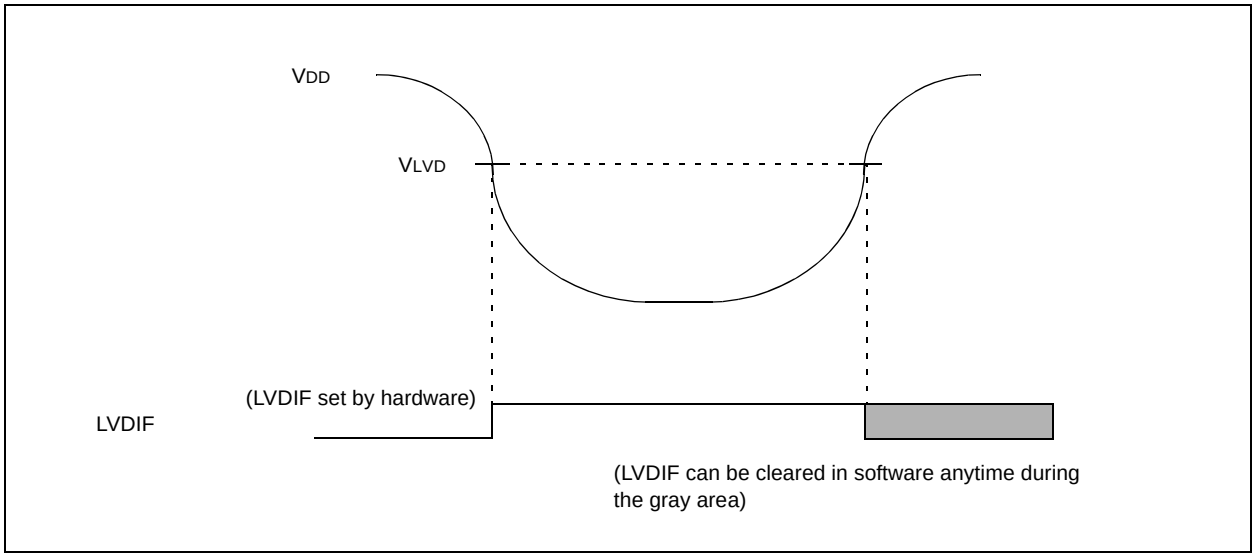

TABLE 15-8: ELECTRICAL CHARACTERISTICS: LVD

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC Characteristics Section 15.1.					
Param. No.	**Characteristic**		**Symbol**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420*	LVD Voltage	LVV = 0100	VLVD	2.5	2.58	2.66	V	
		LVV = 0101		2.7	2.78	2.86	V	
		LVV = 0110		2.8	2.89	2.98	V	
		LVV = 0111		3.0	3.1	3.2	V	
		LVV = 1000		3.3	3.41	3.52	V	
		LVV = 1001		3.5	3.61	3.72	V	
		LVV = 1010		3.6	3.72	3.84	V	
		LVV = 1011		3.8	3.92	4.04	V	
		LVV = 1100		4.0	4.13	4.26	V	
		LVV = 1101		4.2	4.33	4.46	V	
		LVV = 1110		4.5	4.64	4.78	V	

* These parameters are characterized but not tested.

Note 1: Production tested at Tamb = 25°C. Specifications over temperature limits ensured by characterization.

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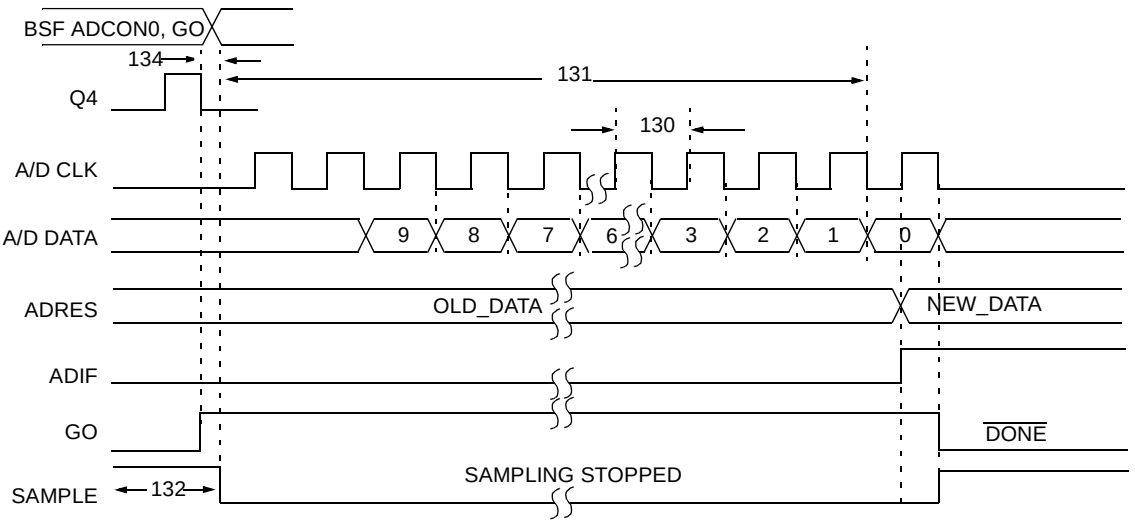
FIGURE 15-17: PIC16C717 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-16: PIC16C717 AND PIC16LC717 A/D CONVERSION REQUIREMENT (SLEEP MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	3.0	6.0	9.0	µs	ADCS<1:0> = 11 (A/D RC mode) At VDD = 3.0V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	11TAD	—	—	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2 + TCY	—	—	If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

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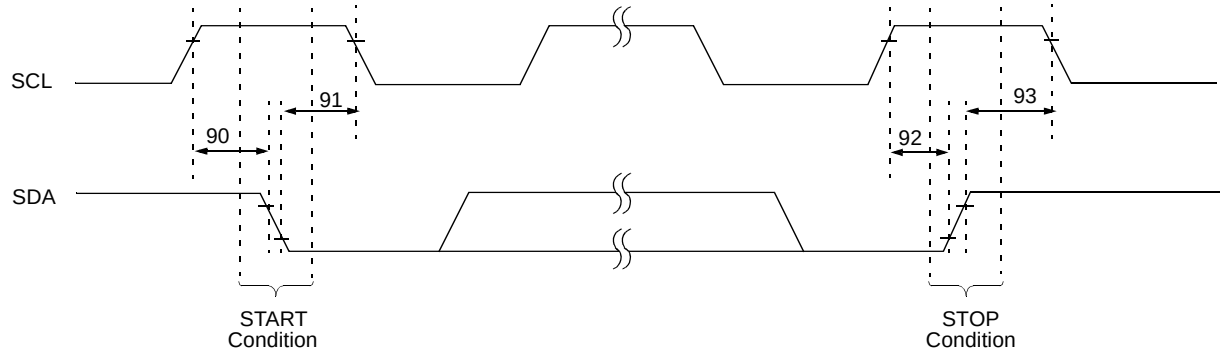
15.6 Master SSP I²C Mode Timing Waveforms and Requirements

FIGURE 15-22: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS



Note: Refer to Figure 15-4 for load conditions.

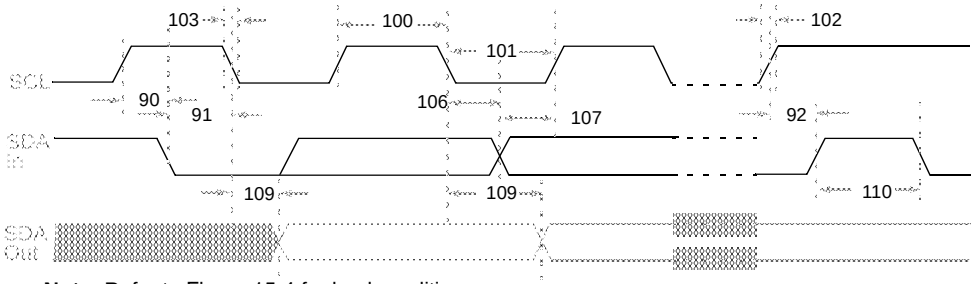
TABLE 15-21: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	Only relevant for a Repeated START condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
93*	THD:STO	STOP condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		

* These parameters are characterized but not tested. For the value required by the I²C specification, please refer to the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

Maximum pin capacitance = 10 pF for all I²C pins.

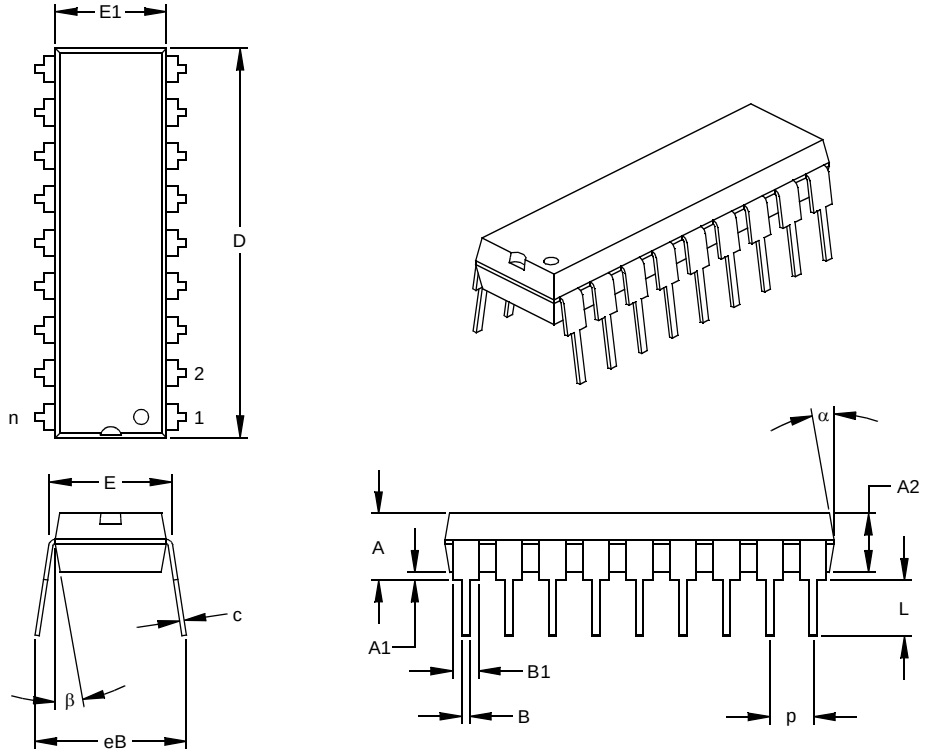
FIGURE 15-23: MASTER SSP I²C BUS DATA TIMING



Note: Refer to Figure 15-4 for load conditions.

17.2 18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

17.6 20-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

DRAWING NOT AVAILABLE