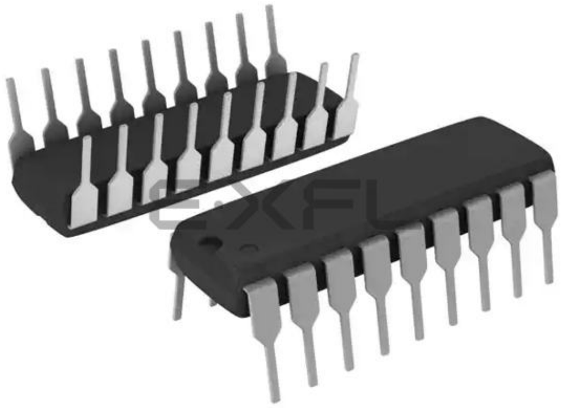

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c717-p

FIGURE 3-8: BLOCK DIAGRAM OF RB2/SCK/SCL, RB3/CCP1/P1A, RB4/SDI/SDA, RB5/SDO/P1B

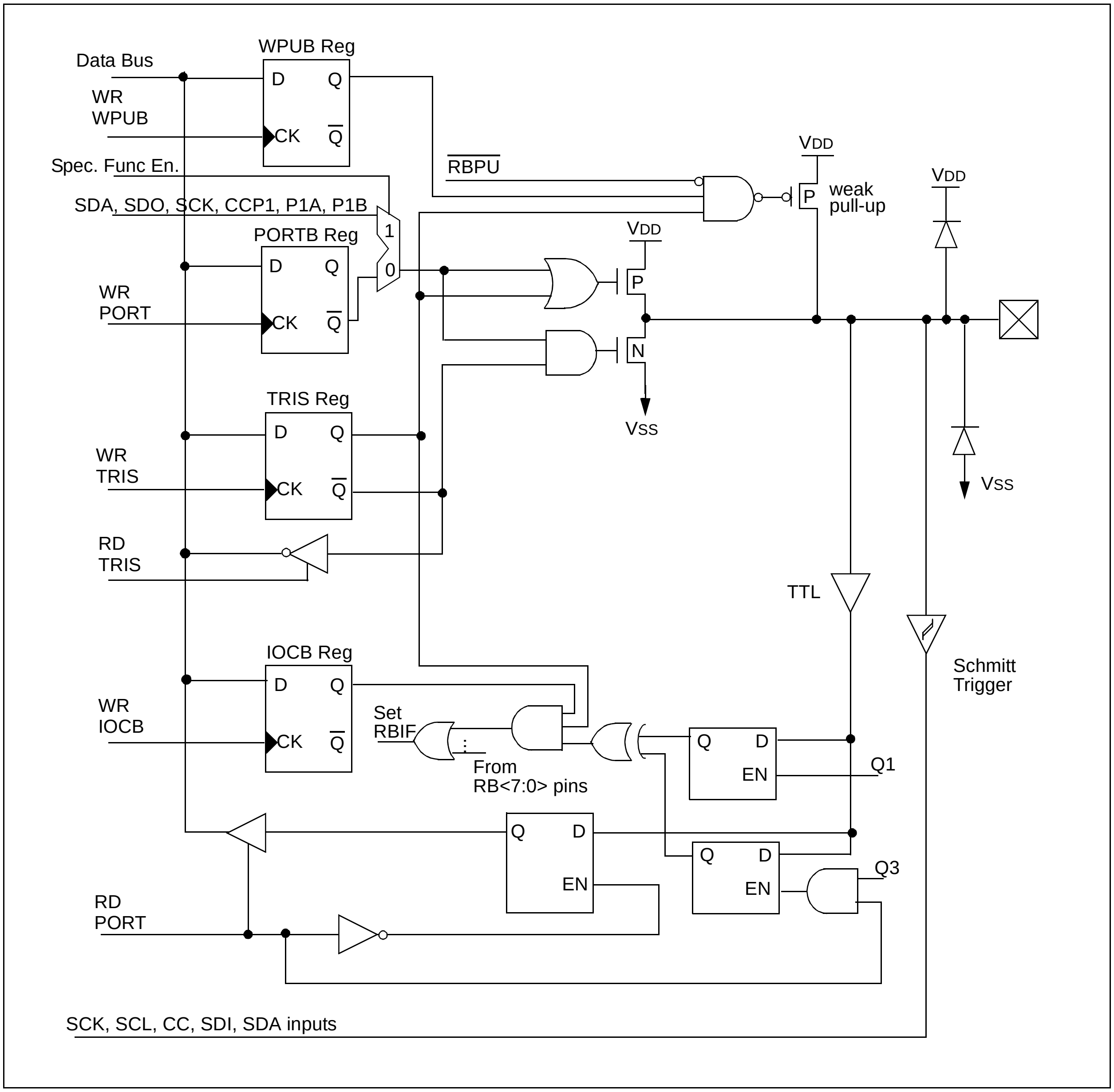


TABLE 4-1: PROGRAM MEMORY READ REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--xx xxxx	--uu uuuu
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	xxxx xxxx	uuuu uuuu
10Fh	PMADRH	—	—	—	—	PMA11	PMA10	PMA9	PMA8	---- xxxx	---- uuuu
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Program Memory Read.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

PWM duty cycle = (CCPR1L:CCP1CON<5:4>) • TOSC • (TMR2 prescale value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

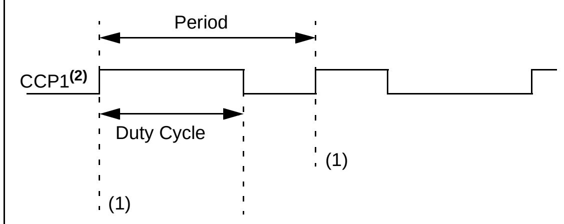
8.3.3 PWM OUTPUT CONFIGURATIONS

The PWM1M1 bits in the CCP1CON register allows one of the following configurations:

- Single output
- Half-Bridge output
- Full-Bridge output, Forward mode
- Full-Bridge output, Reverse mode

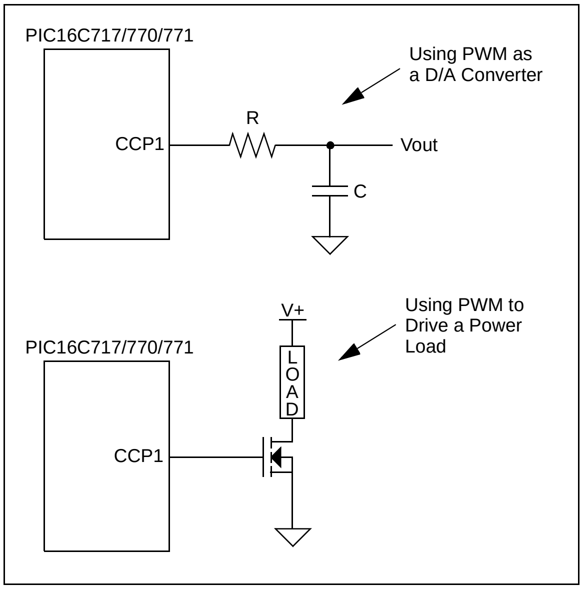
In the Single Output mode, the RB3/CCP1/P1A pin is used as the PWM output. Since the CCP1 output is multiplexed with the PORTB<3> data latch, the TRISB<3> bit must be cleared to make the CCP1 pin an output.

FIGURE 8-4: SINGLE PWM OUTPUT



Note 1: At this time, the TMR2 register is equal to the PR2 register.
2: Output signal is shown as asserted high.

FIGURE 8-5: EXAMPLE OF SINGLE OUTPUT APPLICATION



In the Half-Bridge Output mode, two pins are used as outputs. The RB3/CCP1/P1A pin has the PWM output signal, while the RB5/SDO/P1B pin has the complementary PWM output signal. This mode can be used for half-bridge applications, as shown on Figure 8-7, or for full-bridge applications, where four power switches are being modulated with two PWM signal.

Since the P1A and P1B outputs are multiplexed with the PORTB<3> and PORTB<5> data latches, the TRISB<3> and TRISB<5> bits must be cleared to configure P1A and P1B as outputs.

In Half-Bridge Output mode, the programmable deadband delay can be used to prevent shoot-through current in bridge power devices. See Section 8.3.5 for more details of the deadband delay operations.

9.2.2.3 SLAVE RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear (SSPSR<0> = 0) and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register on the falling edge of the eighth SCL pulse.

When the address byte overflow condition exists, then no Acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) or bit SSPOV (SSPCON<6>) is set.

An MSSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the received byte.

> **Note:** The SSPBUF will be loaded if the SSPOV bit is set and the BF flag is cleared. If a read of the SSPBUF was performed, but the user did not clear the state of the SSPOV bit before the next receive occurred, the $\overline{ACK}$ is not sent and the SSPBUF is updated.

TABLE 9-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		SSPSR → SSPBUF	Generate $\overline{ACK}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if enabled)
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	Yes	No	Yes

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

FIGURE 9-8: I^{2}C SLAVE MODE WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

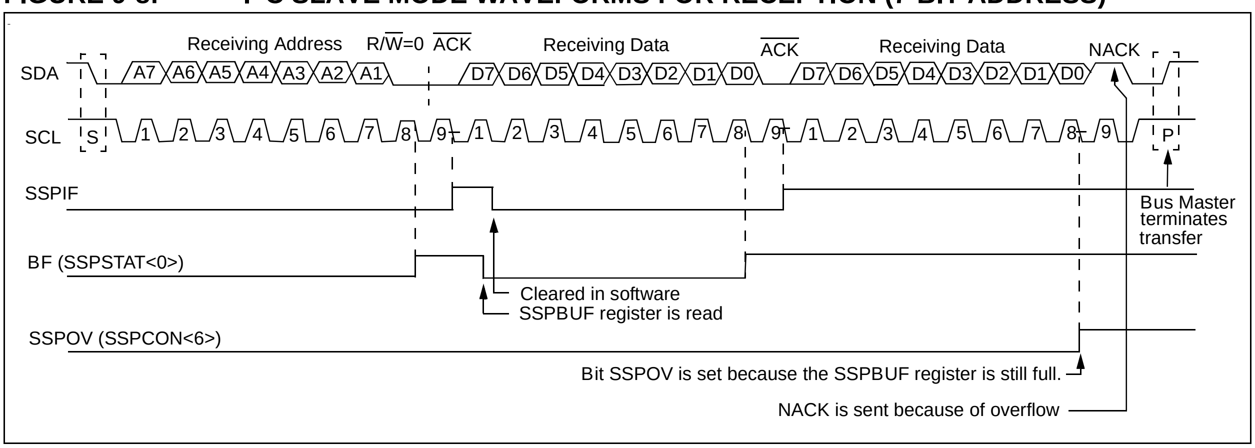
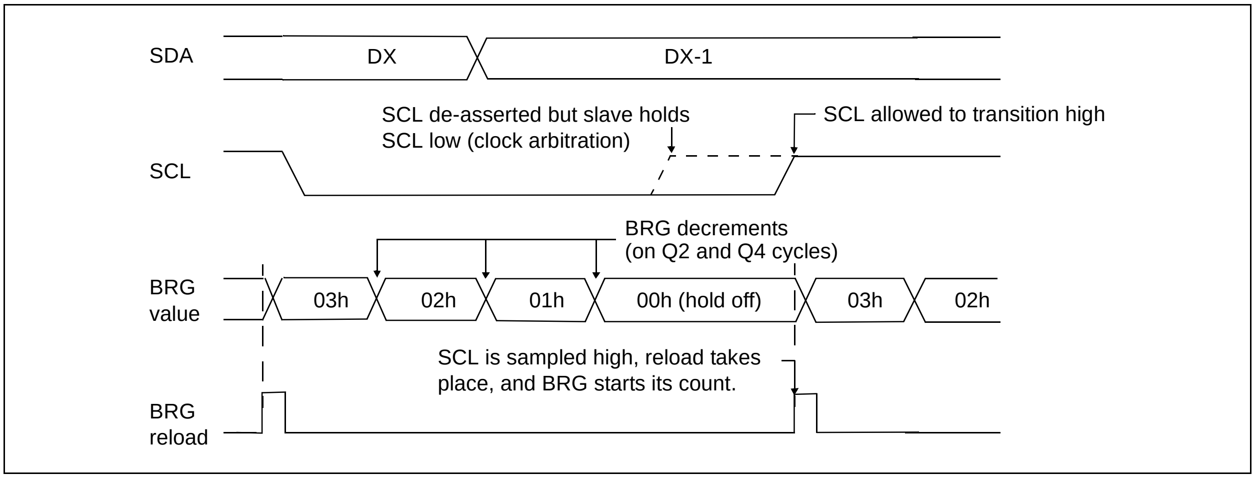


FIGURE 9-15: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



9.2.10 I²C MASTER MODE START CONDITION TIMING

To initiate a START condition, the user sets the START condition enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, indicating that the bus is available, the baud rate generator is loaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the baud rate generator times out (TBRG) indicating the bus is still available, the SDA pin is driven low. The SDA transition from high to low while SCL is high is the START condition. This causes the S bit (SSPSTAT<3>) to be set. When the S bit is set, the baud rate generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the baud rate generator times out (TBRG) the START condition is complete, concurrent with the following events:

- The SEN bit (SSPCON2<0>) is automatically cleared by hardware,
- The baud rate generator is suspended leaving the SDA line held low.
- The SSPIF flag is set.

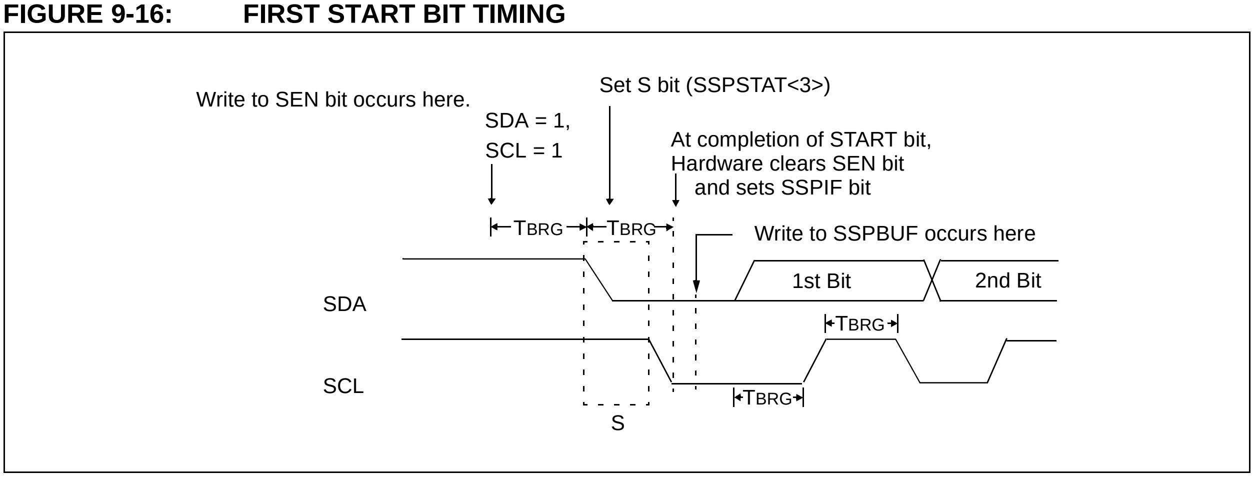
Note:	If at the beginning of START condition, the SDA and SCL pins are already sampled low, or if during the START condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs. Thus, the Bus Collision Interrupt Flag (BCLIF) is set, the START condition is aborted, and the I²C module is RESET into its IDLE state.

9.2.10.1 WCOL STATUS FLAG

If the user writes the SSPBUF when a START sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note:	Because queueing of events is not allowed, writing to the lower five bits of SSPCON2 is disabled until the START condition is complete.

FIGURE 9-16: FIRST START BIT TIMING



9.2.11 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated START condition occurs when the RSEN bit (SSPCON2<1>) is set high while the I²C module is in the idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the baud rate generator is loaded with the contents of SSPADD<6:0> and begins counting. The SDA pin is released (brought high) for one baud rate generator count (TBRG). When the baud rate generator times out, if SDA is sampled high, the SCL pin will be de-asserted (brought high). When SCL is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG period. This action is then followed by assertion of the SDA pin (SDA is low) for one TBRG period while SCL is high. As soon as a START condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. Following this, the baud rate generator is reloaded with the contents of SSPAD<6:0> and begins counting. When the BRG times out a third time, the RSEN bit in the SSPCON2 register is automatically cleared and SCL is pulled low. The SSPIF flag is set, which indicates the Restart sequence is complete.

Note 1:	If RSEN is set while another event is in progress, it will not take effect. Queuing of events is not allowed.
2:	A bus collision during the Repeated START condition occurs if either of the following is true: a) SDA is sampled low when SCL goes from low to high. b) SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

Immediately following the SSPIF bit transition to true, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an $\overline{ACK}$ is received, the user may then perform one of the following:

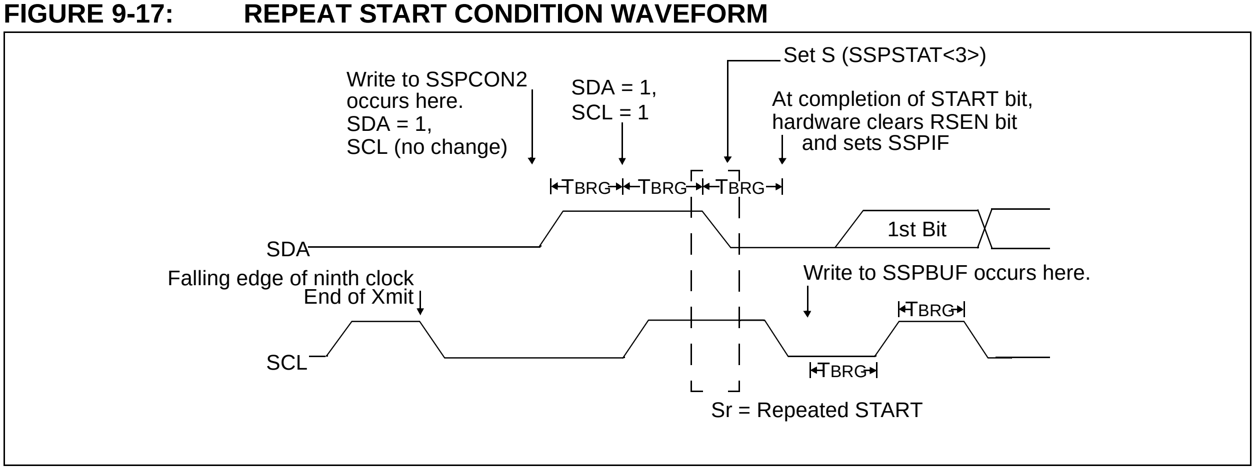
- Transmit an additional eight bits of address (if the user transmitted the first half of a 10-bit address with R/$\overline{W}$ = 0),
- Transmit eight bits of data (if the user transmitted a 7-bit address with R/$\overline{W}$ = 0), or
- Receive eight bits of data (if the user transmitted either the first half of a 10-bit address or a 7-bit address with R/$\overline{W}$ = 1).

9.2.11.1 WCOL STATUS FLAG

If the user writes the SSPBUF when a Repeated START sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note:	Because queueing of events is not allowed, writing of the lower five bits of SSPCON2 is disabled until the Repeated START condition is complete.

FIGURE 9-17: REPEAT START CONDITION WAVEFORM



11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has six inputs for the PIC16C717/770/771.

The PIC16C717 analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 10-bit digital value, while the A/D converter in the PIC16C770/771 allows conversion to a corresponding 12-bit digital value. The A/D module has up to 6 analog inputs, which are multiplexed into one sample and hold. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltages are software selectable to either the device's analog positive and negative supply voltages (AV_{DD}/AV_{SS}), the voltage level on the V_{REF+} and V_{REF-} pins, or internal voltage references if enabled (VRH, VRL).

The A/D converter can be triggered by setting the GO/$\overline{\text{DONE}}$ bit, or by the special event Compare mode of the ECCP module. When conversion is complete, the GO/$\overline{\text{DONE}}$ bit returns to '0', the ADIF bit in the PIR1 register is set, and an A/D interrupt will occur, if enabled.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result Register Low ADRESL
- A/D Result Register High ADRESH
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off and any conversion is aborted.

11.1 Control Registers

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins, the voltage reference configuration and the result format. The ANSEL register, shown in Register 3-1, selects between the Analog or Digital Port Pin modes. The port pins can be configured as analog inputs or as digital I/O.

The combination of the ADRESH and ADRESL registers contain the result of the A/D conversion. The register pair is referred to as the ADRES register. When the A/D conversion is complete, the result is loaded into ADRES, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared, and the A/D interrupt flag ADIF is set. The block diagram of the A/D module is shown in Figure 11-3.

REGISTER 11-2: A/D CONTROL REGISTER 1 (ADCON1: 9Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG2	VCFG1	VCFG0	Reserved	Reserved	Reserved	Reserved
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
`1` = Right justified
`0` = Left justified

bit 6-4 **VCFG<2:0>:** Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
000	AVDD(1)	AVSS(2)
001	External VREF+	External VREF-
010	Internal VRH	Internal VRL
011	External VREF+	AVSS(2)
100	Internal VRH	AVSS(2)
101	AVDD(1)	External VREF-
110	AVDD(1)	Internal VRL
111	Internal VRL	AVSS

bit 3-0 **Reserved:** Do not use.

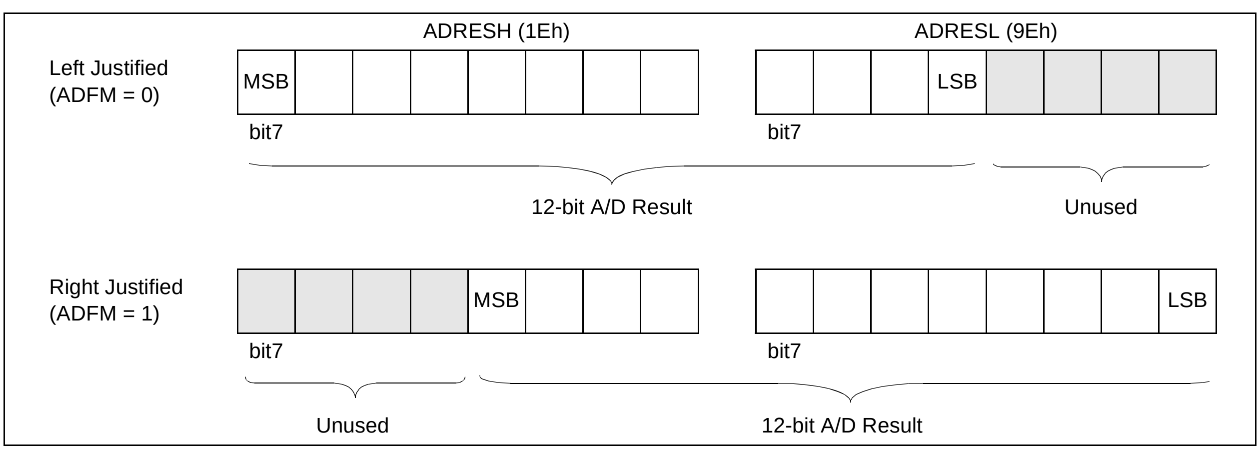
Note 1: This parameter is VDD for the PIC16C717.
2: This parameter is VSS for the PIC16C717.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

The value that is in the ADRESH and ADRESL registers are not modified for a Power-on Reset. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

The A/D conversion results can be left justified (ADFM bit cleared), or right justified (ADFM bit set). Figure 11-1 through Figure 11-2 show the A/D result data format of the PIC16C717/770/771.

FIGURE 11-1: PIC16C770/771 12-BIT A/D RESULT FORMATS



After the A/D module has been configured as desired and the analog input channels have their corresponding TRIS bits selected for port inputs, the selected channel must be acquired before conversion is started. The A/D conversion cycle can be initiated by setting the GO/$\overline{\text{DONE}}$ bit. The A/D conversion begins and lasts for $13T_{AD}$. The following steps should be followed for performing an A/D conversion:

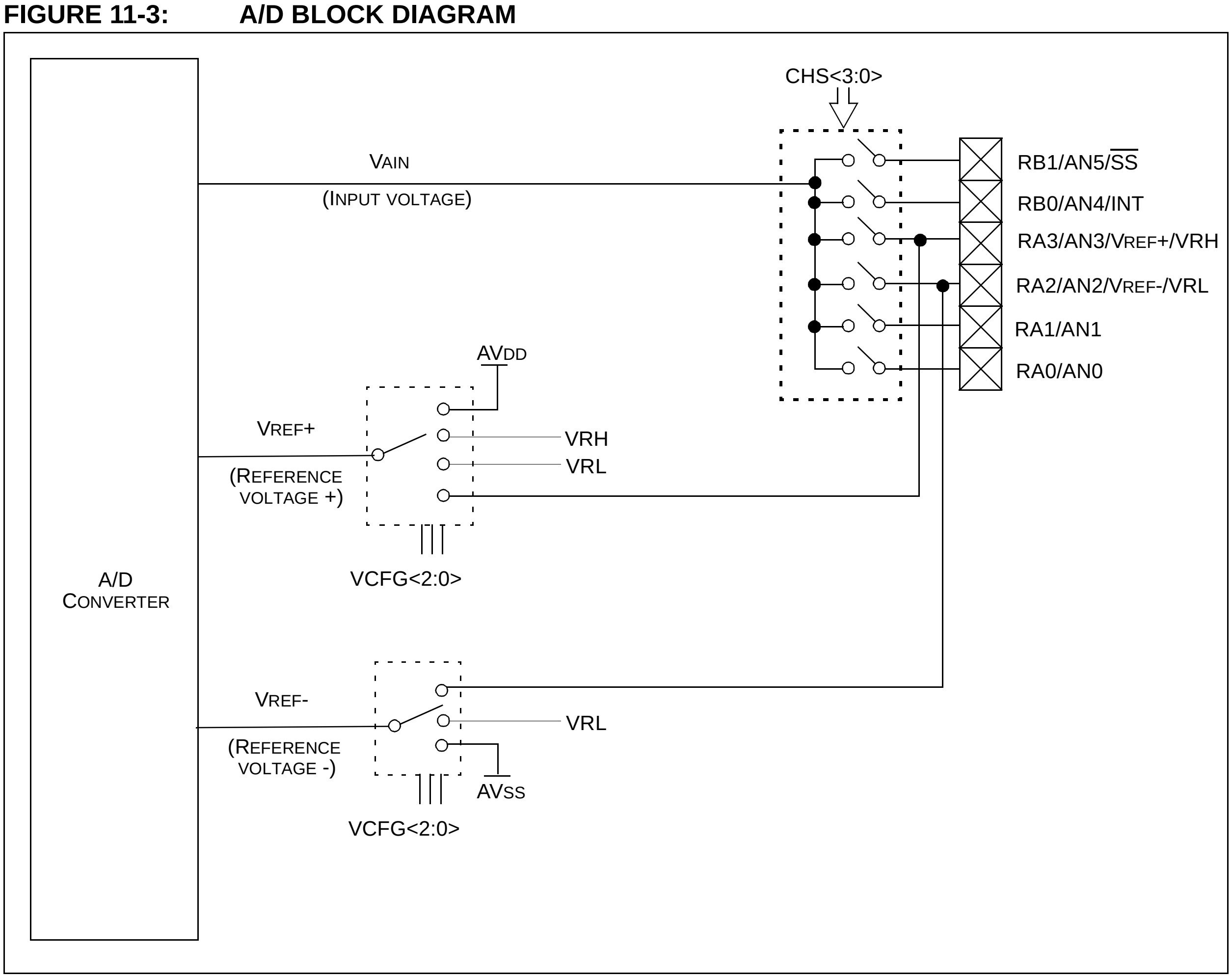
1. Configure port pins:
   - Configure Analog Input mode (ANSEL)
   - Configure pin as input (TRISA or TRISB)
2. Configure the A/D module
   - Configure A/D Result Format / voltage reference (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
3. Configure A/D interrupt (if required)
   - Clear ADIF bit
   - Set ADIE bit
   - Set PEIE bit
   - Set GIE bit
4. Wait the required acquisition time.
5. START conversion
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0)
6. Wait $13T_{AD}$ until A/D conversion is complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
7. Read A/D Result registers (ADRESH and ADRESL), clear ADIF if required.
8. For next conversion, go to step 1, step 2 or step 3 as required.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The ADRESH and ADRESL registers will be updated with the partially completed A/D conversion value. That is, the ADRESH and ADRESL registers will contain the value of the current incomplete conversion.

> **Note:** Do not set the ADON bit and the GO/$\overline{\text{DONE}}$ bit in the same instruction. Doing so will cause the GO/$\overline{\text{DONE}}$ bit to be automatically cleared.

FIGURE 11-3: A/D BLOCK DIAGRAM



12.3 RESET

The PIC16C717/770/771 devices have several different RESETS. These RESETS are grouped into two classifications; power-up and non-power-up. The power-up type RESETS are the Power-on and Brown-out Resets which assume the device VDD was below its normal operating range for the device's configuration. The non power-up type RESETS assume normal operating limits were maintained before/during and after the RESET.

- Power-on Reset (POR)
- Programmable Brown-out Reset (PBOR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during SLEEP
- WDT Reset (during normal operation)

Some registers are not affected in any RESET condition. Their status is unknown on a Power-up Reset and unchanged in any other RESET. Most other registers are placed into an initialized state upon RESET, however they are not affected by a WDT Reset during SLEEP, because this is considered a WDT Wake-up, which is viewed as the resumption of normal operation.

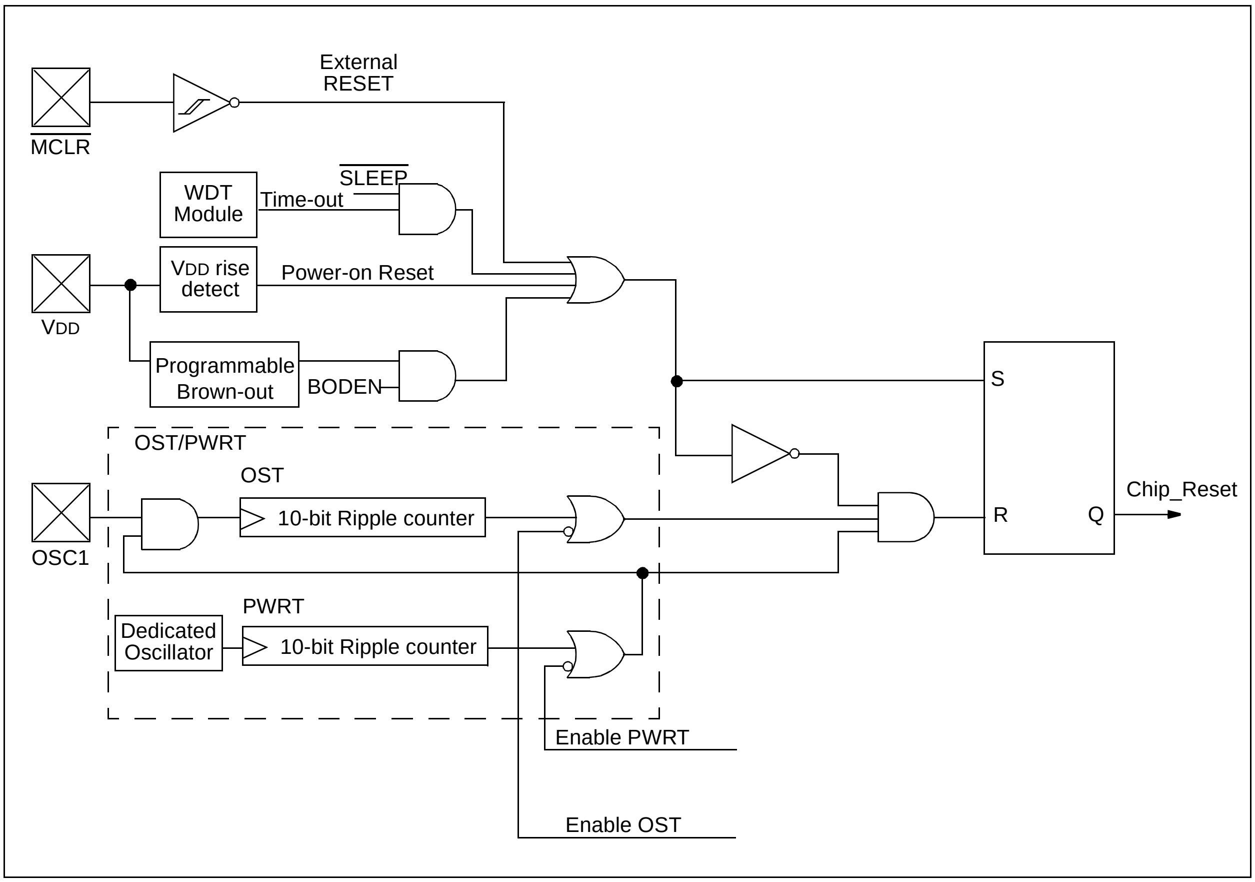
Several status bits have been provided to indicate which RESET occurred (see Table 12-4). See Table 12-6 for a full description of RESET states of all registers.

A simplified block diagram of the On-Chip Reset circuit is shown in Figure 12-4.

These devices have a $\overline{\text{MCLR}}$ noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

FIGURE 12-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



12.10 Interrupts

The devices have up to 11 sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

A Global Interrupt Enable bit, GIE (INTCON<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on RESET.

The "return from interrupt" instruction, `RETFIE`, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

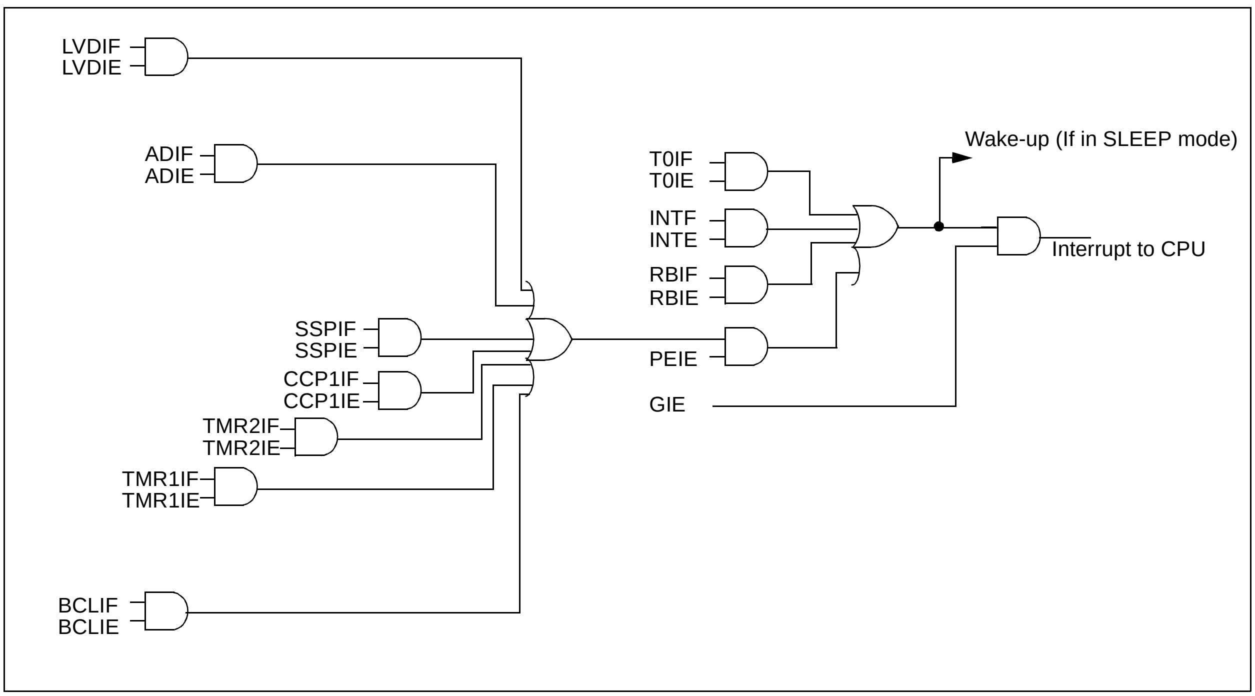
The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2, and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit

FIGURE 12-10: INTERRUPT LOGIC



14.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

14.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

14.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

TABLE 15-6: ENHANCED CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

Param. No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**717/770/771	10	—	—	ns	
				PIC16**LC**717/770/771	20	—	—	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**717/770/771	10	—	—	ns	
				PIC16**LC**717/770/771	20	—	—	ns	
52*	TccP	CCP1 input period			$\frac{3TCY + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)
53*	TccR	CCP1 output fall time		PIC16**C**717/770/771	—	10	25	ns	
				PIC16**LC**717/770/771	—	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16**C**717/770/771	—	10	25	ns	
				PIC16**LC**717/770/771	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.4.5 A/D CONVERTER MODULE

TABLE 15-11: PIC16C770/771 AND PIC16LC770/771 A/D CONVERTER CHARACTERISTICS:

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	12 bits	bit	Min. resolution for A/D is 1 mV, VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A03	EIL	Integral error	—	—	±2	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A04	EDL	Differential error	—	—	+2 -1	LSb	No missing codes to 12 bits VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A06	EOFF	Offset error	—	—	±2	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A07	EGN	Gain Error	—	—	±2	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A10	—	Monotonicity	—	Note 3	—	—	AVSS ≤ VAIN ≤ VREF+
A20*	VREF	Reference voltage (VREF+ - VREF-)	4.096	—	VDD +0.3V	V	Absolute minimum electrical spec to ensure 12-bit accuracy.
A21*	VREF+	Reference V High (AVDD or VREF+)	VREF-	—	AVDD	V	Min. resolution for A/D is 1 mV
A22*	VREF-	Reference V Low (AVSS or VREF-)	AVSS	—	VREF+	V	Min. resolution for A/D is 1 mV
A25*	VAIN	Analog input voltage	VREFL	—	VREFH	V	
A30*	ZAIN	Recommended impedance of analog voltage source	—	—	2.5	kΩ	
A50*	IREF	VREF input current **(Note 2)**	—	—	10	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 11.0. During A/D conversion cycle.

* These parameters are characterized but not tested.

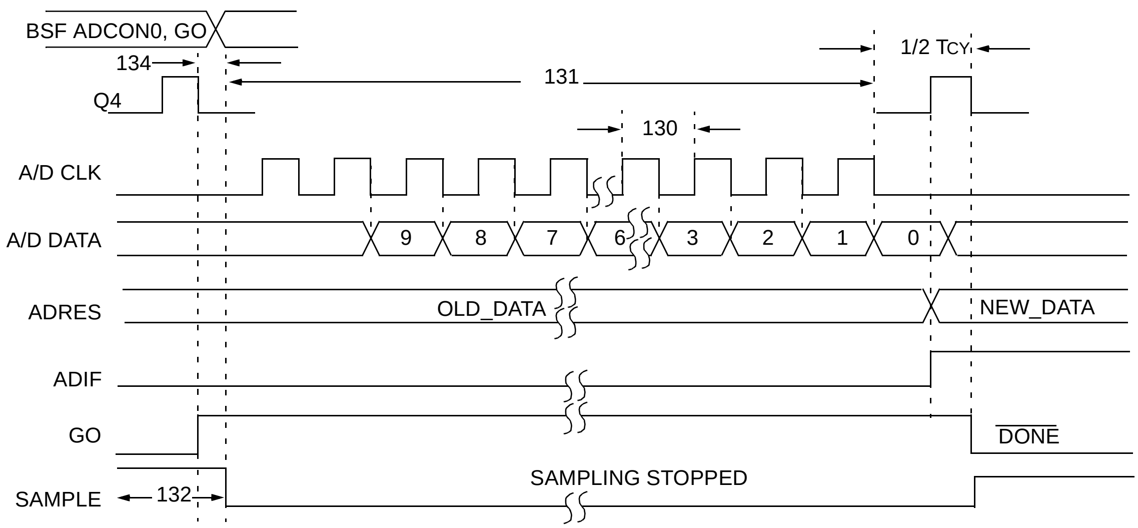
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF input current is from External VREF+, or VREF-, or AVSS, or AVDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

FIGURE 15-16: PIC16C717 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

TABLE 15-15: PIC16C717 AND PIC16LC717 A/D CONVERSION REQUIREMENT (NORMAL MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	1.6	—	—	μs	Tosc based, VREF ≥ 2.5V
			3.0	—	—	μs	Tosc based, VREF full range
							ADCS<1:0> = 11 (A/D RC mode)
			3.0	6.0	9.0	μs	At VDD = 2.5V
			2.0	4.0	6.0	μs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	11TAD	—	TAD	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	μs	
			5*	—	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2	—	—	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

FIGURE 16-2: TYPICAL IDD VS. FOSC OVER VDD (HS MODE)

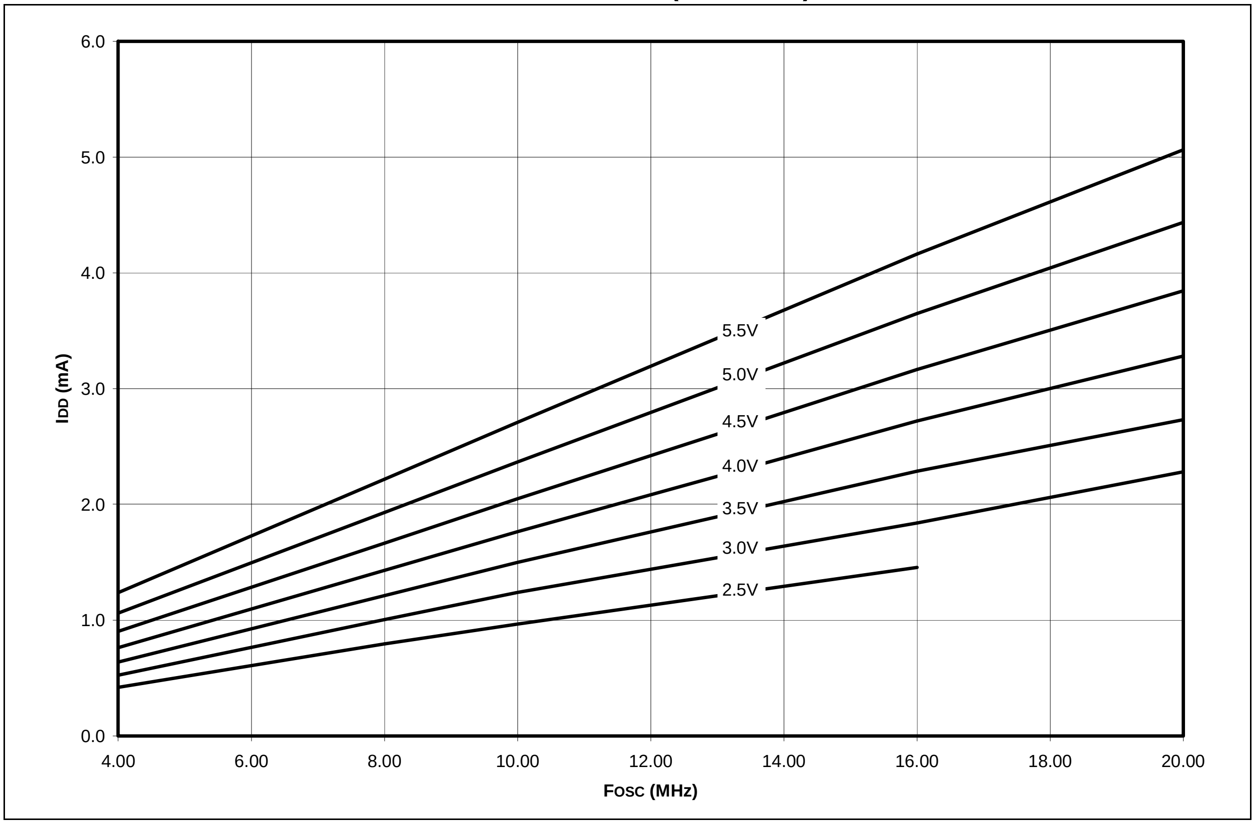


FIGURE 16-3: MAXIMUM IDD VS. FOSC OVER VDD (XT MODE)

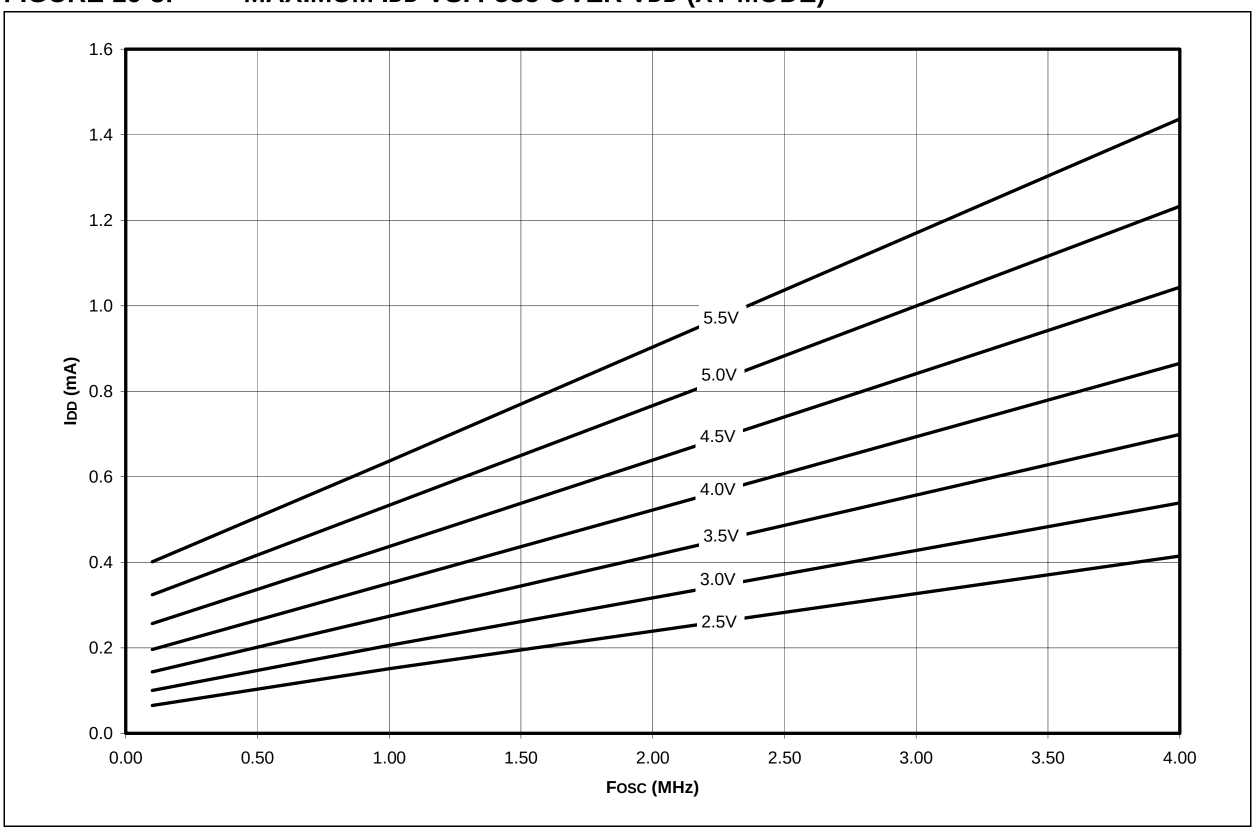


FIGURE 16-16: TYPICAL IDD VS. VDD (INTRC 4 MHz MODE)

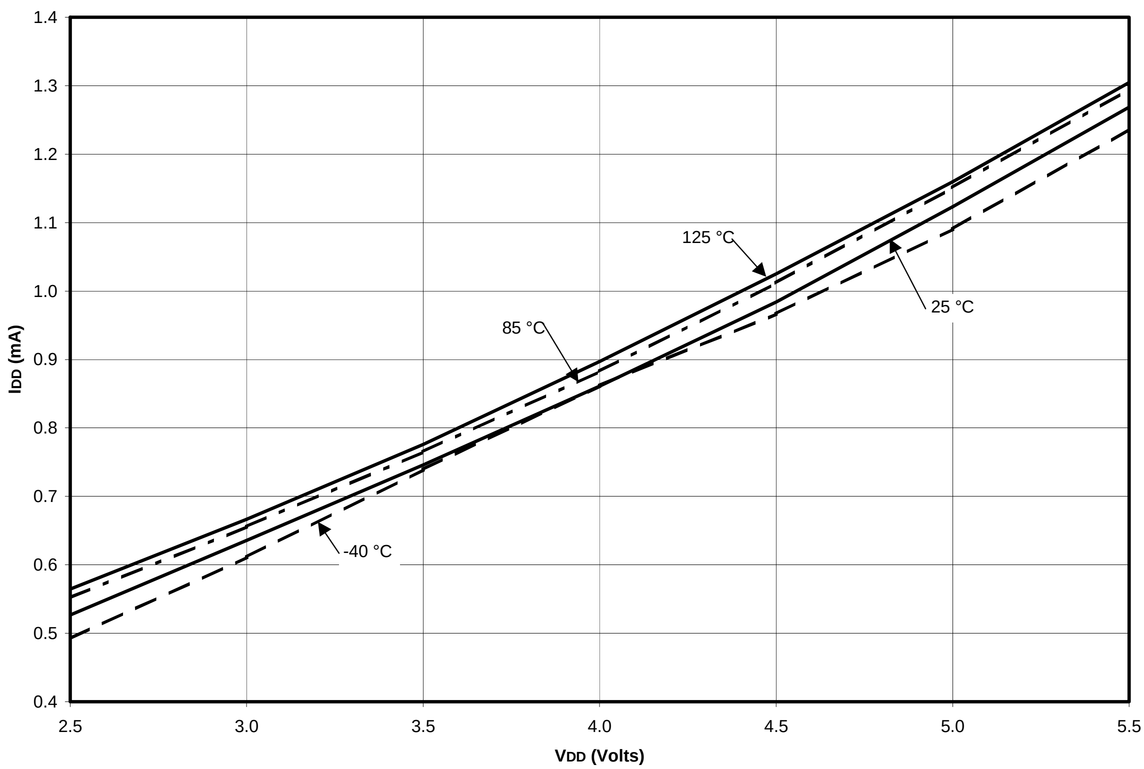
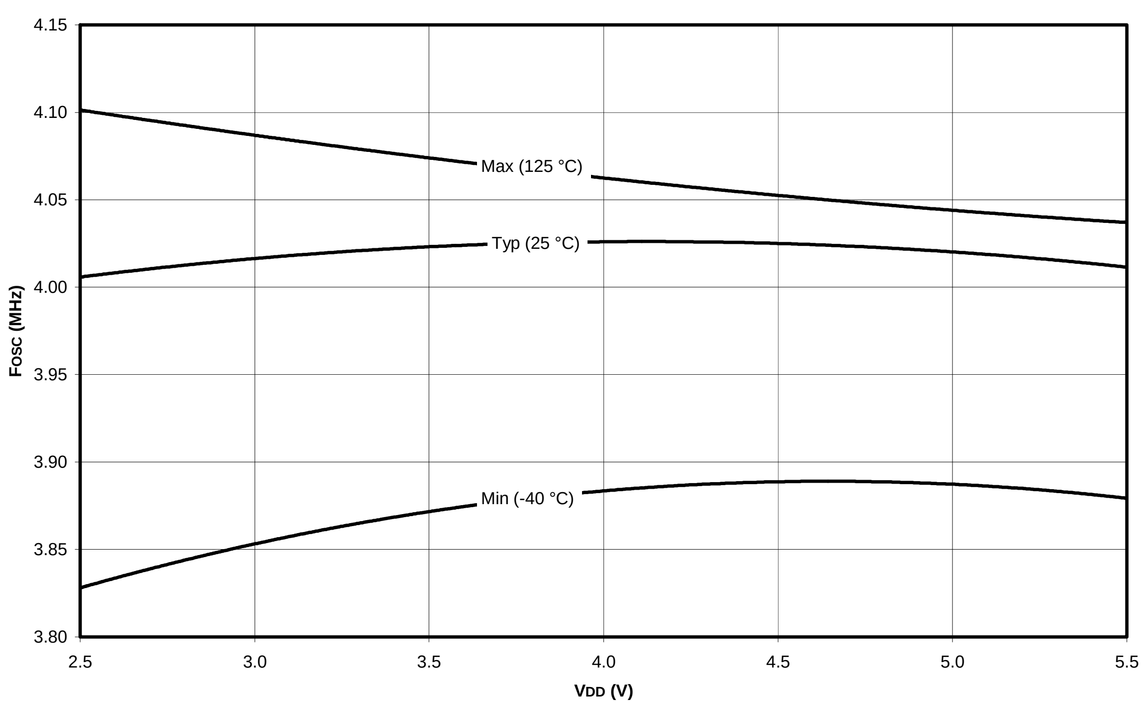
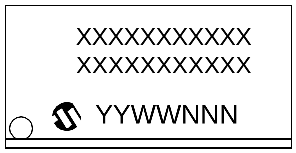


FIGURE 16-17: INTERNAL RC FOSC VS. VDD OVER TEMPERATURE (4 MHz)

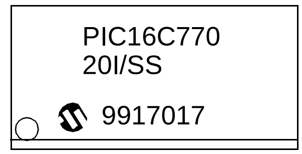


17.1 Package Marking Information (Cont'd)

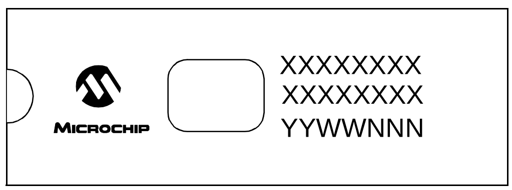
20-Lead SSOP



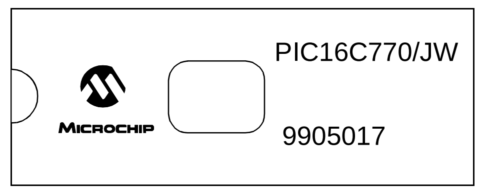
Example



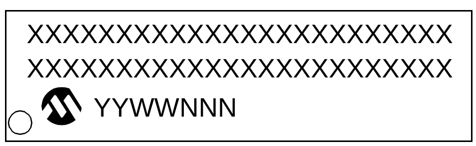
20-Lead CERDIP Windowed



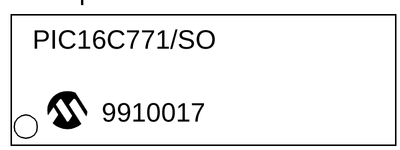
Example



20-Lead SOIC

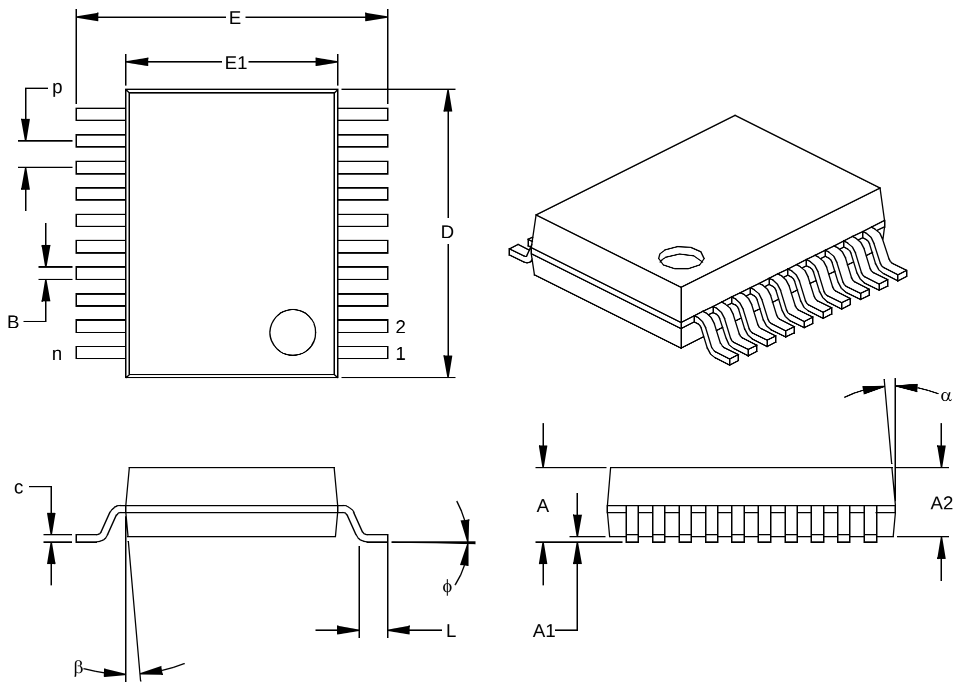


Example



17.8 20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

NOTES: