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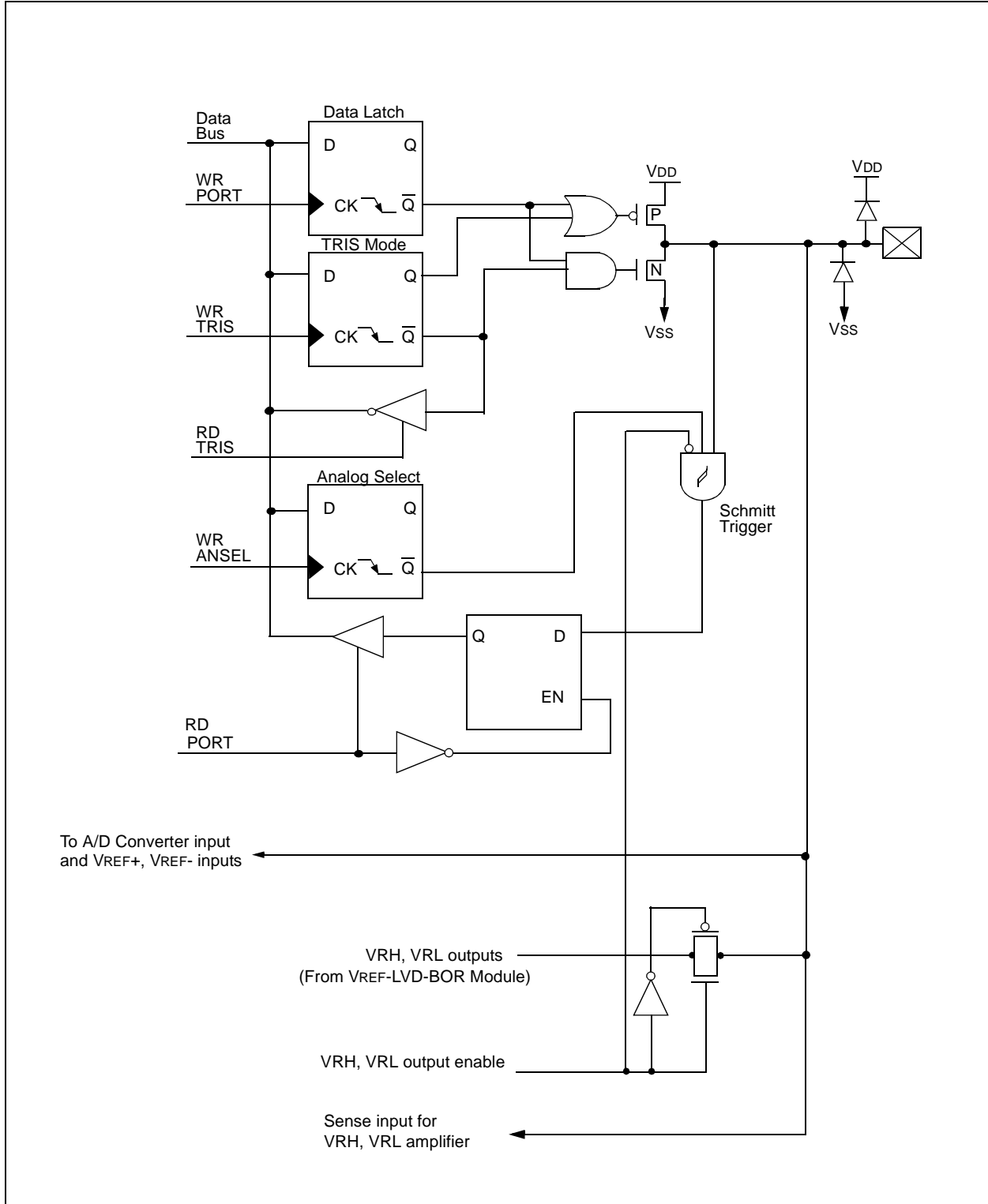
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

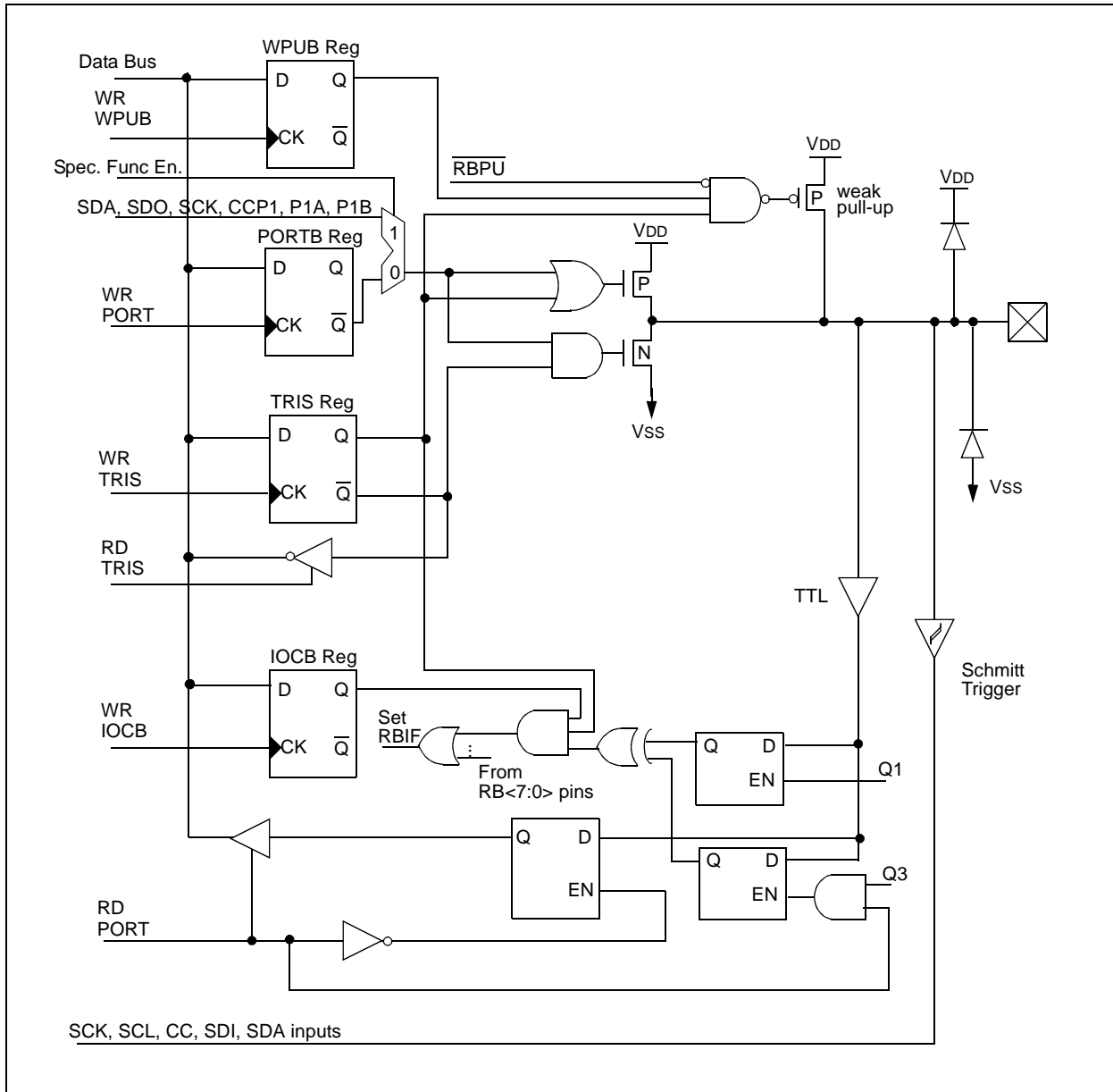
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c717-ss

FIGURE 3-2: BLOCK DIAGRAM OF RA2/AN2/VREF-/VRL AND RA3/AN3/VREF+/VRH



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FIGURE 3-8: BLOCK DIAGRAM OF RB2/SCK/SCL, RB3/CCP1/P1A, RB4/SDI/SDA, RB5/SDO/P1B



4.3 READING THE EPROM PROGRAM MEMORY

To read a program memory location, the user must write 2 bytes of the address to the PMADRH and PMADRL registers, then set control bit RD (PMCON1<0>). Once the read control bit is set, the Program Memory Read (PMR) controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following

the “BSF PMCON1,RD” instruction to be ignored. The data is available, in the very next cycle, in the PMDATH and PMDATL registers; therefore it can be read as 2 bytes in the following instructions. PMDATH and PMDATL registers will hold this value until another Program Memory Read or until it is written to by the user.

Note: The two instructions that follow setting the PMCON1 read bit must be NOPS.

EXAMPLE 4-1: OTP PROGRAM MEMORY Read

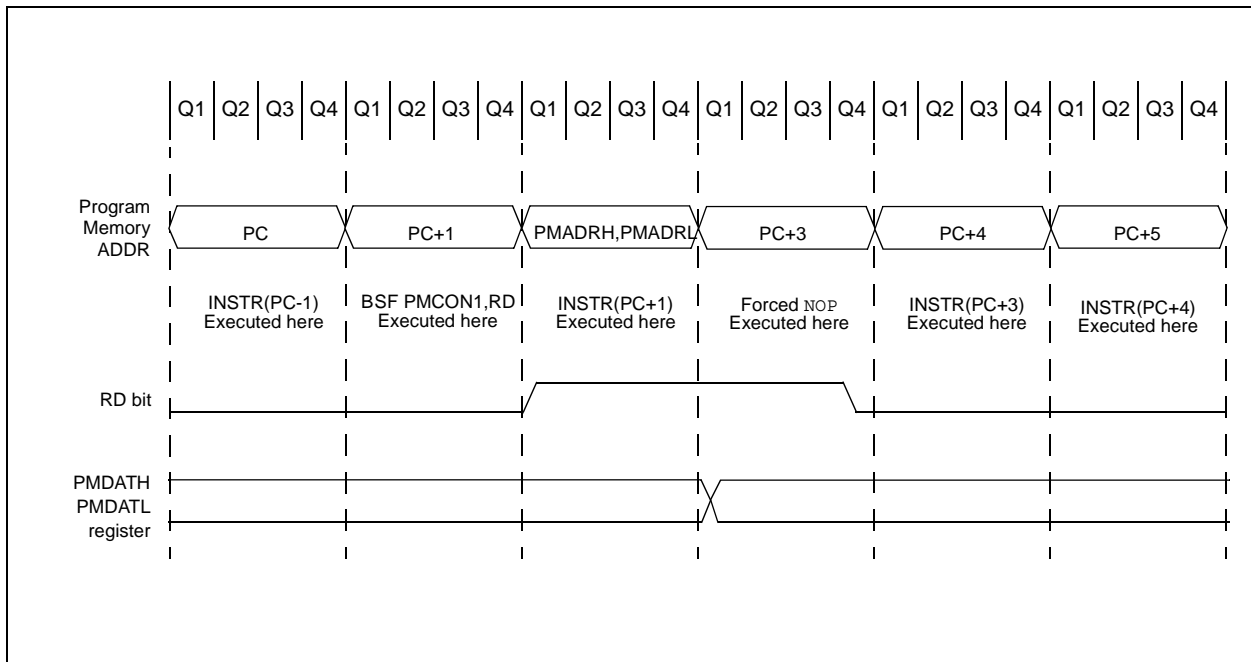
```

BSF    STATUS, RP1    ;
BCF    STATUS, RP0    ; Bank 2
MOVLW  MS_PROG_PM_ADDR ;
MOVWF  PMADRH         ; MS Byte of Program Memory Address to read
MOVLW  LS_PROG_PM_ADDR ;
MOVWF  PMADRL         ; LS Byte of Program Memory Address to read
BSF    STATUS, RP0    ; Bank 3
BSF    PMCON1, RD     ; Program Memory Read
NOP    ; This instruction must be an NOP
NOP    ; This instruction must be an NOP
next instruction      ; PMDATH:PMDATL now has the data
    
```

4.4 OPERATION DURING CODE PROTECT

When the device is code protected, the CPU can still perform the Program Memory Read function.

FIGURE 4-1: PROGRAM MEMORY READ CYCLE EXECUTION



6.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
(Two 8-bit registers; TMR1H and TMR1L)
- Readable and writable (Both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- RESET from ECCP module trigger

Timer1 has a control register, shown in Register 6-1. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Figure 6-2 is a simplified block diagram of the Timer1 module.

Additional information on timer modules is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

6.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

The Operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

REGISTER 6-1: TIMER1 CONTROL REGISTER (T1CON: 10h)

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
	bit 7							bit 0
bit 7-6	Unimplemented: Read as '0'							
bit 5-4	T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits							
	11 = 1:8 Prescale value							
	10 = 1:4 Prescale value							
	01 = 1:2 Prescale value							
	00 = 1:1 Prescale value							
bit 3	T1OSCEN: Timer1 Oscillator Enable Control bit							
	1 = Oscillator is enabled							
	0 = Oscillator is shut off ⁽¹⁾							
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Control bit							
	<u>TMR1CS = 1:</u>							
	1 = Do not synchronize external clock input							
	0 = Synchronize external clock input							
	<u>TMR1CS = 0:</u>							
	This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.							
bit 1	TMR1CS: Timer1 Clock Source Select bit							
	1 = External clock from pin RB6/T1OSO/T1CKI /P1C (on the rising edge)							
	0 = Internal clock (Fosc/4)							
bit 0	TMR1ON: Timer1 On bit							
	1 = Enables Timer1							
	0 = Stops Timer1							

Note 1: The oscillator inverter and feedback resistor are turned off to eliminate power drain.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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6.1.1 TIMER1 COUNTER OPERATION

In this mode, Timer1 is being incremented via an external source. Increments occur on a rising edge. After Timer1 is enabled in Counter mode, the module must first have a falling edge before the counter begins to increment.

FIGURE 6-1: TIMER1 INCREMENTING EDGE

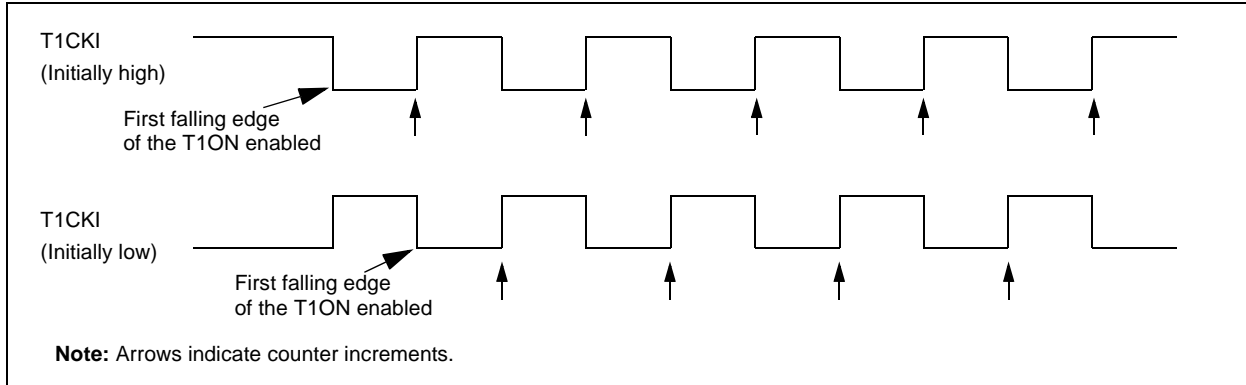
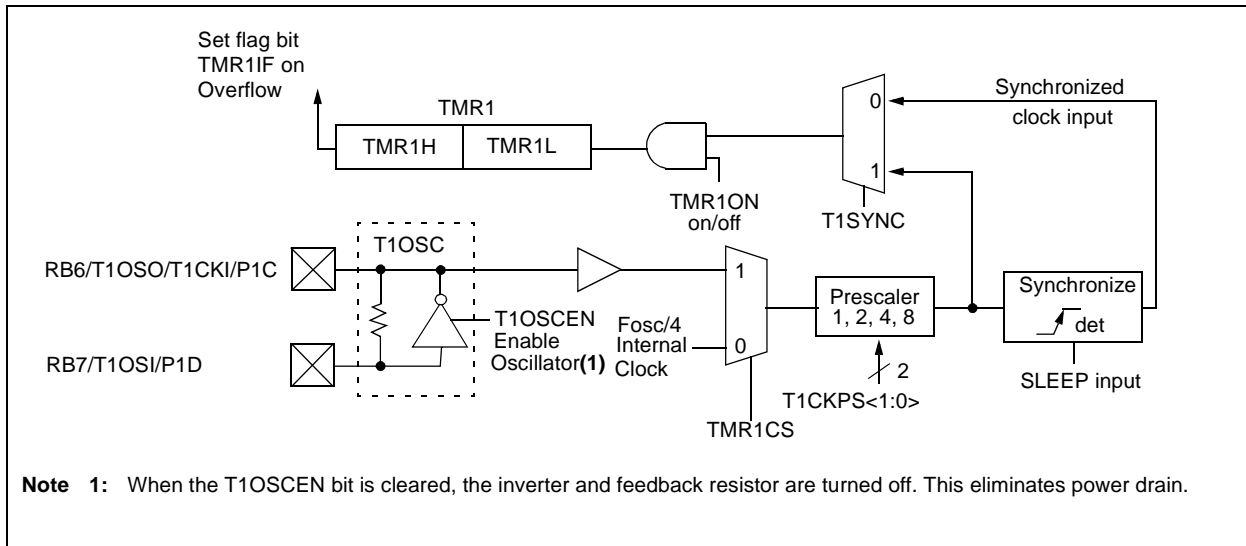


FIGURE 6-2: TIMER1 BLOCK DIAGRAM

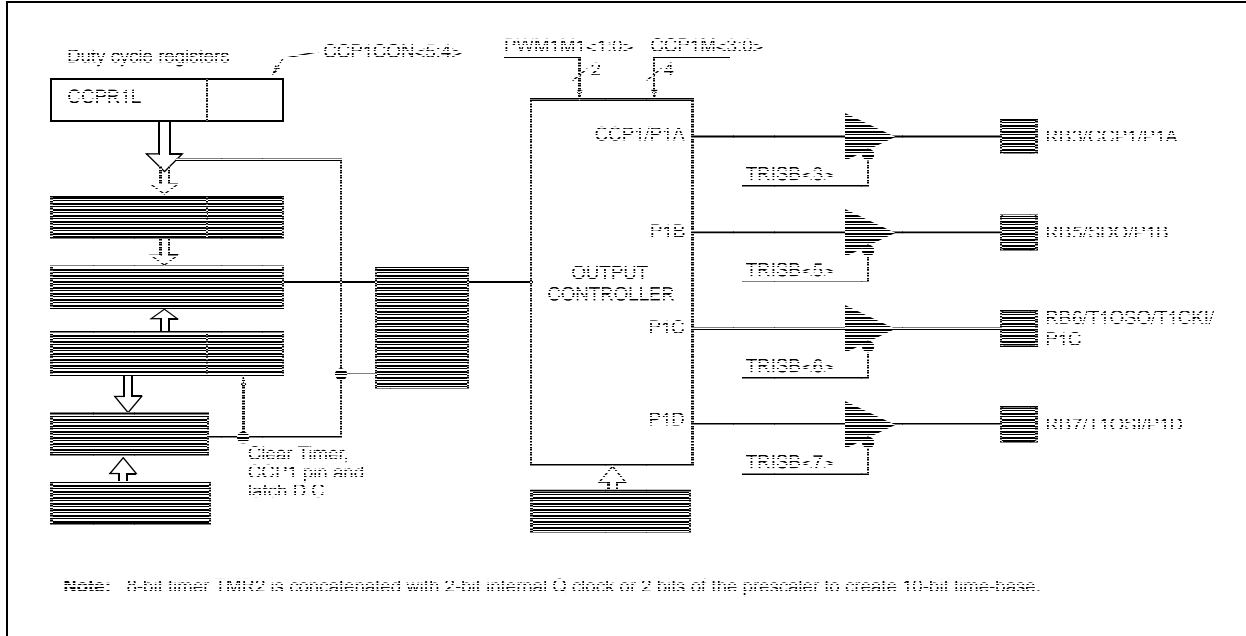


PIC16C717/770/771

8.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the ECCP module produces up to a 10-bit resolution PWM output. Figure 8-3 shows the simplified PWM block diagram.

FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM PERIOD} = \frac{[(\text{PR2}) + 1] \cdot 4 \cdot \text{TOSC}}{(\text{TMR2 PRESCALE VALUE})}$$

PWM frequency is defined as $1 / [\text{PWM period}]$.

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

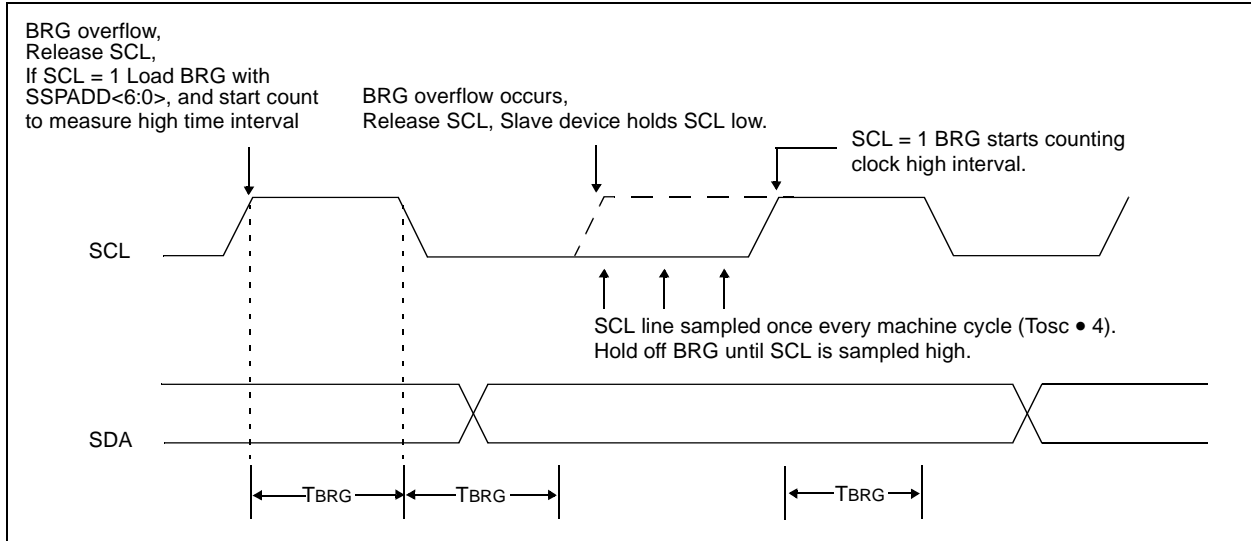
Note: The Timer2 postscaler (see Section 7.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

9.2.16 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or repeated START/STOP condition, de-asserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the

SCL pin is actually sampled high. When the SCL pin is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 9-22).

FIGURE 9-22: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE



11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has six inputs for the PIC16C717/770/771.

The PIC16C717 analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 10-bit digital value, while the A/D converter in the PIC16C770/771 allows conversion to a corresponding 12-bit digital value. The A/D module has up to 6 analog inputs, which are multiplexed into one sample and hold. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltages are software selectable to either the device's analog positive and negative supply voltages (AVDD/AVSS), the voltage level on the VREF+ and VREF- pins, or internal voltage references if enabled (VRH, VRL).

The A/D converter can be triggered by setting the $\overline{\text{GO/DONE}}$ bit, or by the special event Compare mode of the ECCP module. When conversion is complete, the $\overline{\text{GO/DONE}}$ bit returns to '0', the ADIF bit in the PIR1 register is set, and an A/D interrupt will occur, if enabled.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result Register Low ADRESL
- A/D Result Register High ADRESH
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off and any conversion is aborted.

11.1 Control Registers

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins, the voltage reference configuration and the result format. The ANSEL register, shown in Register 3-1, selects between the Analog or Digital Port Pin modes. The port pins can be configured as analog inputs or as digital I/O.

The combination of the ADRESH and ADRESL registers contain the result of the A/D conversion. The register pair is referred to as the ADRES register. When the A/D conversion is complete, the result is loaded into ADRES, the $\overline{\text{GO/DONE}}$ bit (ADCON0<2>) is cleared, and the A/D interrupt flag ADIF is set. The block diagram of the A/D module is shown in Figure 11-3.

11.7 Use of the ECCP Trigger

An A/D conversion can be started by the “special event trigger” of the CCP module. This requires that the CCP1M<3:0> bits be programmed as 1011b and that the A/D module is enabled (ADON is set). When the trigger occurs, the GO/DONE bit will be set on Q2 to start the A/D conversion and the Timer1 counter will be reset to zero. Timer1 is RESET to automatically repeat the A/D conversion cycle, with minimal software overhead (moving the ADRESH and ADRESL to the desired location). The appropriate analog input channel must be selected before the “special event trigger” sets the GO/DONE bit (starts a conversion cycle).

If the A/D module is not enabled (ADON is cleared), then the “special event trigger” will be ignored by the A/D module, but will still RESET the Timer1 counter.

11.8 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRESH and ADRESL registers are not modified. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

11.9 Faster Conversion - Lower Resolution Trade-off

Not all applications require a result with 12 bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the A/D module may be halted by clearing the GO/DONE bit after the desired number of bits in the result have been converted. Once the GO/DONE bit has been cleared, all of the remaining A/D result bits are '0'. The equation to determine the time before the GO/DONE bit can be switched is as follows:

$$\text{Conversion time} = (N+1)T_{AD}$$

Where: N = number of bits of resolution required, and 1T_{AD} is the amplifier settling time.

Since T_{AD} is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D GO/DONE bit may be cleared. Table 11-4 shows a comparison of time required for a conversion with 4 bits of resolution, versus the normal 12-bit resolution conversion. The example is for devices operating at 20 MHz. The A/D clock is programmed for 32 T_{osc}.

EXAMPLE 11-4: 4-BIT vs. 12-BIT CONVERSION TIME Example

4-Bit Example:

$$\begin{aligned}\text{Conversion Time} &= (N + 1) T_{AD} \\ &= (4 + 1) T_{AD} \\ &= (5)(1.6 \mu\text{S}) \\ &= 8 \mu\text{S}\end{aligned}$$

12-Bit Example:

$$\begin{aligned}\text{Conversion Time} &= (N + 1) T_{AD} \\ &= (12 + 1) T_{AD} \\ &= (13)(1.6 \mu\text{S}) \\ &= 20.8 \mu\text{S}\end{aligned}$$

13.1 Instruction Descriptions

ADDLW **Add Literal and W**

Syntax: *[label]* ADDLW k
 Operands: $0 \leq k \leq 255$
 Operation: $(W) + k \rightarrow (W)$
 Status Affected: C, DC, Z
 Description: The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

ANDWF **AND W with f**

Syntax: *[label]* ANDWF f,d
 Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
 Operation: $(W) .AND. (f) \rightarrow (\text{destination})$
 Status Affected: Z
 Description: AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ADDWF **Add W and f**

Syntax: *[label]* ADDWF f,d
 Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
 Operation: $(W) + (f) \rightarrow (\text{destination})$
 Status Affected: C, DC, Z
 Description: Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF **Bit Clear f**

Syntax: *[label]* BCF f,b
 Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$
 Operation: $0 \rightarrow (f)$
 Status Affected: None
 Description: Bit 'b' in register 'f' is cleared.

ANDLW **AND Literal with W**

Syntax: *[label]* ANDLW k
 Operands: $0 \leq k \leq 255$
 Operation: $(W) .AND. (k) \rightarrow (W)$
 Status Affected: Z
 Description: The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.

BSF **Bit Set f**

Syntax: *[label]* BSF f,b
 Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$
 Operation: $1 \rightarrow (f)$
 Status Affected: None
 Description: Bit 'b' in register 'f' is set.

TABLE 15-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC16C717/770/771 AND PIC16LC717/770/771

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
		Operating Voltage V_{DD} range is described in Section and Section					
Parameter No.	Sym	Characteristic	Min	Typ ^{(1)*}	Max	Units	Conditions
	FIRC	Internal Calibrated RC Frequency	3.65	4.00	4.28	MHz	$V_{DD} = 5.0\text{V}$
		Internal RC Frequency*	3.55	4.00	4.31	MHz	$V_{DD} = 2.5\text{V}$

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

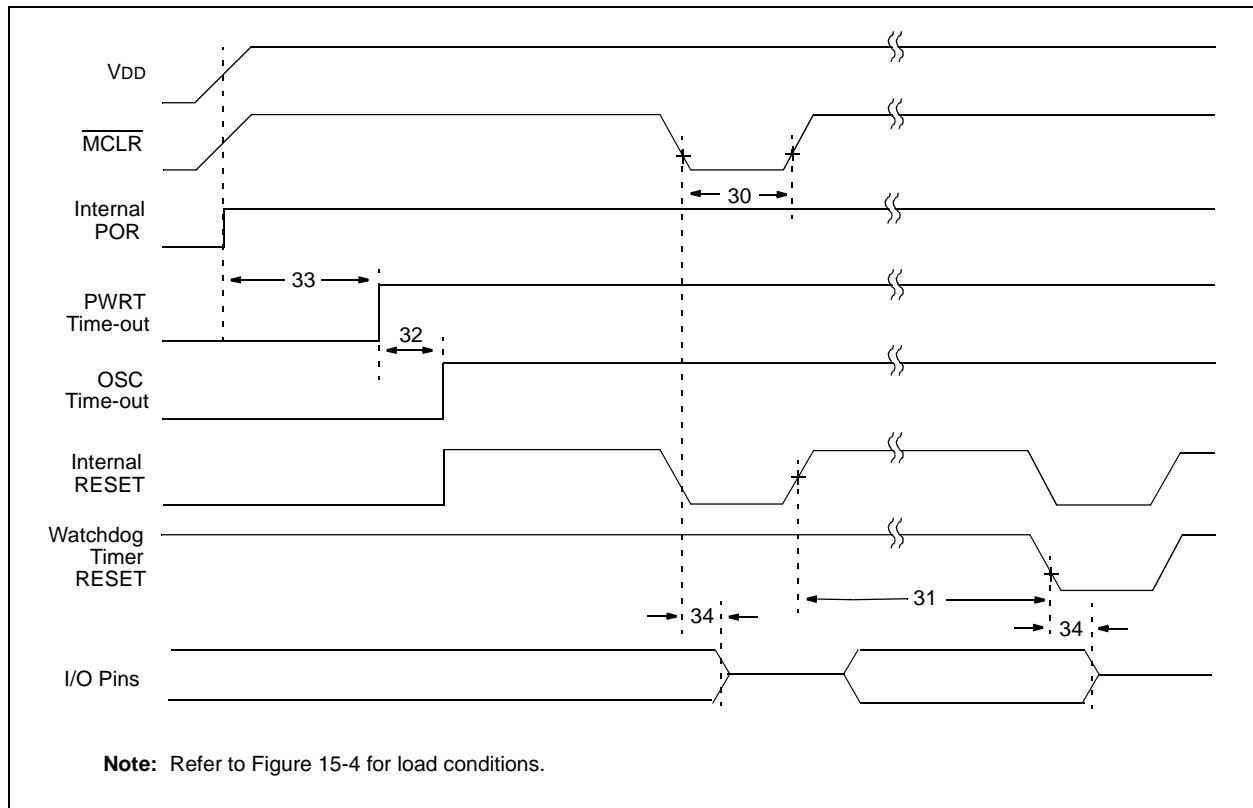
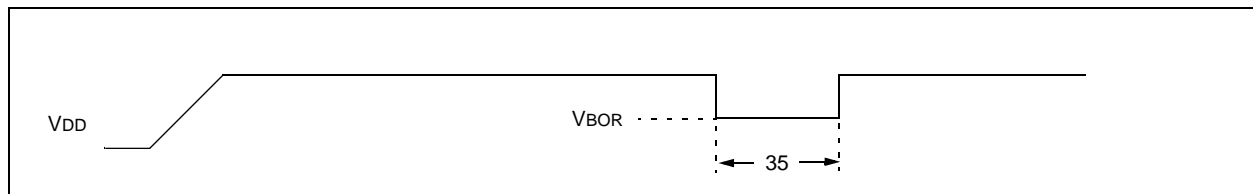


FIGURE 15-8: BROWN-OUT RESET TIMING



PIC16C717/770/771

FIGURE 15-17: PIC16C717 A/D CONVERSION TIMING (SLEEP MODE)

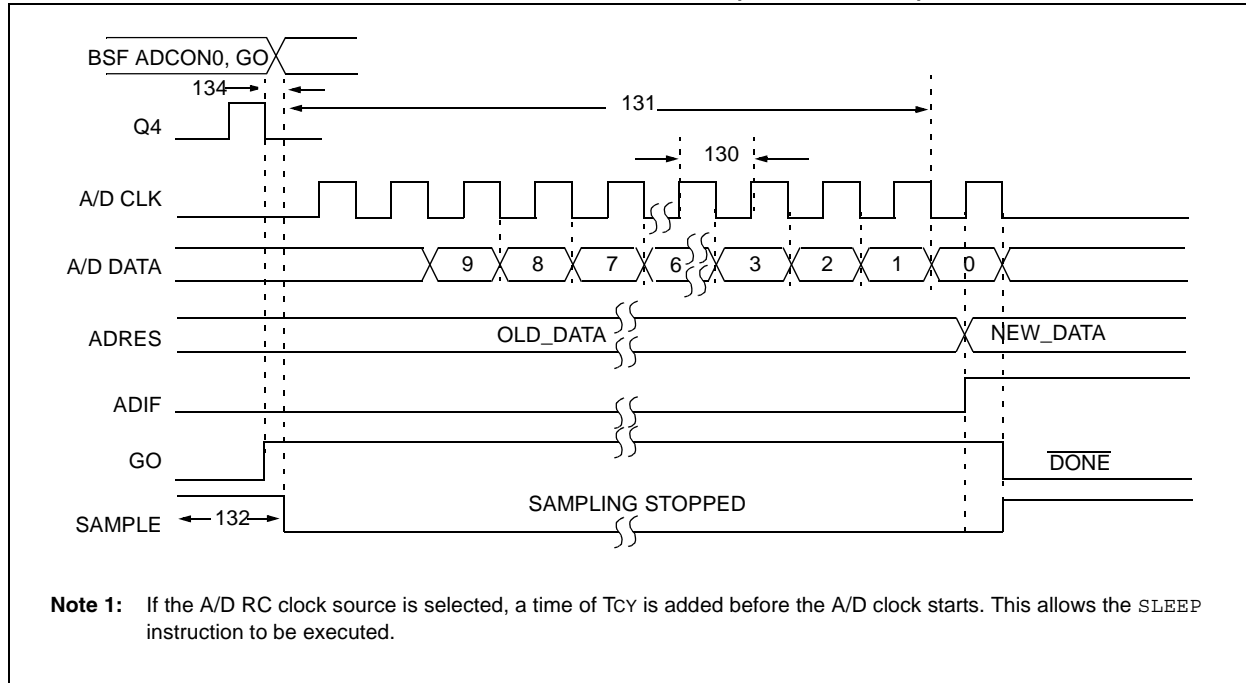


TABLE 15-16: PIC16C717 AND PIC16LC717 A/D CONVERSION REQUIREMENT (SLEEP MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	3.0	6.0	9.0	μs	ADCS<1:0> = 11 (A/D RC mode) At $V_{DD} = 3.0\text{V}$ At $V_{DD} = 5.0\text{V}$
			2.0	4.0	6.0	μs	
131*	TCNV	Conversion time (not including acquisition time) (Note 1)	—	$11T_{AD}$	—	—	
132*	TACQ	Acquisition Time	(Note 2)	11.5	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
			5*	—	—	μs	
134*	TGO	Q4 to A/D clock start	—	$T_{OSC}/2 + T_{CY}$	—	—	If the A/D RC clock source is selected, a time of T_{CY} is added before the A/D clock starts. This allows the <code>SLEEP</code> instruction to be executed.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{CY} cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if V_{RH} or V_{RL} is selected as A/D reference.

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FIGURE 16-14: INTERNAL RC Fosc VS. VDD OVER TEMPERATURE (37 KHZ)

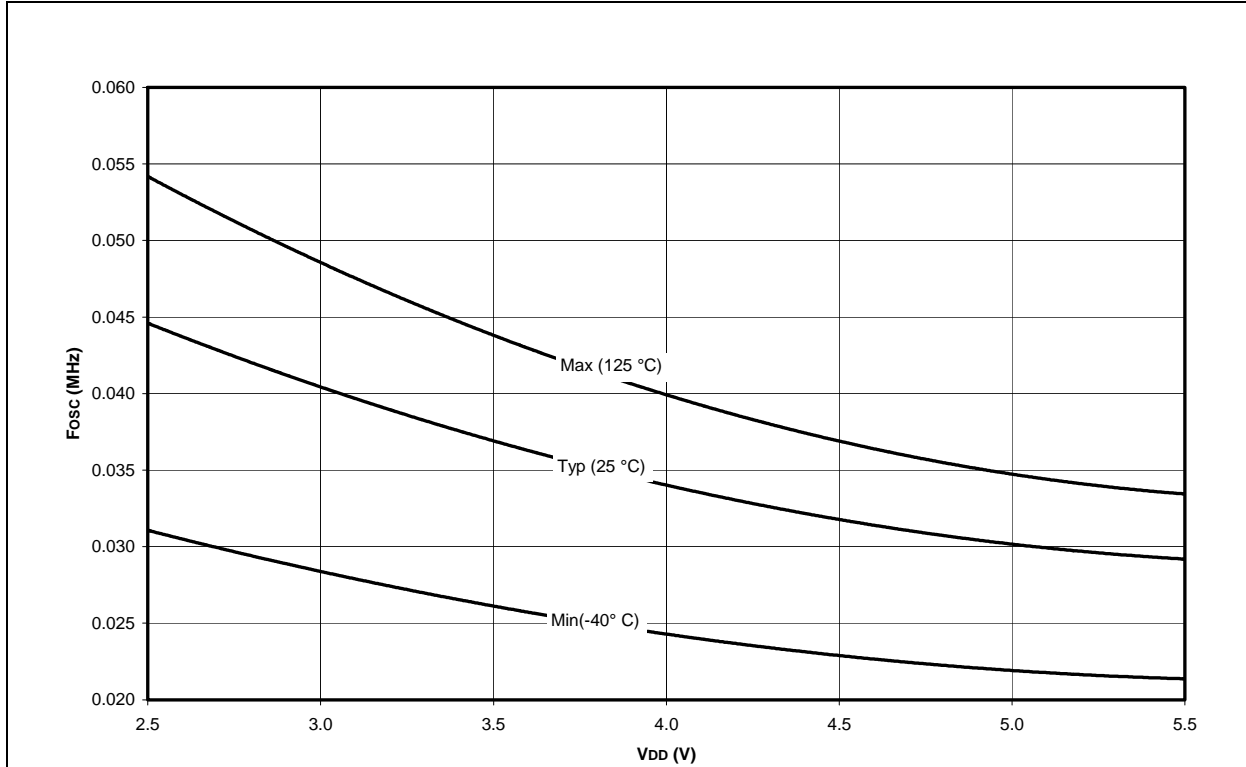


FIGURE 16-15: MAXIMUM AND TYPICAL I_{DD} VS. VDD (INTRC 4 MHz MODE)

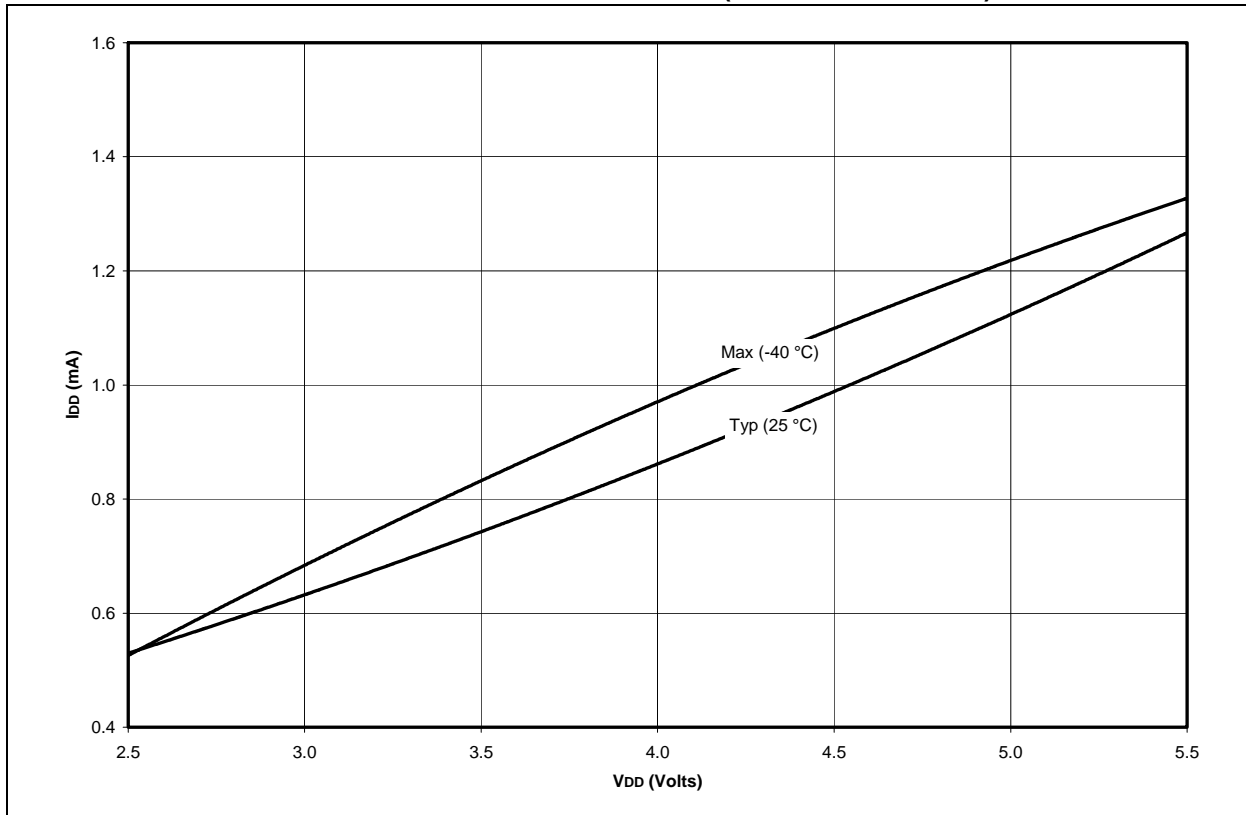


FIGURE 16-16: TYPICAL I_{DD} VS. V_{DD} (INTRC 4 MHz MODE)

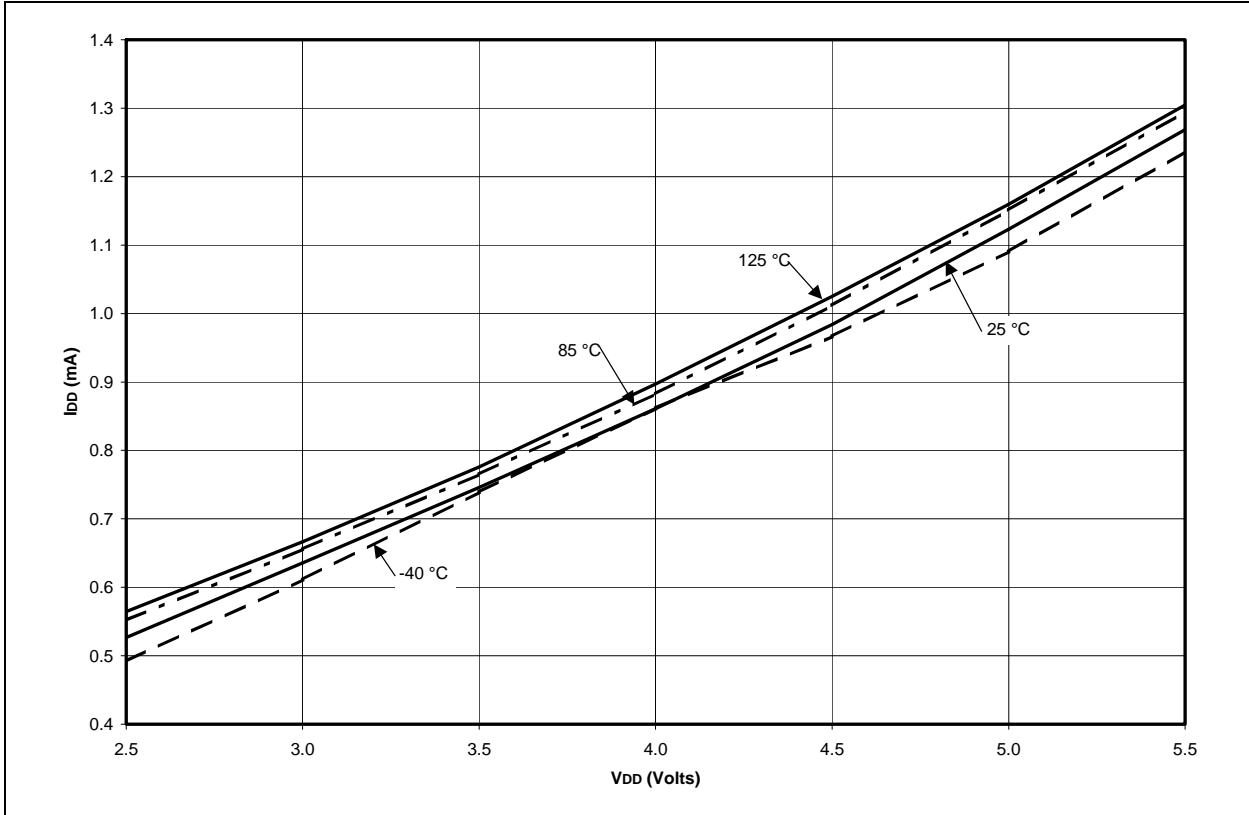
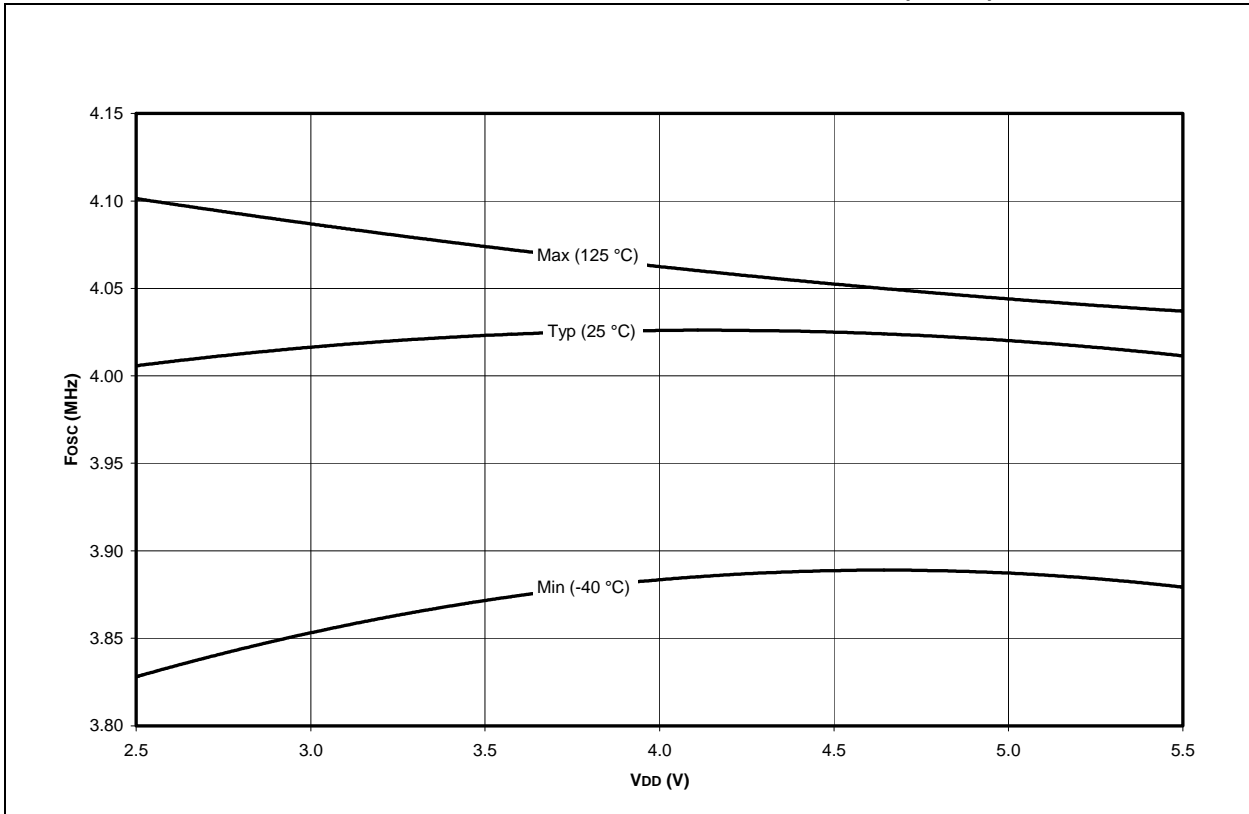


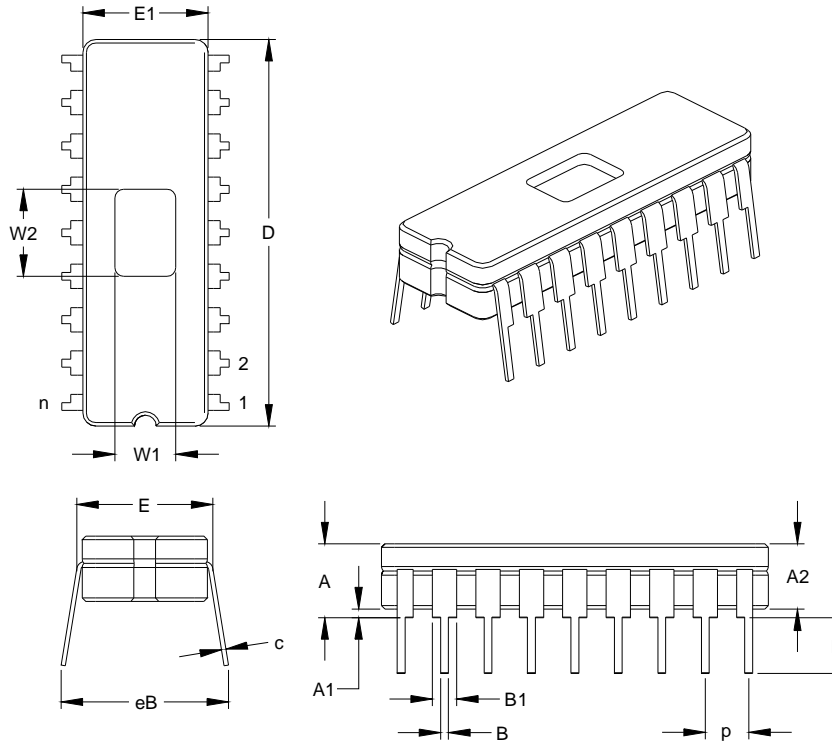
FIGURE 16-17: INTERNAL RC F_{osc} VS. V_{DD} OVER TEMPERATURE (4 MHz)



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17.3 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



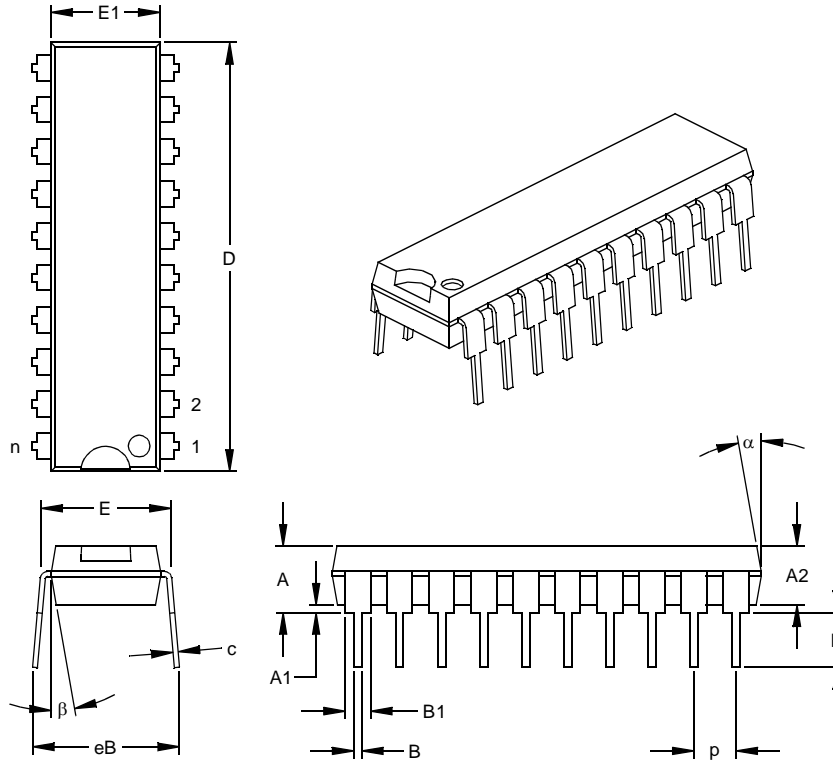
Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	P		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

*Controlling Parameter
JEDEC Equivalent: MO-036
Drawing No. C04-010

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17.5 20-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES*			MILLIMETERS			
		MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		20			20		
Pitch	p		.100			2.54		
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32	
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26	
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60	
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42	
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56	
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65	
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56	
Overall Row Spacing	§	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-019

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I	
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