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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c770-i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16c770-i-so</a>

# PIC16C717/770/771

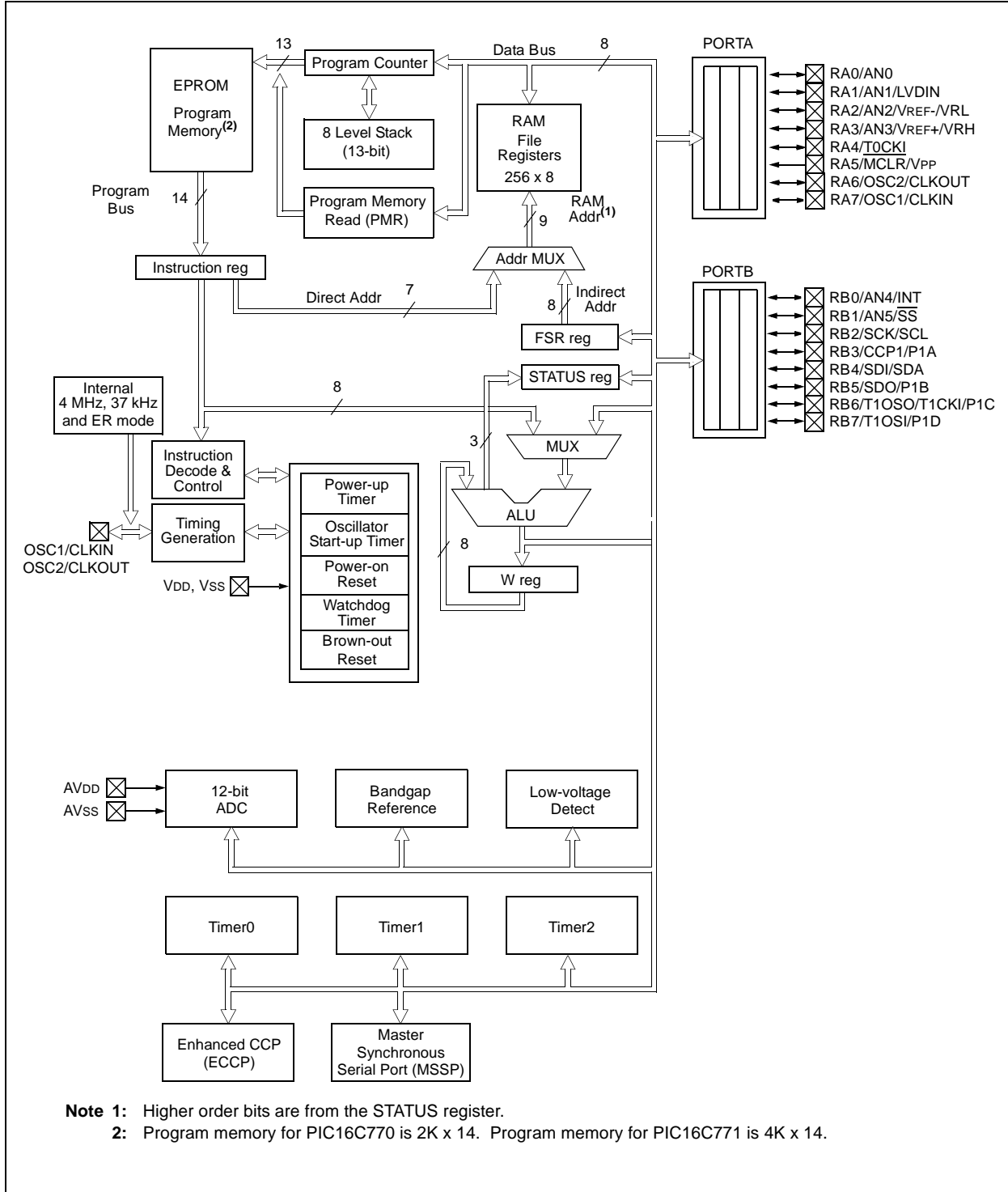
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NOTES:

# PIC16C717/770/771

FIGURE 1-2: PIC16C770/771 BLOCK DIAGRAM



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## 2.2.2.7 PIR2 REGISTER

This register contains the SSP Bus Collision and low-voltage detect interrupt flag bits.

**Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

### REGISTER 2-7: PERIPHERAL INTERRUPT REGISTER 2 (PIR2: 0Dh)

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
LVDIF	—	—	—	BCLIF	—	—	—
bit 7							bit 0

- bit 7     **LVDIF:** Low Voltage Detect Interrupt Flag bit  
1 = The supply voltage has fallen below the specified LVD voltage (must be cleared in software)  
0 = The supply voltage is greater than the specified LVD voltage
- bit 6-4   **Unimplemented:** Read as '0'
- bit 3     **BCLIF:** Bus Collision Interrupt Flag bit  
1 = A bus collision has occurred while the SSP module configured in I<sup>2</sup>C Master was transmitting (must be cleared in software)  
0 = No bus collision occurred
- bit 2-0   **Unimplemented:** Read as '0'

Legend:  
R = Readable bit           W = Writable bit           U = Unimplemented bit, read as '0'  
- n = Value at POR        '1' = Bit is set           '0' = Bit is cleared       x = Bit is unknown

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## EXAMPLE 3-1: Initializing PORTA

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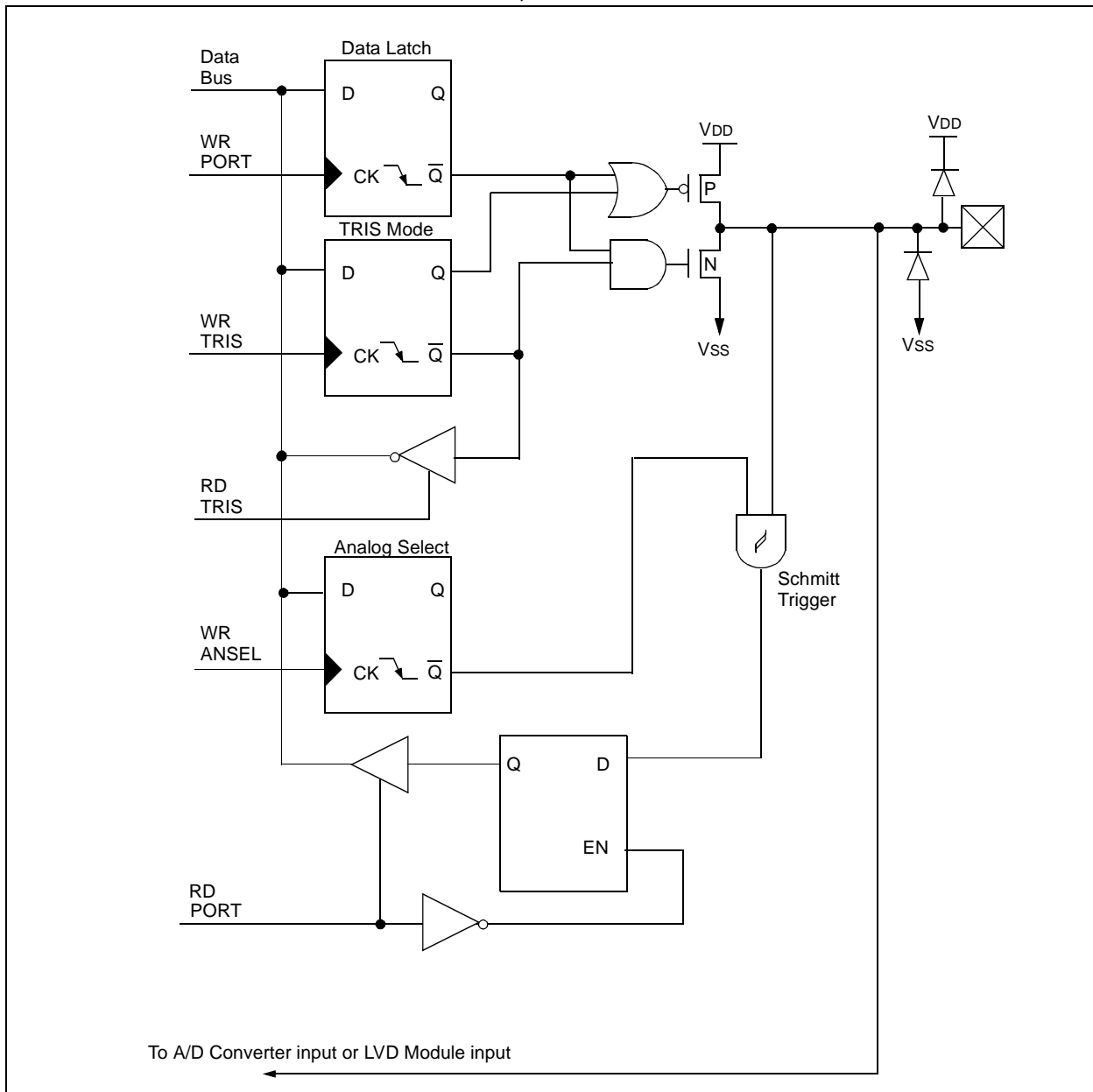
BCF STATUS, RP0 ; Select Bank 0
CLRF PORTA      ; Initialize PORTA by
                ; clearing output
                ; data latches

BSF STATUS, RP0 ; Select Bank 1
MOVLW 0Fh       ; Value used to
                ; initialize data
                ; direction

MOVWF TRISA     ; Set RA<3:0> as inputs
                ; RA<7:4> as outputs. RA<7:6>availability depends on oscillator selection.

MOVLW 03        ; Set RA<1:0> as analog inputs, RA<7:2> are digital I/O
MOVWF ANSEL
BCF STATUS, RP0 ; Return to Bank 0
    
```

FIGURE 3-1: BLOCK DIAGRAM OF RA0/AN0, RA1/AN1/LVDIN



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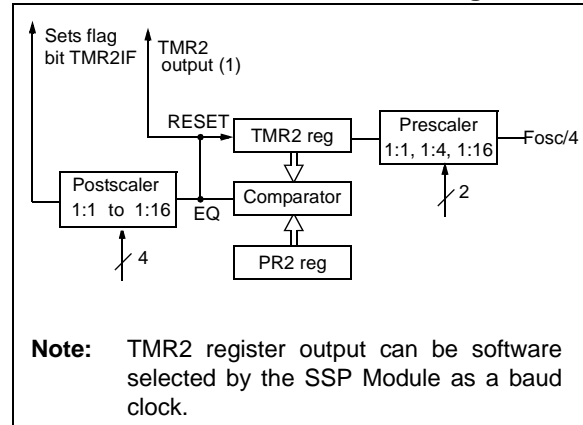
## 7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

## 7.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

**FIGURE 7-1: Timer2 Block Diagram**



**TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh,10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
11h	TMR2	Timer2 register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

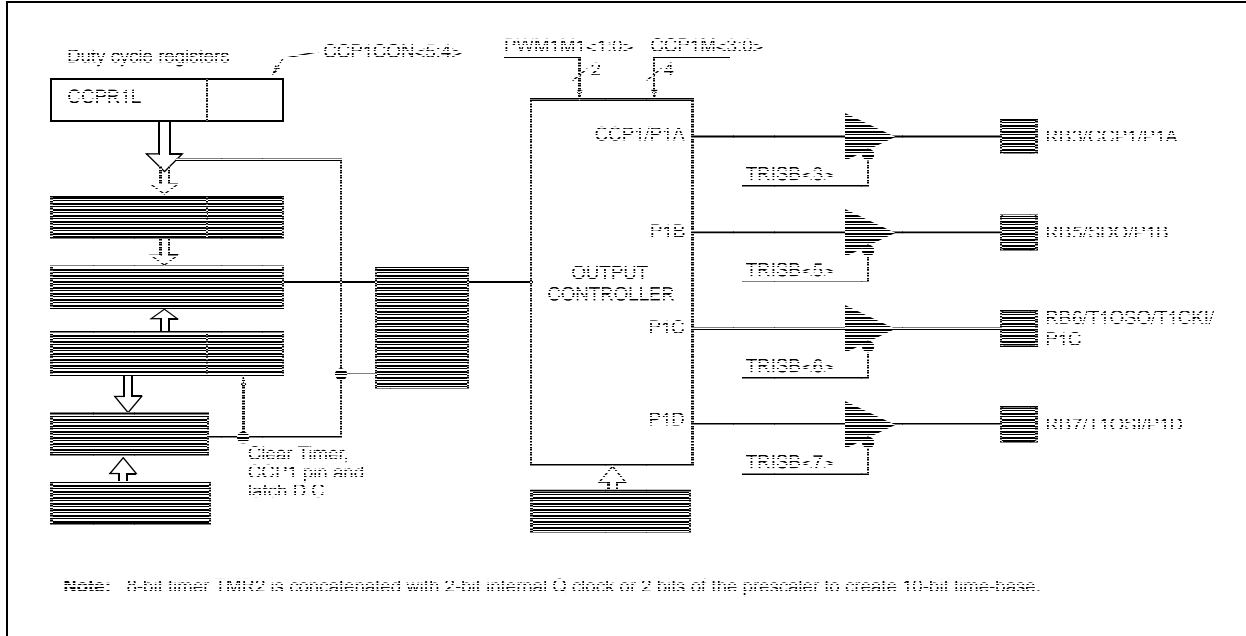
Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.

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## 8.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the ECCP module produces up to a 10-bit resolution PWM output. Figure 8-3 shows the simplified PWM block diagram.

**FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM**



### 8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM PERIOD} = \frac{[(\text{PR2}) + 1] \cdot 4 \cdot \text{TOSC}}{(\text{TMR2 PRESCALE VALUE})}$$

PWM frequency is defined as  $1 / [\text{PWM period}]$ .

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

**Note:** The Timer2 postscaler (see Section 7.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

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## 9.2 MSSP I<sup>2</sup>C Operation

The MSSP module in I<sup>2</sup>C mode fully implements all master and slave functions (including general call support) and provides interrupts on START and STOP bits in hardware to determine when the bus is free (multi-master function). The MSSP module implements the Standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used to transfer data. They are the SCL pin (clock) and the SDA pin (data). The MSSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>). The SCL and SDA pins are "glitch" filtered when operating as inputs. This filter functions in both the 100 kHz and 400 kHz modes. When these pins operate as outputs in the 100 kHz mode, there is a slow rate control of the pin that is independent of device frequency.

Before selecting any I<sup>2</sup>C mode, the SCL and SDA pins must be programmed as inputs by setting the appropriate TRIS bits. This allows the MSSP module to configure and drive the I/O pins as required by the I<sup>2</sup>C protocol.

The MSSP module has six registers for I<sup>2</sup>C operation. They are listed below.

- SSP Control Register (SSPCON)
- SSP Control Register2 (SSPCON2)
- SSP STATUS Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows for control of the I<sup>2</sup>C operation. Four mode selection bits (SSPCON<3:0>) configure the MSSP as any one of the following I<sup>2</sup>C modes:

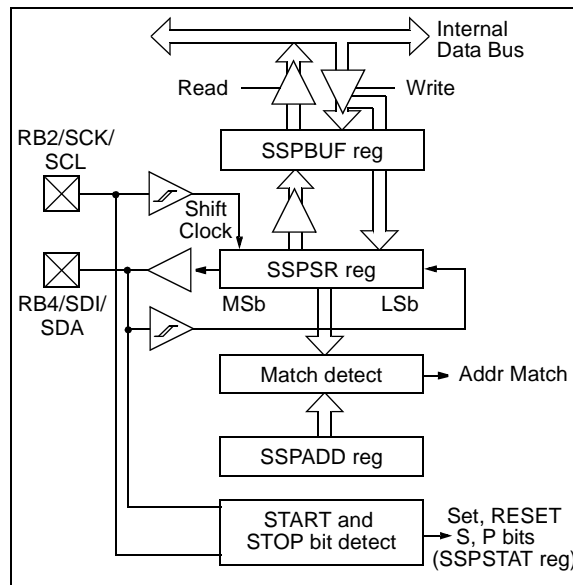
- I<sup>2</sup>C Slave mode (7-bit address)
- I<sup>2</sup>C Slave mode (10-bit address)
- I<sup>2</sup>C Master mode  
SCL Freq = FOSC / [4 • (SSPADD + 1)]
- I<sup>2</sup>C Slave mode with START and STOP interrupts (7-bit address)
- I<sup>2</sup>C Slave mode with START and STOP interrupts (10-bit address)
- Firmware Controlled Master mode

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START (S) or STOP (P) bit. It specifies whether the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer.

SSPBUF is the register to which the transfer data is written, and from which the transfer data is read. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled, buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is

transferred from the SSPSR register to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read a receiver overflow occurs, in which case, the SSPOV bit (SSPCON<6>) is set and the byte in the SSPSR is lost.

**FIGURE 9-7: I<sup>2</sup>C SLAVE MODE BLOCK DIAGRAM**



### 9.2.1 UPWARD COMPATIBILITY WITH SSP MODULE

The MSSP module includes three SSP modes of operation to maintain upward compatibility with the SSP module. These modes are:

- Firmware controlled Master mode (slave idle)
- 7-bit Slave mode with START and STOP condition interrupts.
- 10-bit Slave mode with START and STOP condition interrupts.

The firmware controlled Master mode enables the START and STOP condition interrupts but all other I<sup>2</sup>C functions are generated through firmware including:

- Generating the START and STOP conditions
- Generating the SCL clock
- Supplying the SDA bits in the proper time and phase relationship to the SCL signal.

In firmware controlled Master mode, the SCL and SDA lines are manipulated by clearing and setting the corresponding TRIS bits. The output level is always low irrespective of the value(s) in the PORT register. A '1' is output by setting the TRIS bit and a '0' is output by clearing the TRIS bit

The 7-bit and 10-bit Slave modes with START and STOP condition interrupts operate identically to the MSSP Slave modes except that START and STOP conditions generate SSPIF interrupts.



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## 9.2.3 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I<sup>2</sup>C bus is such that the first byte after the START condition usually determines which device will be the slave addressed by the master. The exception is the general call address, which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I<sup>2</sup>C protocol. It consists of all 0's with R/W = 0

The general call address is recognized when the General Call Enable bit (GCEN) is set (SSPCON2<7> is set). Following a START bit detect, eight bits are shifted

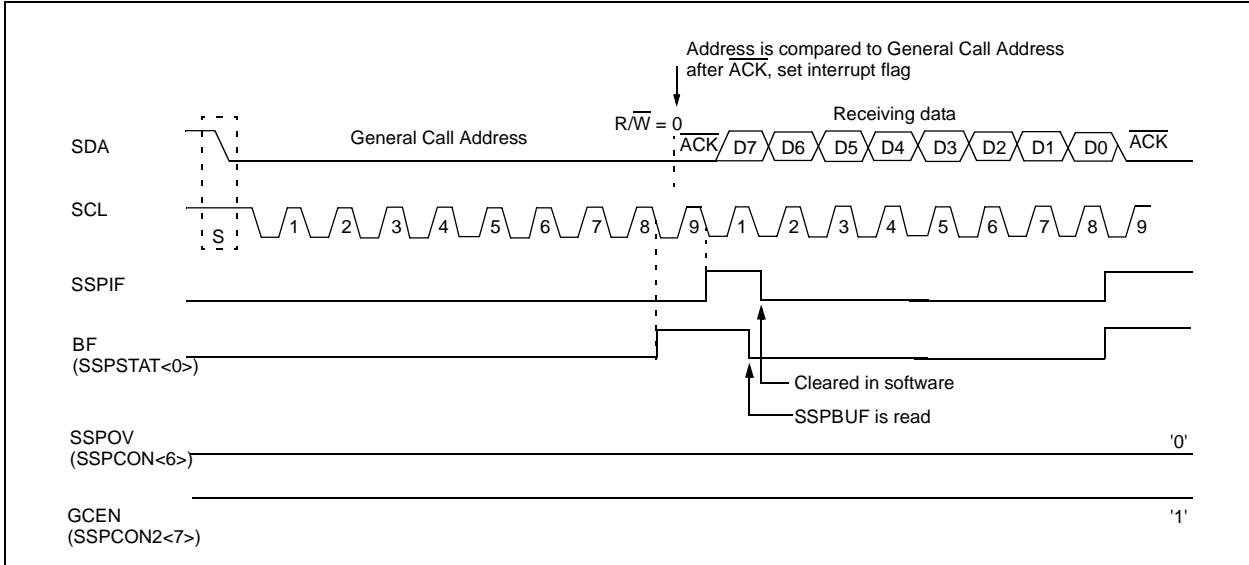
into the SSPSR, and the address is compared against SSPADD. It is also compared to the general call address, fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag is set (eighth bit), and on the falling edge of the ninth bit ( $\overline{\text{ACK}}$  bit), the SSPIF flag is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF to determine if the address was device specific or a general call address.

If the general call address is sampled with GCEN set and the slave configured in 10-bit Address mode, the second half of the address is not necessary. The UA bit will not be set and the slave will begin receiving data after the Acknowledge (Figure 9-12).

**FIGURE 9-12: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7- OR 10-BIT MODE)**



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## 9.2.11 I<sup>2</sup>C MASTER MODE REPEATED START CONDITION TIMING

A Repeated START condition occurs when the RSEN bit (SSPCON2<1>) is set high while the I<sup>2</sup>C module is in the idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the baud rate generator is loaded with the contents of SSPADD<6:0> and begins counting. The SDA pin is released (brought high) for one baud rate generator count (TBRG). When the baud rate generator times out, if SDA is sampled high, the SCL pin will be de-asserted (brought high). When SCL is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG period. This action is then followed by assertion of the SDA pin (SDA is low) for one TBRG period while SCL is high. As soon as a START condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. Following this, the baud rate generator is reloaded with the contents of SSPAD<6:0> and begins counting. When the BRG times out a third time, the RSEN bit in the SSPCON2 register is automatically cleared and SCL is pulled low. The SSPIF flag is set, which indicates the Restart sequence is complete.

Immediately following the SSPIF bit transition to true, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then perform one of the following:

- Transmit an additional eight bits of address (if the user transmitted the first half of a 10-bit address with R/W = 0),
- Transmit eight bits of data (if the user transmitted a 7-bit address with R/W = 0), or
- Receive eight bits of data (if the user transmitted either the first half of a 10-bit address or a 7-bit address with R/W = 1).

### 9.2.11.1 WCOL STATUS FLAG

If the user writes the SSPBUF when a Repeated START sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

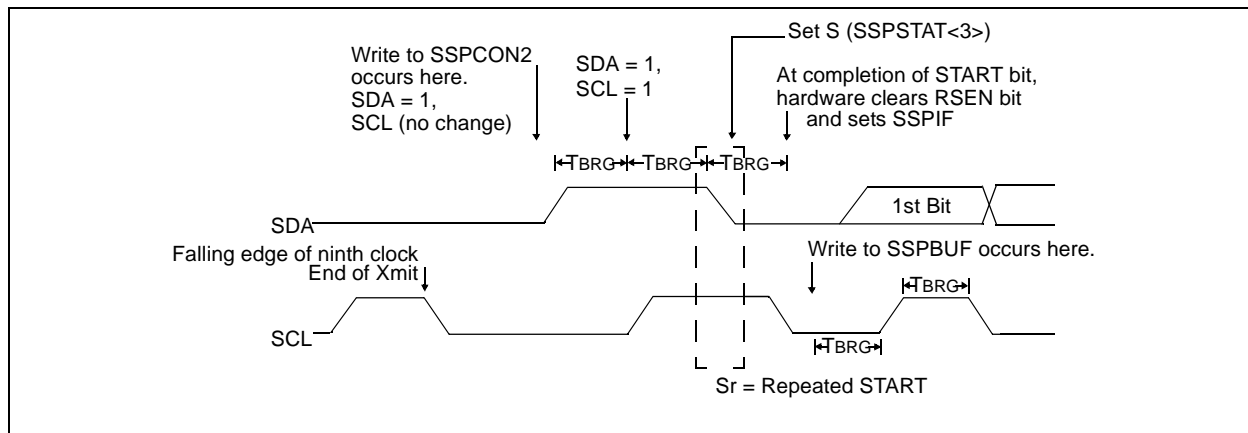
**Note:** Because queuing of events is not allowed, writing of the lower five bits of SSPCON2 is disabled until the Repeated START condition is complete.

**Note 1:** If RSEN is set while another event is in progress, it will not take effect. Queuing of events is not allowed.

**2:** A bus collision during the Repeated START condition occurs if either of the following is true:

- SDA is sampled low when SCL goes from low to high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

**FIGURE 9-17: REPEAT START CONDITION WAVEFORM**



## 9.2.14 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge sequence enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit ACKDT (SSPCON2<5>) is presented on the SDA pin. If the user wishes to generate an Acknowledge (ACK), then the ACKDT bit should be cleared. Otherwise, the user should set the ACKDT bit (NACK) before starting an Acknowledge sequence. The baud rate generator is then loaded from SSPADD<6:0> and counts for one rollover period (TBRG). The SCL pin is then de-asserted (pulled high). When the SCL pin is sampled high (clock

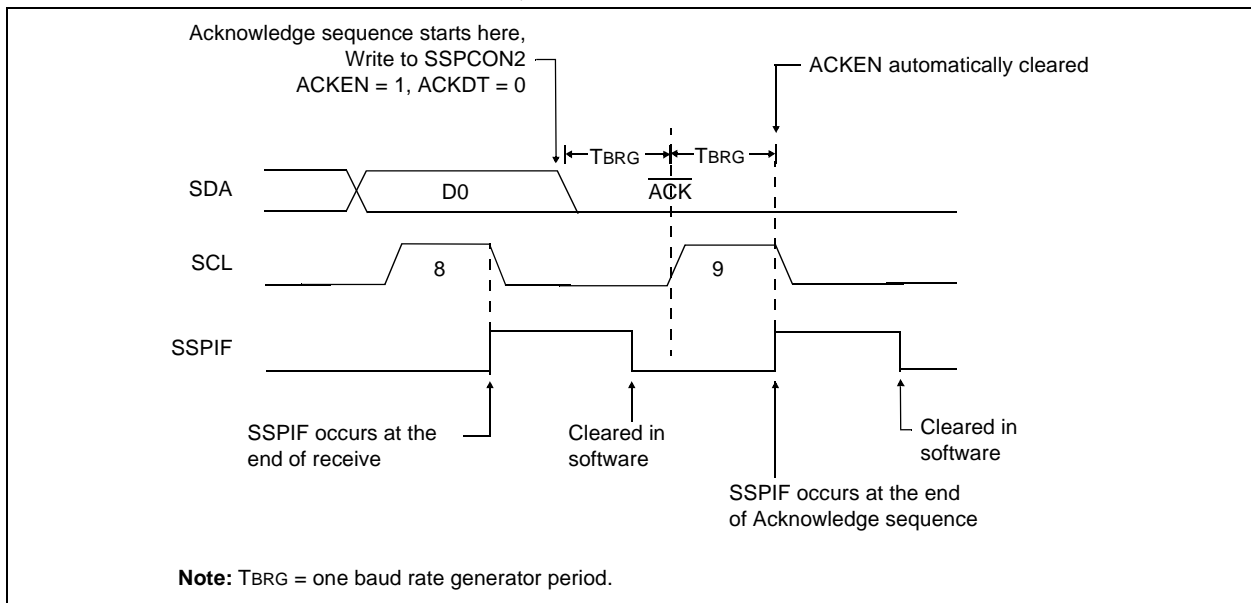
arbitration), the baud rate generator is reloaded and counts for another TBRG. At the completion of the TBRG period, the following events occur (see Figure 9-20):

- The SCL pin is pulled low.
- The ACKEN bit is automatically cleared.
- The baud rate generator is turned off.
- The MSSP module goes into IDLE mode.

### 9.2.14.1 WCOL STATUS FLAG

If the user writes the SSPBUF when an Acknowledge sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

**FIGURE 9-20: ACKNOWLEDGE SEQUENCE WAVEFORM**



## 11.7 Use of the ECCP Trigger

An A/D conversion can be started by the “special event trigger” of the CCP module. This requires that the CCP1M<3:0> bits be programmed as 1011b and that the A/D module is enabled (ADON is set). When the trigger occurs, the GO/DONE bit will be set on Q2 to start the A/D conversion and the Timer1 counter will be reset to zero. Timer1 is RESET to automatically repeat the A/D conversion cycle, with minimal software overhead (moving the ADRESH and ADRESL to the desired location). The appropriate analog input channel must be selected before the “special event trigger” sets the GO/DONE bit (starts a conversion cycle).

If the A/D module is not enabled (ADON is cleared), then the “special event trigger” will be ignored by the A/D module, but will still RESET the Timer1 counter.

## 11.8 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRESH and ADRESL registers are not modified. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

## 11.9 Faster Conversion - Lower Resolution Trade-off

Not all applications require a result with 12 bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the A/D module may be halted by clearing the GO/DONE bit after the desired number of bits in the result have been converted. Once the GO/DONE bit has been cleared, all of the remaining A/D result bits are '0'. The equation to determine the time before the GO/DONE bit can be switched is as follows:

$$\text{Conversion time} = (N+1)T_{AD}$$

Where: N = number of bits of resolution required, and 1T<sub>AD</sub> is the amplifier settling time.

Since T<sub>AD</sub> is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D GO/DONE bit may be cleared. Table 11-4 shows a comparison of time required for a conversion with 4 bits of resolution, versus the normal 12-bit resolution conversion. The example is for devices operating at 20 MHz. The A/D clock is programmed for 32 T<sub>osc</sub>.

### EXAMPLE 11-4: 4-BIT vs. 12-BIT CONVERSION TIME Example

4-Bit Example:

$$\begin{aligned}\text{Conversion Time} &= (N + 1) T_{AD} \\ &= (4 + 1) T_{AD} \\ &= (5)(1.6 \mu\text{S}) \\ &= 8 \mu\text{S}\end{aligned}$$

12-Bit Example:

$$\begin{aligned}\text{Conversion Time} &= (N + 1) T_{AD} \\ &= (12 + 1) T_{AD} \\ &= (13)(1.6 \mu\text{S}) \\ &= 20.8 \mu\text{S}\end{aligned}$$

## 14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

## 14.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

## 14.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

## 14.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

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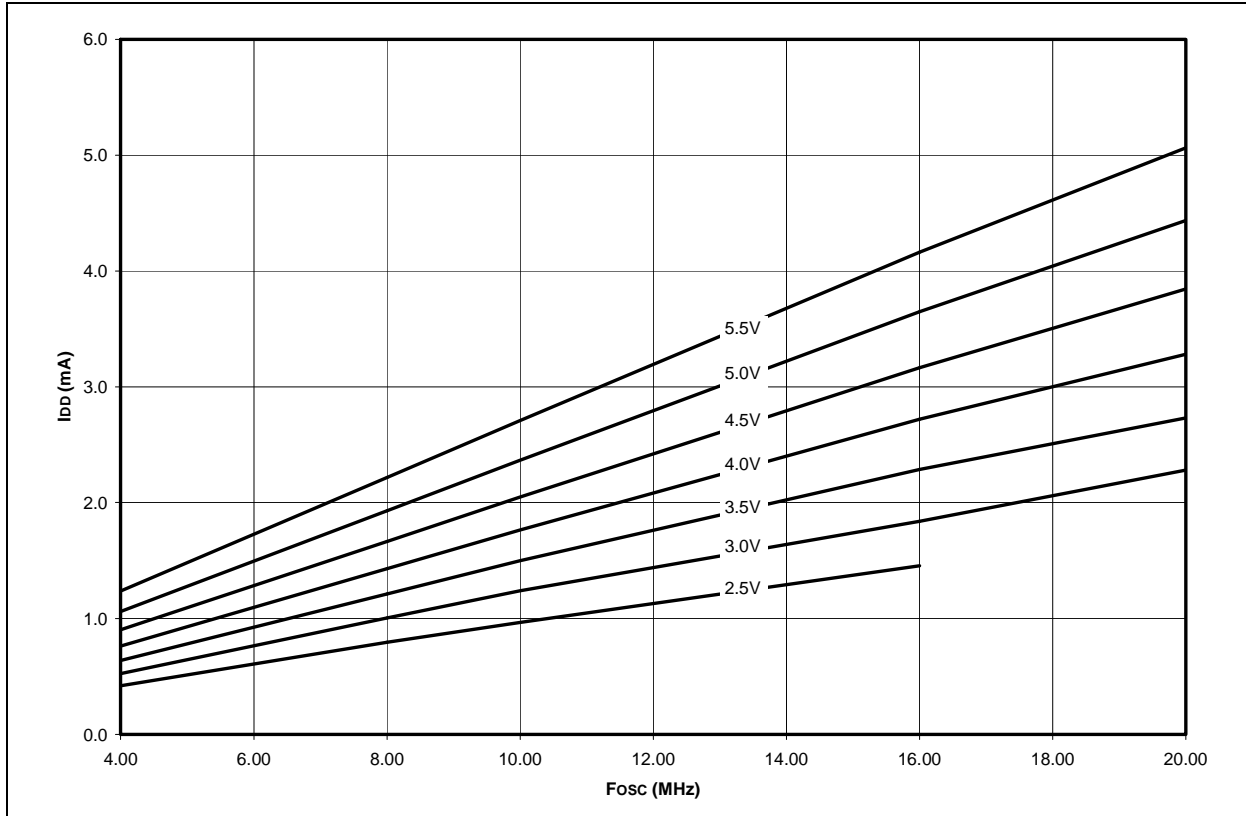
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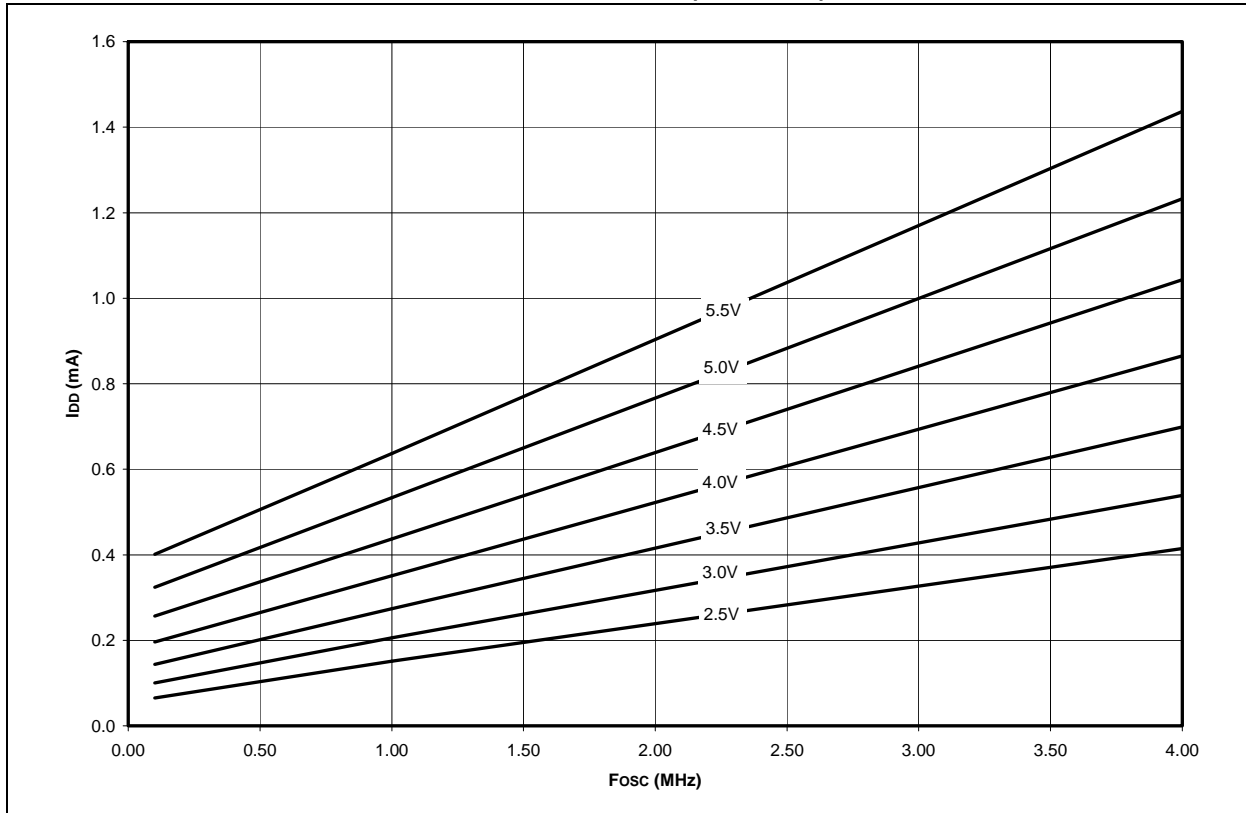
NOTES:

# PIC16C717/770/771

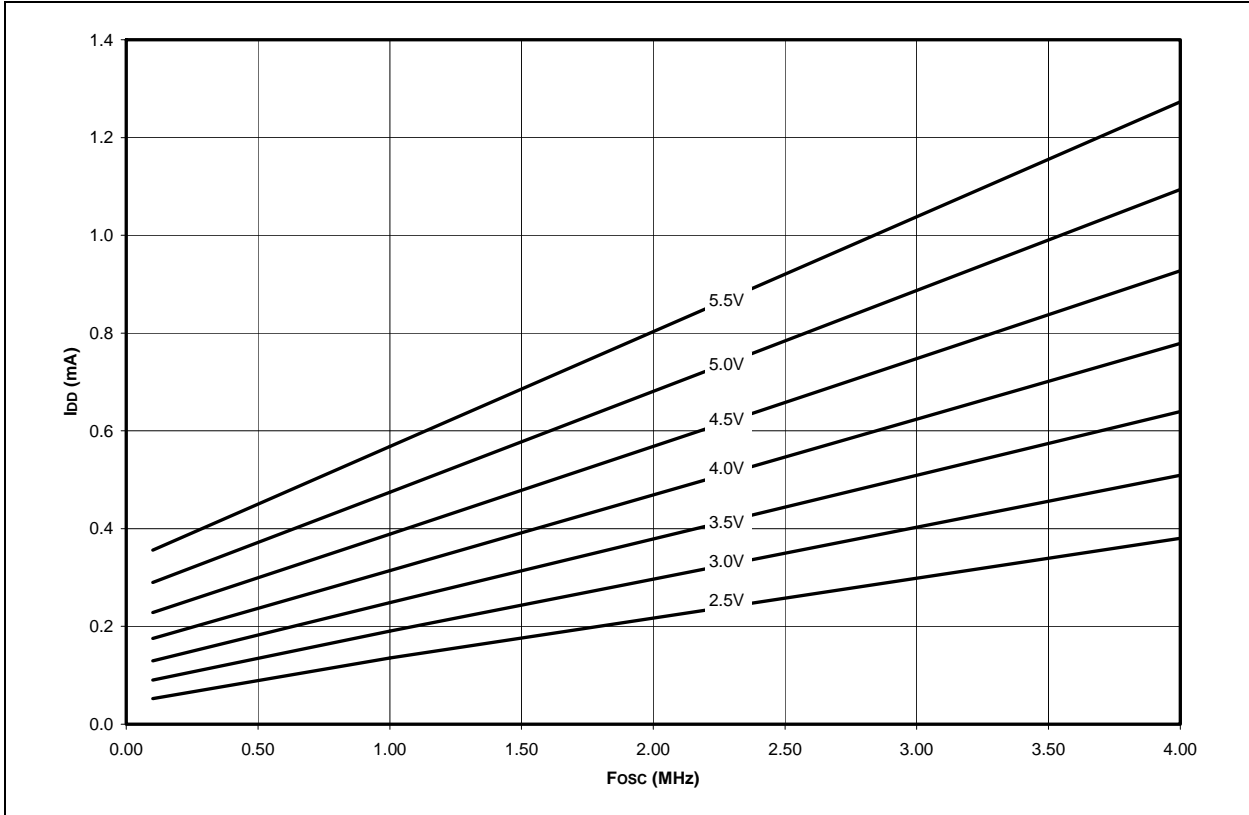
**FIGURE 16-2: TYPICAL  $I_{DD}$  VS.  $F_{osc}$  OVER  $V_{DD}$  (HS MODE)**



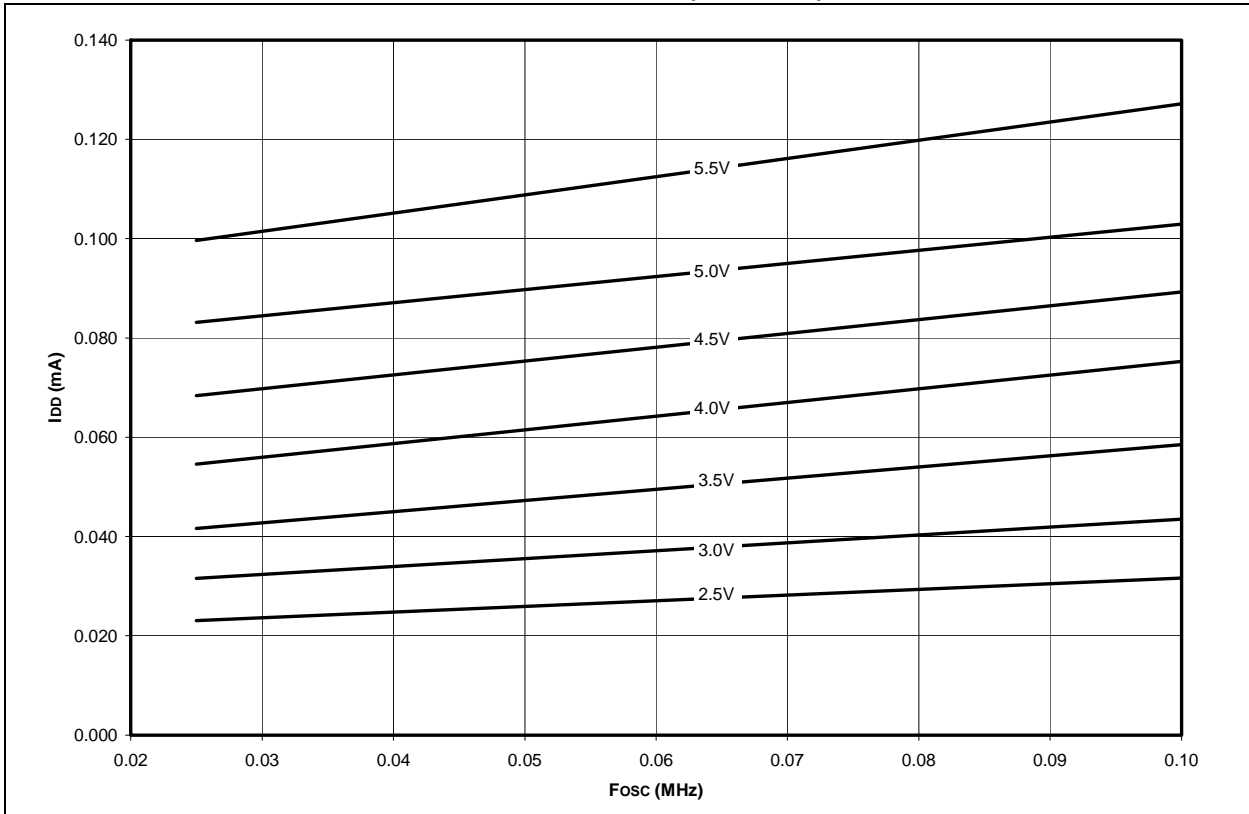
**FIGURE 16-3: MAXIMUM  $I_{DD}$  VS.  $F_{osc}$  OVER  $V_{DD}$  (XT MODE)**



**FIGURE 16-4: TYPICAL  $I_{DD}$  VS.  $F_{osc}$  OVER  $V_{DD}$  (XT MODE)**



**FIGURE 16-5: MAXIMUM  $I_{DD}$  VS.  $F_{osc}$  OVER  $V_{DD}$  (LP MODE)**





# PIC16C717/770/771

FIGURE 16-6: TYPICAL  $I_{DD}$  VS.  $F_{osc}$  OVER  $V_{DD}$  (LP MODE)

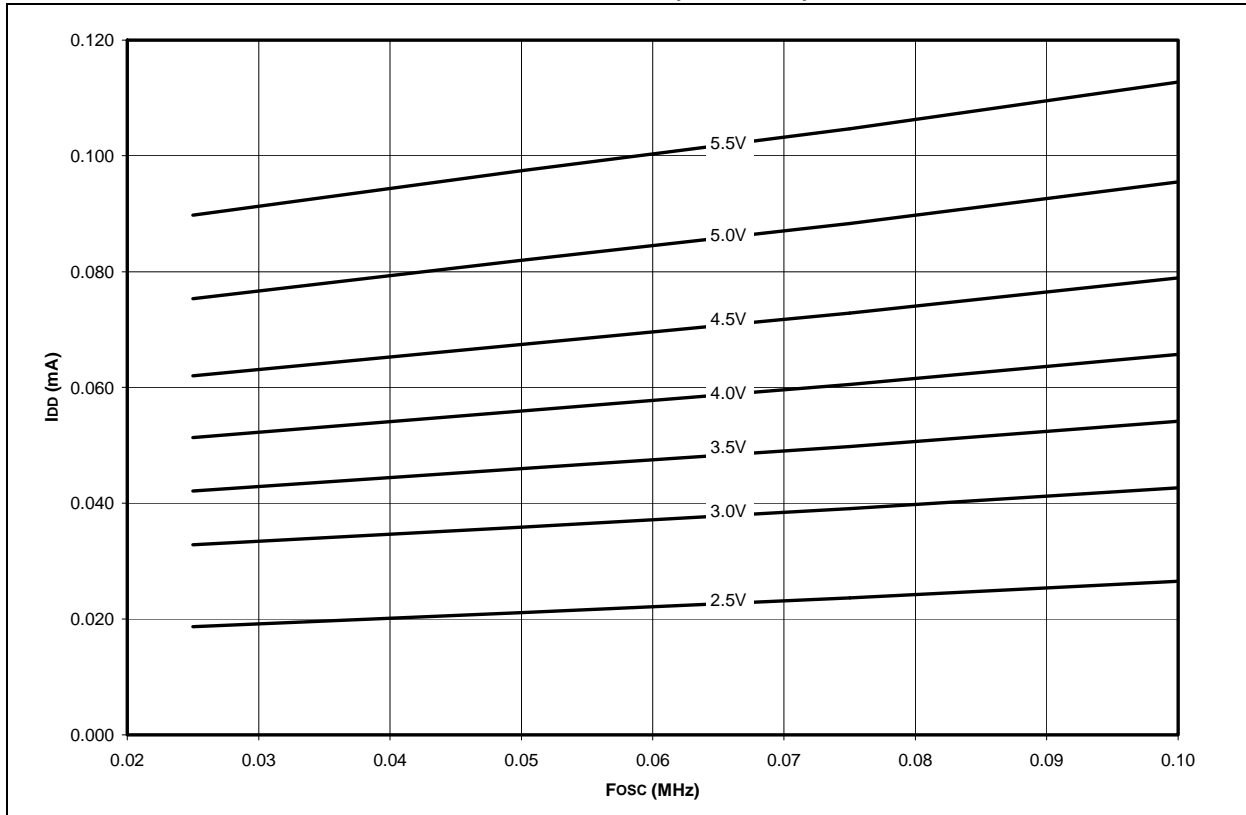
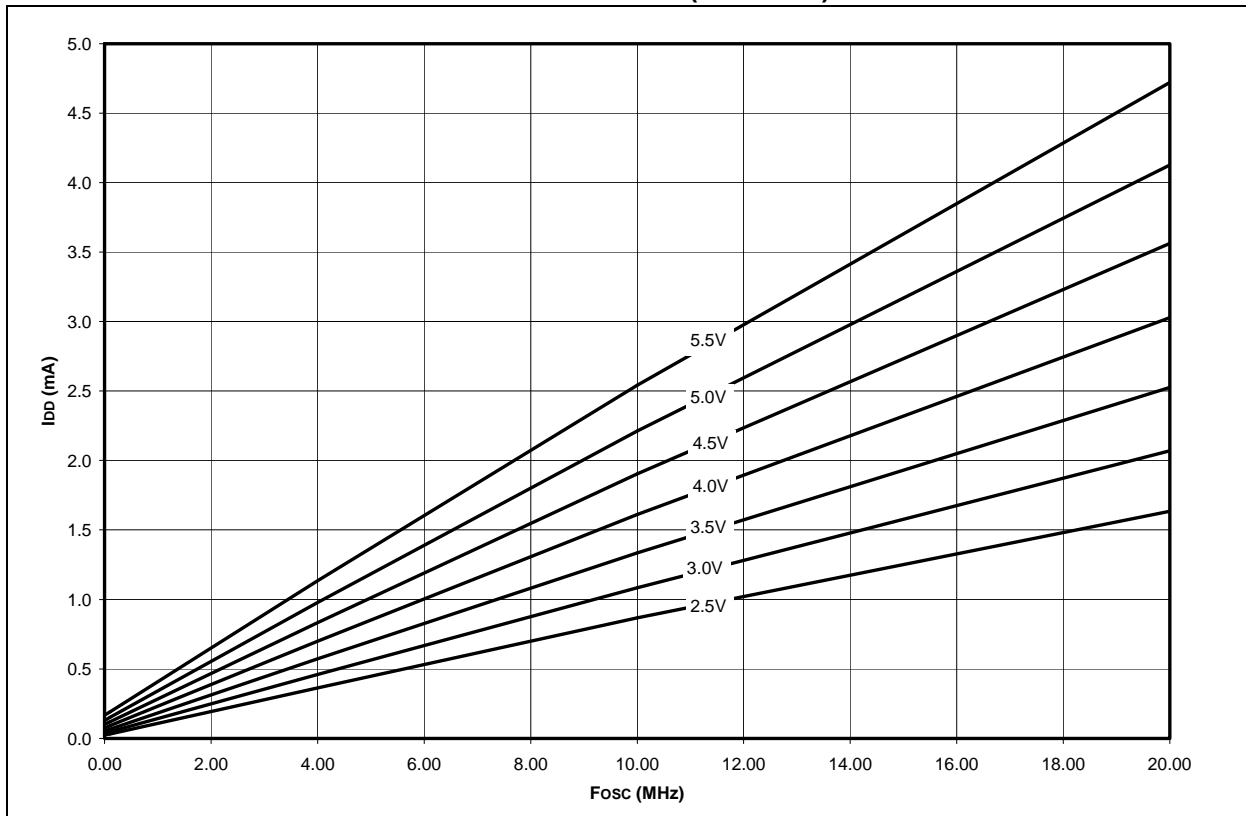
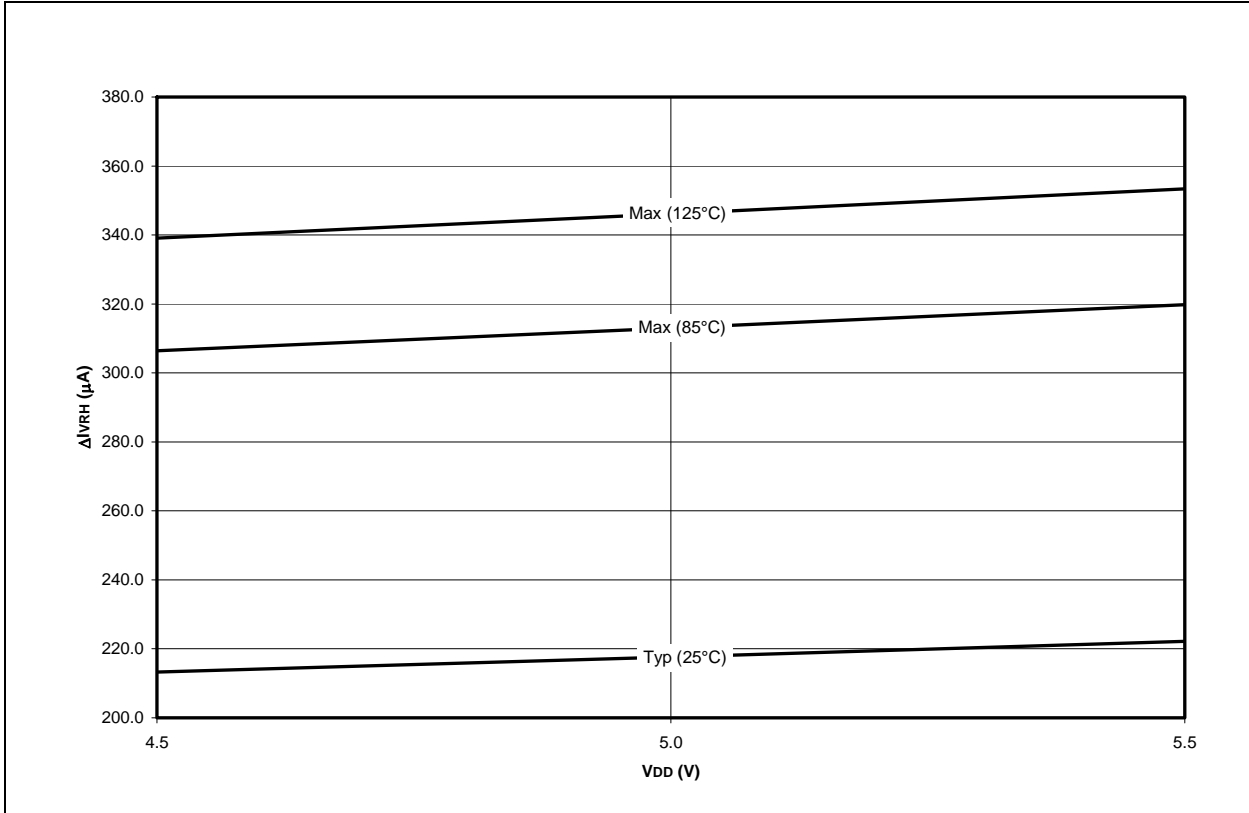


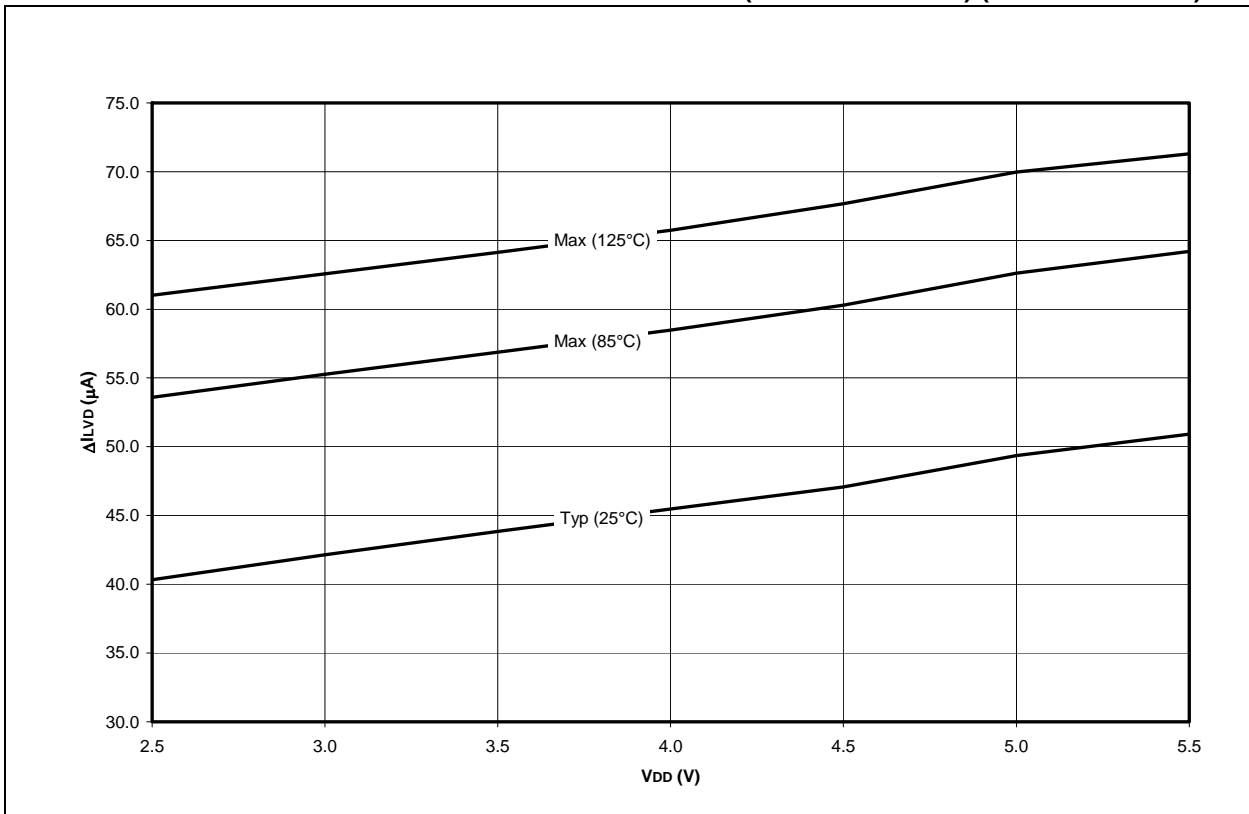
FIGURE 16-7: MAXIMUM  $I_{DD}$  VS.  $F_{osc}$  OVER  $V_{DD}$  (EC MODE)



**FIGURE 16-22: TYPICAL AND MAXIMUM  $\Delta I_{VRH}$  VS.  $V_{DD}$  (-40°C TO +125°C)**



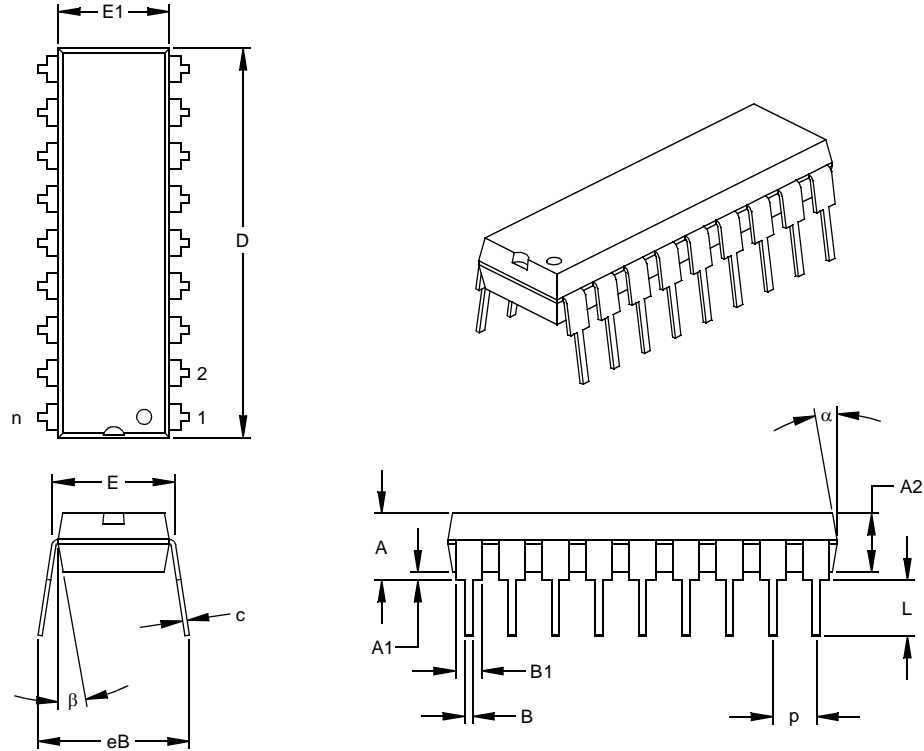
**FIGURE 16-23: TYPICAL AND MAXIMUM  $\Delta I_{LVD}$  VS.  $V_{DD}$  (-40°C TO +125°C) (LVD TRIP = 3.0V)**



# PIC16C717/770/771

## 17.2 18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



Dimension	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015				0.38	
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

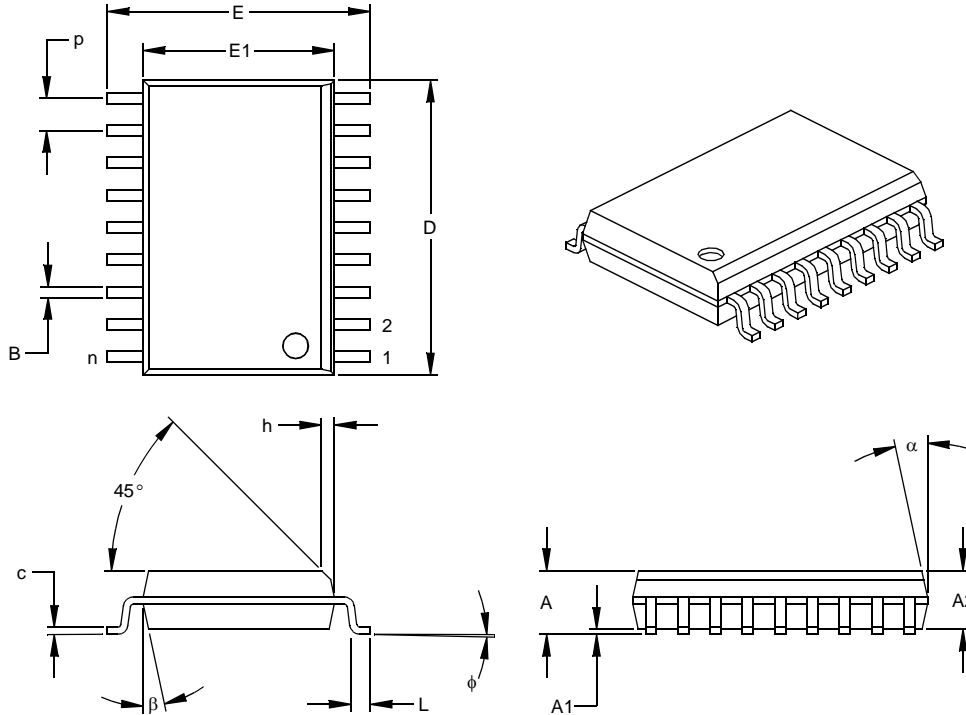
\* Controlling Parameter  
 § Significant Characteristic

Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-001  
 Drawing No. C04-007

# PIC16C717/770/771

## 17.4 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter  
§ Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-051

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