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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c770-so

NOTES:

2.2.2.6 PIE2 REGISTER

This register contains the individual enable bits for the SSP bus collision and low voltage detect interrupts.

REGISTER 2-6: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (PIE2: 8Dh)

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
LVDIE	—	—	—	BCLIE	—	—	—
bit 7							bit 0

bit 7 **LVDIE:** Low Voltage Detect Interrupt Enable bit
1 = LVD Interrupt is enabled
0 = LVD Interrupt is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **BCLIE:** Bus Collision Interrupt Enable bit
1 = Bus Collision interrupt is enabled
0 = Bus Collision interrupt is disabled

bit 2-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

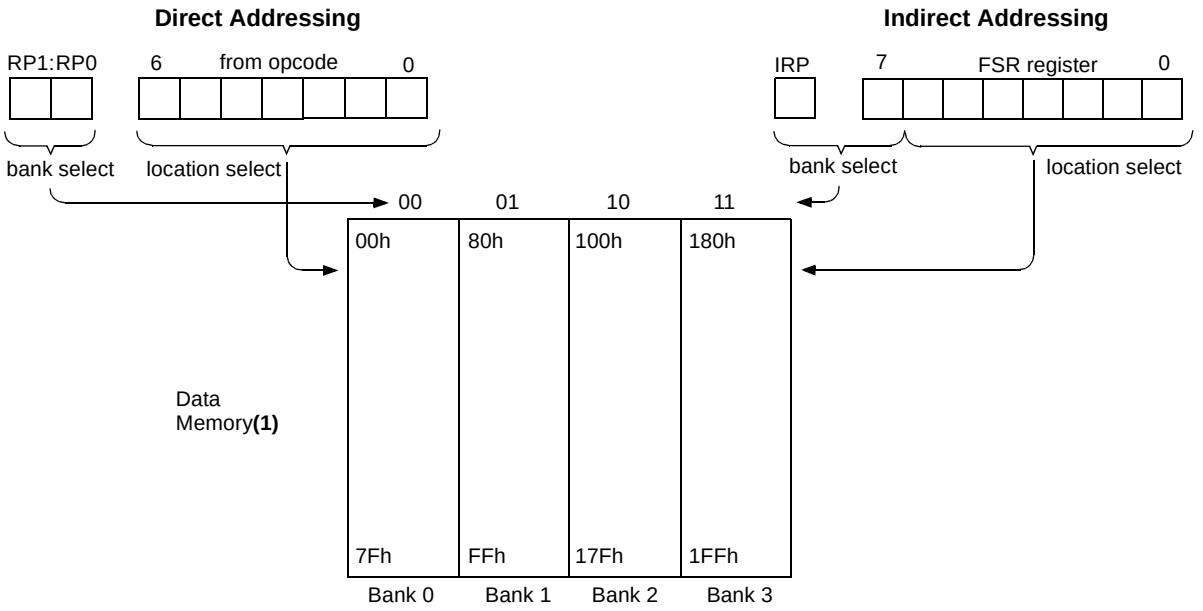
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: How to Clear RAM Using Indirect Addressing

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;  to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;NO, clear next
CONTINUE
        :               ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-5.

FIGURE 2-5: DIRECT/INDIRECT ADDRESSING

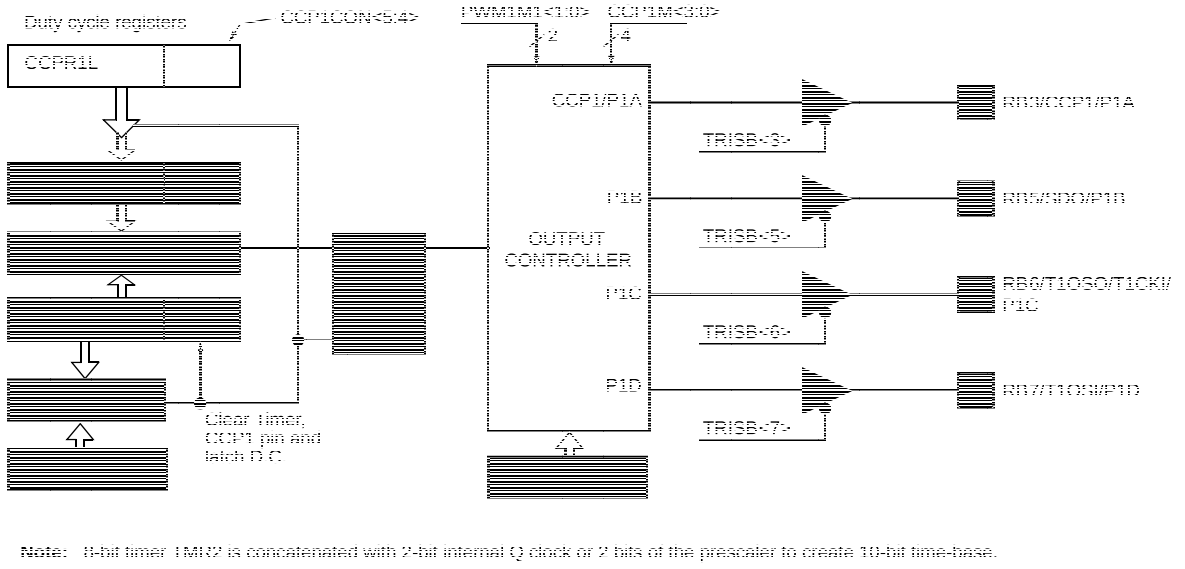


Note 1: For register file map detail see Figure 2-3.

8.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the ECCP module produces up to a 10-bit resolution PWM output. Figure 8-3 shows the simplified PWM block diagram.

FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM PERIOD} = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (\text{TMR2 PRESCALE VALUE})$$

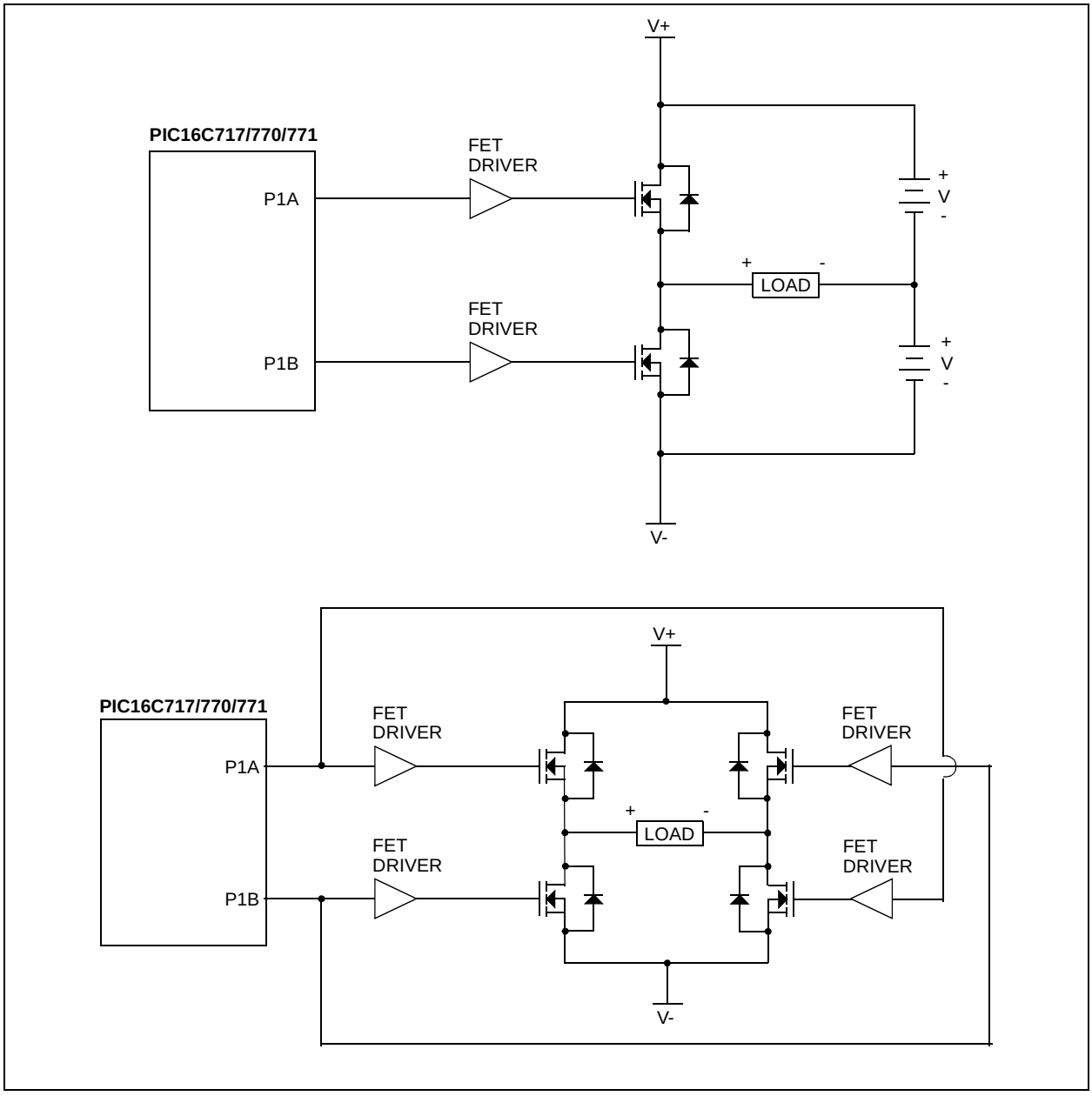
PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 7.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

FIGURE 8-7: EXAMPLE OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



Note that in the Full-Bridge Output mode, the ECCP module does not provide any deadband delay. In general, since only one output is modulated at a time, deadband delay is not required. However, there is a situation where a deadband delay might be required. This situation occurs when all of the following conditions are true:

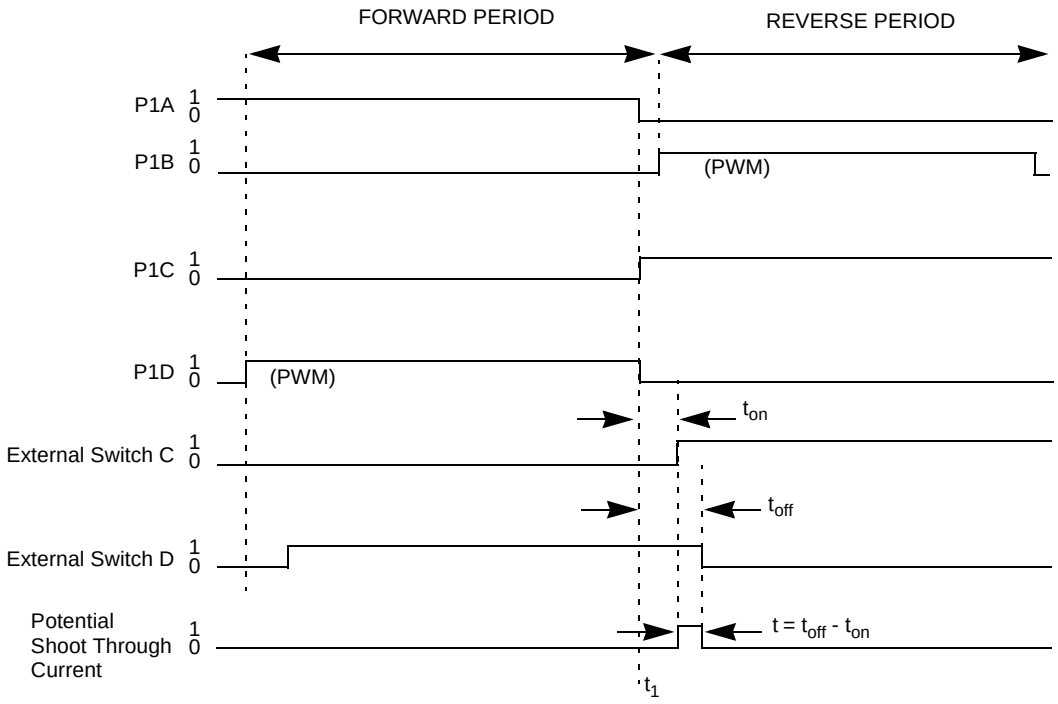
1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
2. The turn off time of the power switch, including the power device and driver circuit, is greater than turn on time.

Figure 8-11 shows an example, where the PWM direction changes from forward to reverse at a near 100% duty cycle. At time t1, the output P1A and P1D become inactive, while output P1C becomes active. In this example, since the turn off time of the power devices is longer than the turn on time, a shoot-through current flows through the power devices, QB and QD, for the duration of $t = t_{off} - t_{on}$. The same phenomenon will occur to power devices, QC and QB, for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for the user's application, one of the following requirements must be met:

1. Avoid changing PWM output direction at or near 100% duty cycle.
2. Use switch drivers that compensate for the slow turn off of the power devices. The total turn off time (t_{off}) of the power device and the driver must be less than the turn on time (t_{on}).

FIGURE 8-11: PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE



Note 1: All signals are shown as active high.

2: t_{on} is the turn on delay of power switch and driver.

3: t_{off} is the turn off delay of power switch and driver.

8.3.7 SYSTEM IMPLEMENTATION

When the ECCP module is used in the PWM mode, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins. When the microcontroller powers up, all of the I/O pins are in the high-impedance state. The external pull-up and pull-down resistors must keep the power switch devices in the off state until the microcontroller drives the I/O pins with the proper signal levels, or activates the PWM output(s).

8.3.8 START-UP CONSIDERATIONS

Prior to enabling the PWM outputs, the P1A, P1B, P1C and P1D latches may not be in the proper states. Enabling the TRISB bits for output at the same time with the CCP module may cause damage to the power switch devices. The CCP1 module must be enabled in the proper Output mode with the TRISB bits enabled as inputs. Once the CCP1 completes a full PWM cycle, the P1A, P1B, P1C and P1D output latches are properly initialized. At this time, the TRISB bits can be enabled for outputs to start driving the power switch devices. The completion of a full PWM cycle is indicated by the TMR2IF bit going from a '0' to a '1'.

8.3.9 SET UP FOR PWM OPERATION

The following steps should be taken when configuring the ECCP module for PWM operation:

1. Configure the PWM module:
   a) Disable the CCP1/P1A, P1B, P1C and/or P1D outputs by setting the respective TRISB bits.
   b) Set the PWM period by loading the PR2 register.
   c) Set the PWM duty cycle by loading the CCPR1L register and CCP1CON<5:4> bits.
   d) Configure the ECCP module for the desired PWM operation by loading the CCP1CON register. With the CCP1M<3:0> bits select the active high/low levels for each PWM output. With the PWM1M<1:0> bits select one of the available Output modes: Single, Half-Bridge, Full-Bridge, Forward or Full-Bridge Reverse.
   e) For Half-Bridge Output mode, set the dead-band delay by loading the P1DEL register.
2. Configure and start TMR2:
   a) Clear the TMR2 interrupt flag bit by clearing the TMR2IF bit in the PIR1 register.
   b) Set the TMR2 prescale value by loading the T2CKPS<1:0> bits in the T2CON register.
   c) Enable Timer2 by setting the TMR2ON bit in the T2CON register.
3. Enable PWM outputs after a new cycle has started:
   a) Wait until TMR2 overflows (TMR2IF bit becomes a ’1’). The new PWM cycle begins here.
   b) Enable the CCP1/P1A, P1B, P1C and/or P1D pin outputs by clearing the respective TRISB bits.

TABLE 8-3: REGISTERS ASSOCIATED WITH PWM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 register								0000 0000	0000 0000
92h	PR2	Timer2 period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	PWM1M1	PWM1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
97h	P1DEL	PWM1 Delay value								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by ECCP module in PWM mode.

9.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI™)
- Inter-Integrated Circuit (I^2C™)

For more information about these SSP modes see Section 15 of the *PIC Mid-Range MCU Family Reference Manual (DS33023)*.

9.2.2 SLAVE MODE

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge ($\overline{ACK}$) pulse. Then, it loads the SSPBUF register with the received value currently in the SSPSR register.

Any combination of the following conditions will cause the MSSP module to generate a NACK pulse in lieu of the $\overline{ACK}$ pulse:

a) The buffer full bit BF (SSPSTAT<0>) is set before the transfer is received.

b) The overflow bit SSPOV (SSPCON<6>) is set before the transfer is received.

If the BF bit is set, the SSPSR register value is not loaded into the SSPBUF. However, both the SSPIF and SSPOV bits are set. Table 9-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. The BF flag bit is cleared by reading the SSPBUF register. The SSPOV flag bit is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I^2C specification as well as the requirements of the MSSP module are shown in timing parameters #100 and #101 of the Electrical Specifications.

9.2.2.1 7-BIT ADDRESSING

Once the MSSP module has been enabled (SSPEN=1), the slave module waits for a START condition to occur. Following the START condition, eight bits are shifted into the SSPSR register. All incoming bits are sampled on the rising edge of the clock (SCL) line. The received address (register SSPSR<7:1>) is compared to the stored address (register SSPADD<7:1>). SSPSR<0> is the R/$\overline{W}$ bit and is not considered in the comparison. Comparison is made on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

a) The SSPSR register value is transferred to the SSPBUF register on the falling edge of the eighth SCL pulse.

b) The buffer full bit; BF is set on the falling edge of the eighth SCL pulse.

c) An $\overline{ACK}$ pulse is generated during the ninth clock cycle.

d) SSP interrupt flag bit; SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

9.2.2.2 10-BIT ADDRESSING

In 10-bit mode, the basic receive and transmit operations are the same as in the 7-bit mode. However, the criteria for address match are more complex.

Two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify that this is a 10-bit address. The LSb of the first received address byte is the R/$\overline{W}$ bit, which must be zero, specifying a write so the slave device will receive the second address byte. For a 10-bit address, the first byte equals '`11110 A9 A8 0`', where A9 and A8 are the two MSbs of the address. The sequence of events for a 10-bit address is as follows, with steps 7 through 9 applicable only to the slave-transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
5. Update the SSPADD register with the first (high) byte of Address. This will clear bit UA and release the SCL line.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive Repeated START condition.
8. Receive first (high) byte of Address with R/$\overline{W}$ bit set to 1 (bits SSPIF and BF are set). This also puts the MSSP module in the Slave-transmit mode.
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

Note:	Following the Repeated START condition (step 7) in 10-bit mode, the user only needs to match the first 7-bit address. The user does not update the SSPADD for the second half of the address.

9.2.12 I²C MASTER MODE TRANSMISSION

In Master-transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains seven bits of address data and the Read/Write (R/$\overline{W}$) bit. In this case, the R/$\overline{W}$ bit will be logic '0'. Subsequent serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

Transmission of a data byte, a 7-bit address, or either half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the buffer full flag (BF) and allow the baud rate generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time spec). SCL is held low for one baud rate generator roll over count (TBRG). Data should be valid before SCL is released high (see data setup time spec). When the SCL pin is released high, it is held that way for TBRG, the data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an $\overline{ACK}$ bit during the ninth bit time. The status of $\overline{ACK}$ is read into the ACKDT on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge status bit (ACKSTAT) is cleared. Otherwise, the bit is set. The SSPIF is set on the falling edge of the ninth clock, and the master clock (baud rate generator) is suspended until the next data byte is loaded into the SSPBUF leaving SCL low and SDA unchanged (Figure 9-18).

A typical transmit sequence would go as follows:

a) The user generates a START Condition by setting the START enable bit (SEN) in SSPCON2.
b) SSPIF is set at the completion of the START sequence.
c) The user resets the SSPIF bit and loads the SSPBUF with seven bits of address plus R/$\overline{W}$ bit to transmit.
d) Address and R/$\overline{W}$ is shifted out the SDA pin until all eight bits are transmitted.
e) The MSSP Module shifts in the $\overline{ACK}$ bit from the slave device, and writes its value into the SSPCON2 register (SSPCON2<6>).
f) The module generates an interrupt at the end of the ninth clock cycle by setting SSPIF.
g) The user resets the SSPIF bit and loads the SSPBUF with eight bits of data.
h) DATA is shifted out the SDA pin until all eight bits are transmitted.
i) The MSSP Module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
j) The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
k) The user resets the SSPIF bit and generates a STOP condition by setting the STOP enable bit PEN in SSPCON2.
l) SSPIF is set when the STOP condition is complete.

9.2.12.1 BF STATUS FLAG

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all eight bits are shifted out.

9.2.12.2 WCOL STATUS FLAG

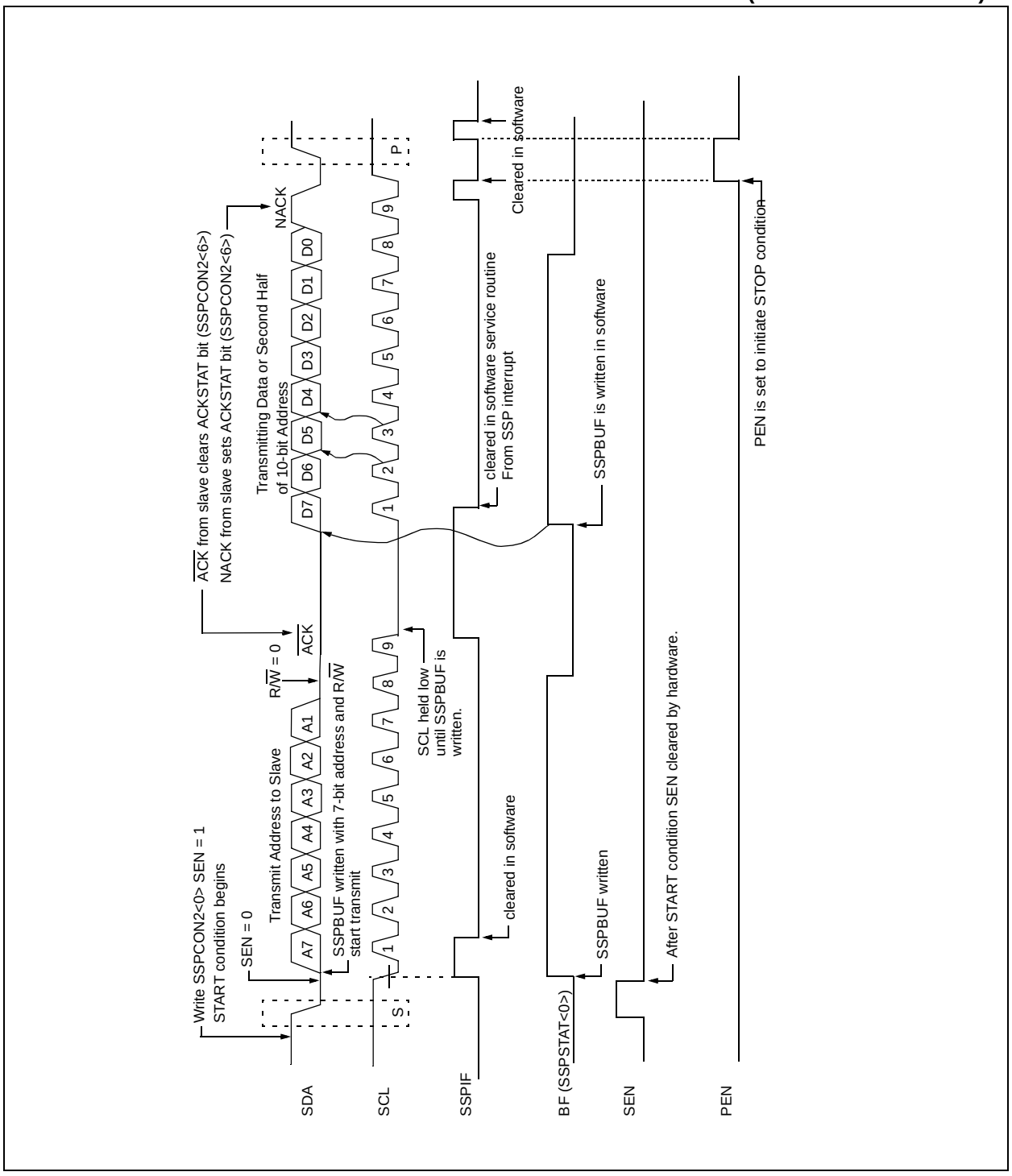
If the user writes the SSPBUF when a transmit is already in progress (i.e. SSPSR is still shifting out a data byte), then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

WCOL must be cleared in software.

9.2.12.3 ACKSTAT STATUS FLAG

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge ($\overline{ACK}$ = 0), and is set when the slave does not Acknowledge ($\overline{ACK}$ = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

FIGURE 9-18: I²C MASTER MODE WAVEFORMS FOR TRANSMISSION (7 OR 10-BIT ADDRESS)



REGISTER 11-1: A/D CONTROL REGISTER 0 (ADCON0: 1Fh).

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON
bit 7							bit 0

bit 7-6 **ADCS<1:0>:** A/D Conversion Clock Select bits

If internal VRL and/or VRH are not used for A/D reference (VCFG<2:0> = 000, 001, 011 or 101):
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from a dedicated RC oscillator)
If internal VRL and/or VRH are used for A/D reference (VCFG<2:0> = 010, 100, 110 or 111):
00 = FOSC/16
01 = FOSC/64
10 = FOSC/256
11 = FRC/8

bit 5-3,1 **CHS:<3:0>:** Analog Channel Select bits

0000 = channel 00 (AN0)
0001 = channel 01 (AN1)
0010 = channel 02 (AN2)
0011 = channel 03 (AN3)
0100 = channel 04 (AN4)
0101 = channel 05 (AN5)
0110 = reserved, do not select
0111 = reserved, do not select
1000 = reserved, do not select
1001 = reserved, do not select
1010 = reserved, do not select
1011 = reserved, do not select
1100 = reserved, do not select
1101 = reserved, do not select
1110 = reserved, do not select
1111 = reserved, do not select

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

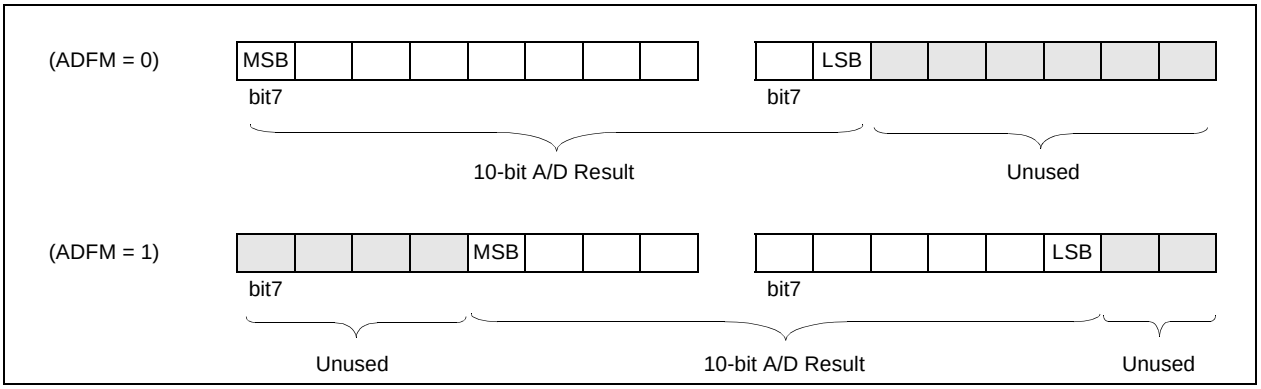
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** A/D On bit

1 = A/D converter module is operating
0 = A/D converter is shutoff and consumes no operating current

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 11-2: PIC16C717 10-BIT A/D RESULT FORMAT



After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS and ANSEL bits selected as an input. To determine acquisition time, see Section 11.6. After this acquisition time has elapsed, the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

11.2 Configuring the A/D Module

11.2.1 CONFIGURING ANALOG PORT PINS

The ANSEL and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted. The proper ANSEL bits must be set (analog input) to disable the digital input buffer.

The A/D operation is independent of the state of the TRIS bits and the ANSEL bits.

Note 1:	When reading the PORTA register, all pins configured as analog input channels will read as '0'.
2:	When reading the PORTB register, all pins configured as analog pins on PORTB will be read as '1'.
3:	Analog levels on any pin that is defined as a digital input, including the ANx pins, may cause the input buffer to consume current that is out of the devices specification.

11.2.2 CONFIGURING THE REFERENCE VOLTAGES

The VCFG bits in the ADCON1 register configure the A/D module reference inputs. The reference high input can come from an internal reference (VRH) or (VRL), an external reference (V_{REF+}), or AV_{DD}. The low reference input can come from an internal reference (VRL), an external reference (V_{REF-}), or AV_{SS}. If an external reference is chosen for the reference high or reference low inputs, the port pin that multiplexes the incoming external references is configured as an analog input, regardless of the values contained in the A/D port configuration bits (PCFG<3:0>).

12.8 Time-out Sequence

On power-up, the time-out sequence is as follows: First PWRT time-out is invoked by the POR pulse. When the PWRT delay expires, the Oscillator Start-up Timer is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 12-6, Figure 12-7, Figure 12-8 and Figure 12-9 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (Figure 12-8). This is useful for testing purposes or to synchronize more than one PIC® microcontroller operating in parallel.

Table 12-5 shows the RESET conditions for some special function registers, while Table 12-6 shows the RESET conditions for all the registers.

12.9 Power Control/STATUS Register (PCON)

The Power Control/STATUS Register, PCON, has two status bits that provide indication of which power-up type RESET occurred.

Bit0 is Brown-out Reset Status bit, $\overline{BOR}$. The $\overline{BOR}$ bit is unknown upon a POR. $\overline{BOR}$ must be set by the user and checked on subsequent RESETS to see if bit $\overline{BOR}$ cleared, indicating a BOR occurred.

Bit1 is $\overline{POR}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 12-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	TPWRT + 1024TOSC	1024TOSC	TPWRT + 1024TOSC	1024TOSC
EC, ER, INTRC	TPWRT	—	TPWRT	—

TABLE 12-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{MCLR}$ Reset during normal operation
1	1	1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 12-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- 1-0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- 1-uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---- 1-uu
WDT Reset	000h	0000 1uuu	---- 1-uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- u-uu
Brown-out Reset	000h	0001 1uuu	---- 1-u0
Interrupt wake-up from SLEEP, GIE = 0	PC + 1	uuu1 0uuu	---- u-uu
Interrupt wake-up from SLEEP, GIE = 1	0004h	uuu1 0uuu	---- u-uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

FIGURE 12-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 1

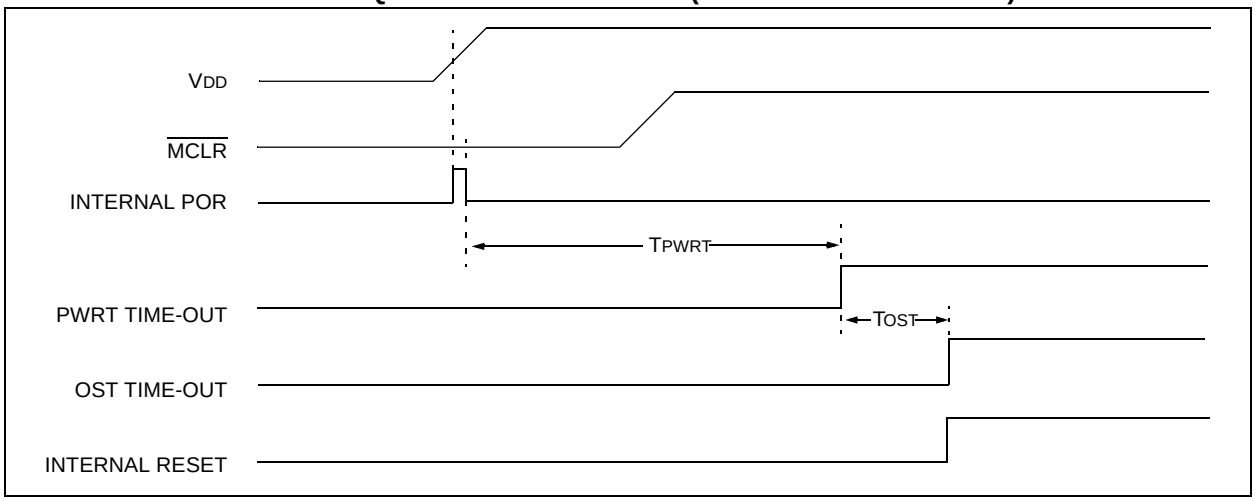


FIGURE 12-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 2

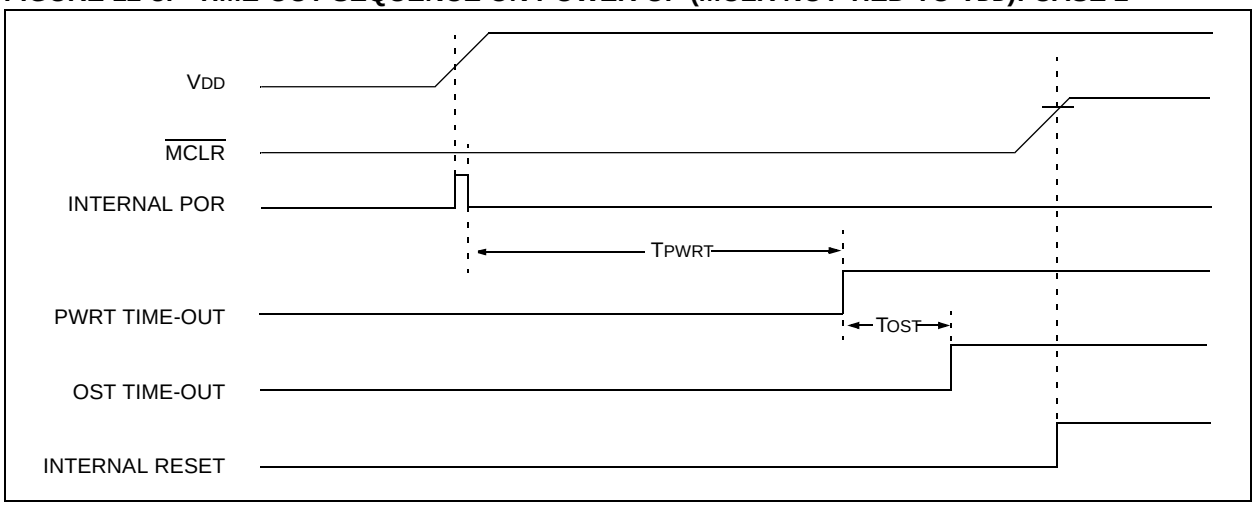
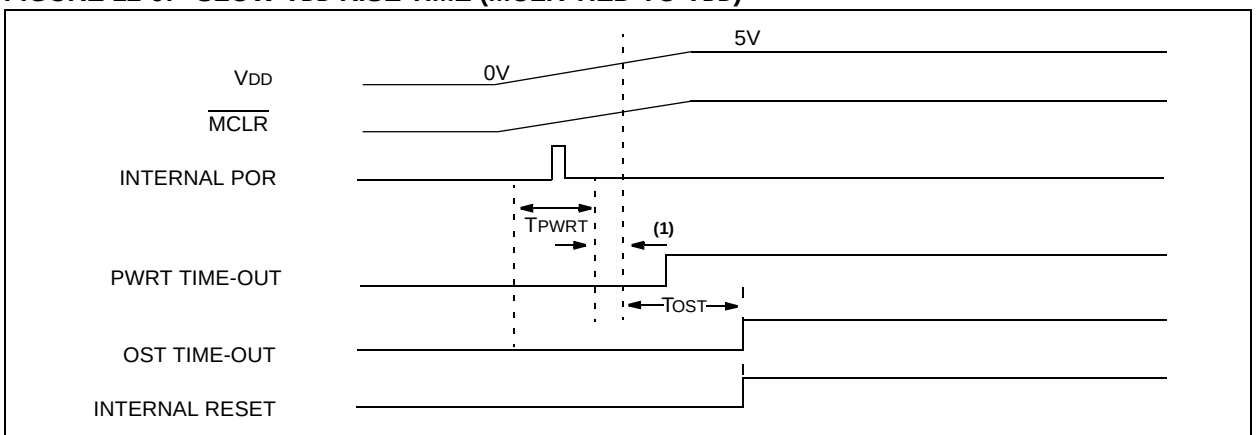


FIGURE 12-9: SLOW V_{DD} RISE TIME ($\overline{MCLR}$ TIED TO V_{DD})



Note 1: Time dependent on oscillator circuit

RETFIE **Return from Interrupt**

Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

RETLW **Return with Literal in W**

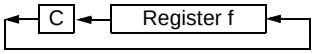
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RETURN **Return from Subroutine**

Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

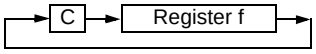
RLF **Rotate Left f through Carry**

Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



RRF **Rotate Right f through Carry**

Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



SLEEP

Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 12.8 for more details.

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TMCL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +85°C
31*	TWDT	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32*	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	TPWRT	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34*	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.1	µs	
35*	TBOR	Brown-out Reset pulse width	100	—	—	µs	VDD ≤ VBOR (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-9: BROWN-OUT RESET CHARACTERISTICS

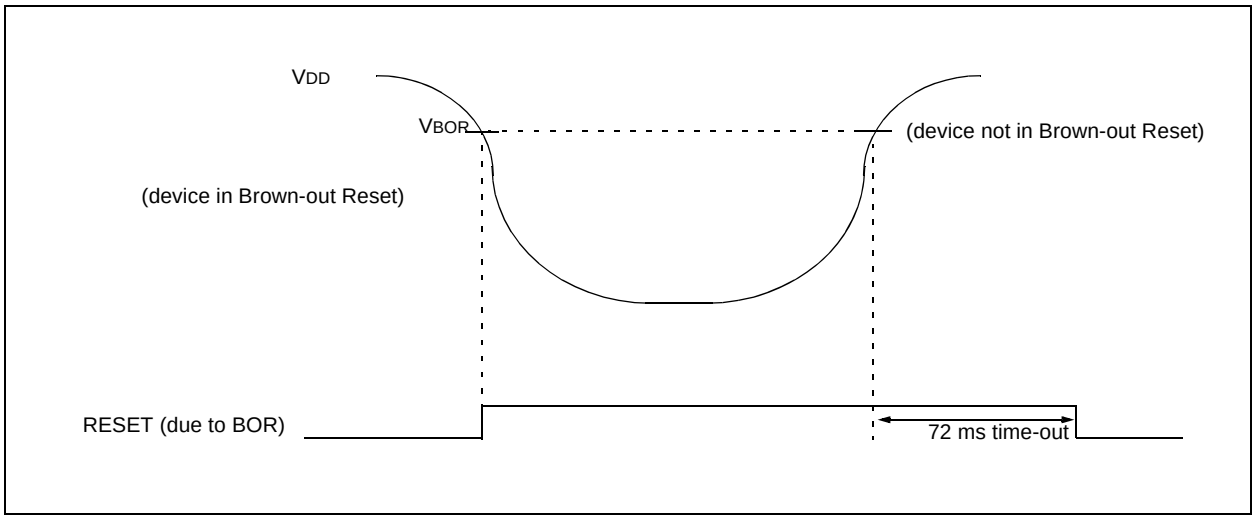
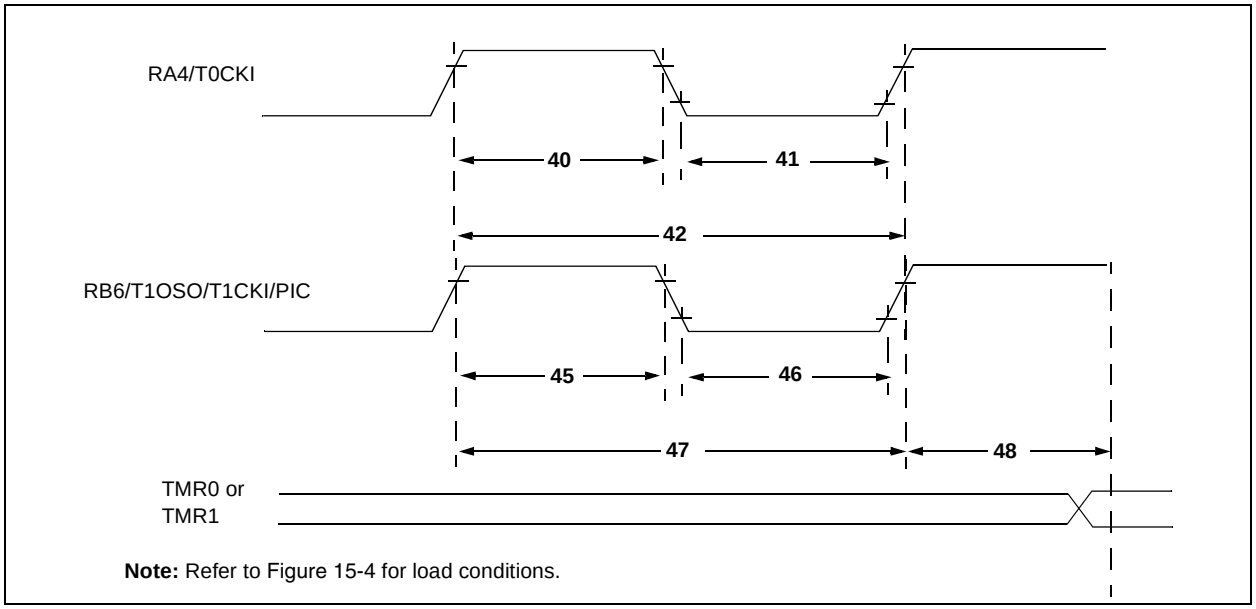


FIGURE 15-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Note: Refer to Figure 15-4 for load conditions.

15.4.2 LOW VOLTAGE DETECT MODULE (LVD)

FIGURE 15-13: LOW VOLTAGE DETECT CHARACTERISTICS

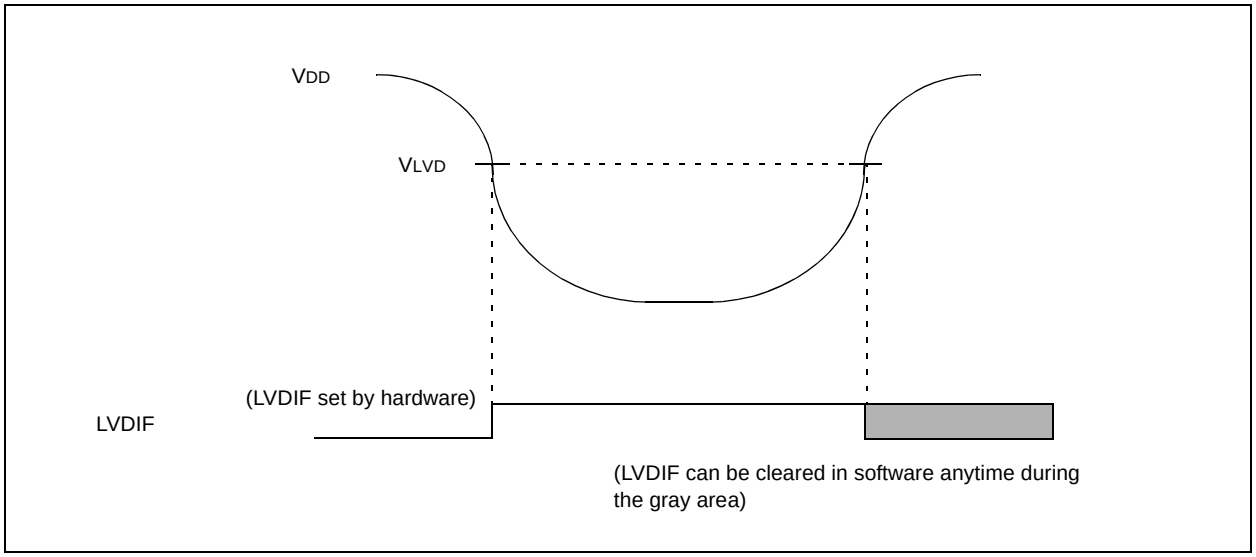


TABLE 15-8: ELECTRICAL CHARACTERISTICS: LVD

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC Characteristics Section 15.1.					
Param. No.	**Characteristic**		**Symbol**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420*	LVD Voltage	LVV = 0100	VLVD	2.5	2.58	2.66	V	
		LVV = 0101		2.7	2.78	2.86	V	
		LVV = 0110		2.8	2.89	2.98	V	
		LVV = 0111		3.0	3.1	3.2	V	
		LVV = 1000		3.3	3.41	3.52	V	
		LVV = 1001		3.5	3.61	3.72	V	
		LVV = 1010		3.6	3.72	3.84	V	
		LVV = 1011		3.8	3.92	4.04	V	
		LVV = 1100		4.0	4.13	4.26	V	
		LVV = 1101		4.2	4.33	4.46	V	
		LVV = 1110		4.5	4.64	4.78	V	

* These parameters are characterized but not tested.

Note 1: Production tested at Tamb = 25°C. Specifications over temperature limits ensured by characterization.

TABLE 15-14: PIC16C717 AND PIC16LC717 A/D CONVERTER CHARACTERISTICS:

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	Min. resolution for A/D is 4.1 mV, VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A03	EIL	Integral error	—	—	±1	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A04	EDL	Differential error	—	—	±1	LSb	No missing codes to 10 bits VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A06	EOFF	Offset error	—	—	±2	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A07	EGN	Gain Error	—	—	±1	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A10	—	Monotonicity	—	Note 3	—	—	AVSS ≤ VAIN ≤ VREF+
A20*	VREF	Reference voltage (VREF+ - VREF-)	4.096	—	VDD +0.3V	V	Absolute minimum electrical spec to ensure 10-bit accuracy.
A21*	VREF+	Reference V High (AVDD or VREF+)	VREF-	—	AVDD	V	Min. resolution for A/D is 4.1 mV
A22*	VREF-	Reference V Low (AVSS or VREF-)	AVSS	—	VREF+	V	Min. resolution for A/D is 4.1 mV
A25*	VAIN	Analog input voltage	VREFL	—	VREFH	V	
A30*	ZAIN	Recommended impedance of analog voltage source	—	—	2.5	kΩ	
A50*	IREF	VREF input current **(Note 2)**	—	—	10	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 11.0. During A/D conversion cycle.

* These parameters are characterized but not tested.

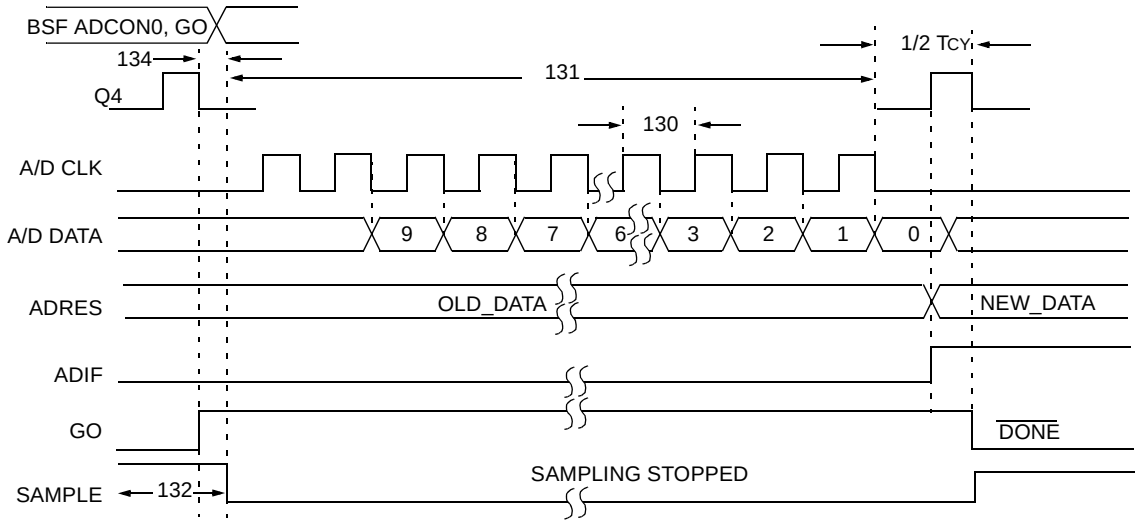
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from External VREF+, or VREF-, or AVSS, or AVDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

FIGURE 15-16: PIC16C717 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-15: PIC16C717 AND PIC16LC717 A/D CONVERSION REQUIREMENT (NORMAL MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	1.6	—	—	µs	Tosc based, VREF ≥ 2.5V
			3.0	—	—	µs	Tosc based, VREF full range
							ADCS<1:0> = 11 (A/D RC mode)
			3.0	6.0	9.0	µs	At VDD = 2.5V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	11TAD	—	TAD	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2	—	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.