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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c770-ss

1.0 DEVICE OVERVIEW

This document contains device-specific information. Additional information may be found in the PICmicro™ Mid-Range MCU Family Reference Manual, (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data

sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

There are three devices (PIC16C717, PIC16C770 and PIC16C771) covered by this data sheet. The PIC16C717 device comes in 18/20-pin packages and the PIC16C770/771 devices come in 20-pin packages.

The following two figures are device block diagrams of the PIC16C717 and the PIC16C770/771.

FIGURE 1-1: PIC16C717 BLOCK DIAGRAM

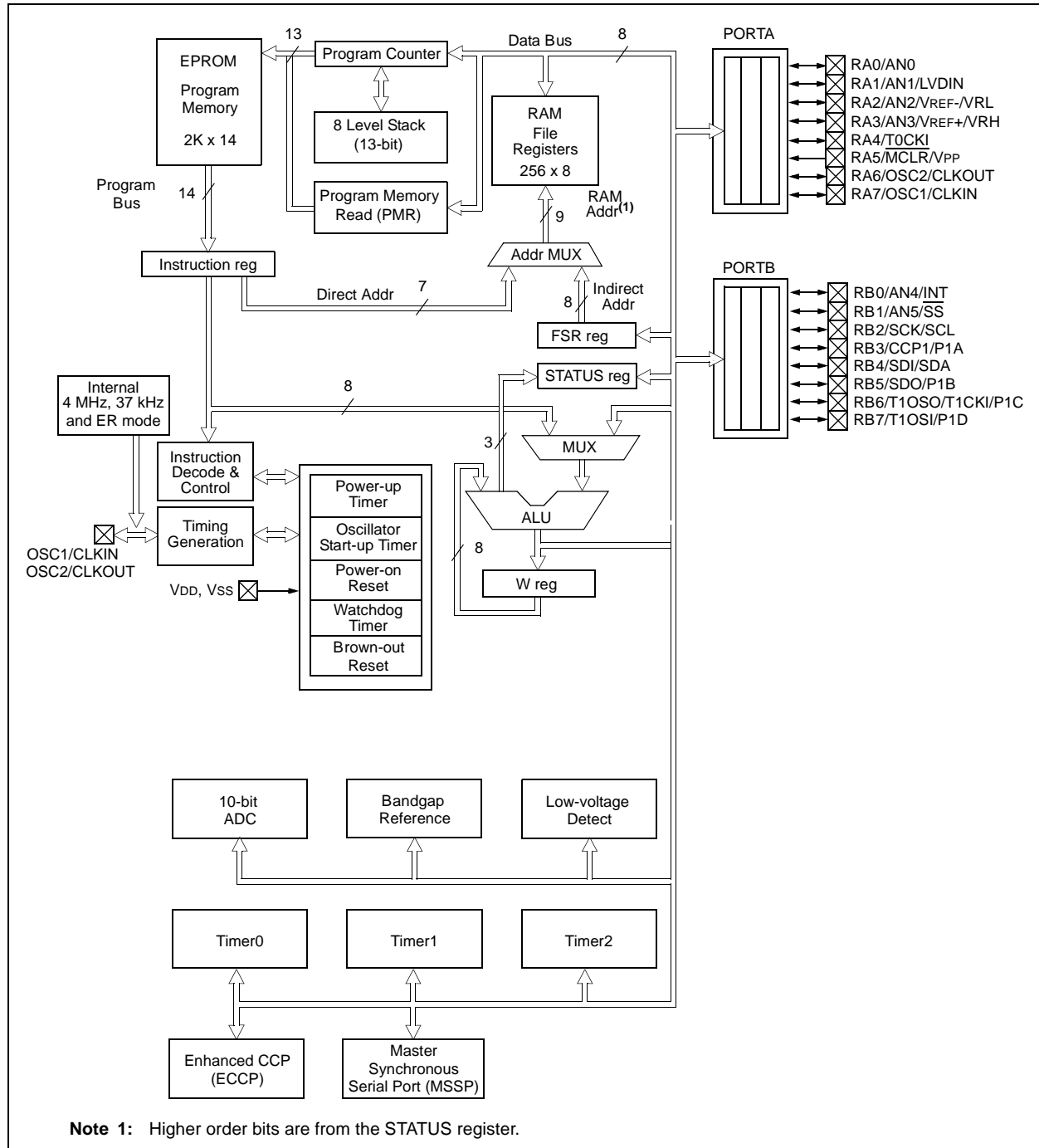


TABLE 1-1: PIC16C717/770/771 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0	RA0	ST	CMOS	Bi-directional I/O
	AN0	AN		A/D input
RA1/AN1/LVDIN	RA1	ST	CMOS	Bi-directional I/O
	AN1	AN		A/D input
	LVDIN	AN		LVD input reference
RA2/AN2/VREF-/VRL	RA2	ST	CMOS	Bi-directional I/O
	AN2	AN		A/D input
	VREF-	AN		Negative analog reference input
	VRL		AN	Internal voltage reference low output
RA3/AN3/VREF+/VRH	RA3	ST	CMOS	Bi-directional I/O
	AN3	AN		A/D input
	VREF+	AN		Positive analog reference input
	VRH		AN	Internal voltage reference high output
RA4/T0CKI	RA4	ST	OD	Bi-directional I/O
	T0CKI	ST		TMR0 clock input
RA5/MCLR/VPP	RA5	ST		Input port
	MCLR	ST		Master clear
	VPP	Power		Programming voltage
RA6/OSC2/CLKOUT	RA6	ST	CMOS	Bi-directional I/O
	OSC2		XTAL	Crystal/resonator
	CLKOUT		CMOS	Fosc/4 output
RA7/OSC1/CLKIN	RA7	ST	CMOS	Bi-directional I/O
	OSC1	XTAL		Crystal/resonator
	CLKIN	ST		External clock input/ER resistor connection
RB0/AN4/INT	RB0	TTL	CMOS	Bi-directional I/O ⁽¹⁾
	AN4	AN		A/D input
	INT	ST		Interrupt input
RB1/AN5/SS	RB1	TTL	CMOS	Bi-directional I/O ⁽¹⁾
	AN5	AN		A/D input
	SS	ST		SSP slave select input
RB2/SCK/SCL	RB2	TTL	CMOS	Bi-directional I/O ⁽¹⁾
	SCK	ST	CMOS	Serial clock I/O for SPI
	SCL	ST	OD	Serial clock I/O for I ² C
RB3/CCP1/P1A	RB3	TTL	CMOS	Bi-directional I/O ⁽¹⁾
	CCP1	ST	CMOS	Capture 1 input/Compare 1 output
	P1A		CMOS	PWM P1A output
RB4/SDI/SDA	RB4	TTL	CMOS	Bi-directional I/O ⁽¹⁾
	SDI	ST		Serial data in for SPI
	SDA	ST	OD	Serial data I/O for I ² C
RB5/SDO/P1B	RB5	TTL	CMOS	Bi-directional I/O ⁽¹⁾
	SDO		CMOS	Serial data out for SPI
	P1B		CMOS	PWM P1B output

Note 1: Bit programmable pull-ups.

2: Only in PIC16C770/771 devices.

2.2.2.2 OPTION_REG REGISTER

The OPTION_REG register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION REGISTER (OPTION_REG: 81h, 181h)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RBP _U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
	bit 7							bit 0
bit 7	RBP_U: PORTB Pull-up Enable bit ⁽¹⁾ 1 = PORTB weak pull-ups are disabled 0 = PORTB weak pull-ups are enabled by the WPUB register							
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin							
bit 5	T0CS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)							
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0CKI pin 0 = Increment on low-to-high transition on RA4/T0CKI pin							
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module							
bit 2-0	PS<2:0>: Prescaler Rate Select bits							
	Bit Value	TMR0 Rate	WDT Rate					
	000	1 : 2	1 : 1					
	001	1 : 4	1 : 2					
	010	1 : 8	1 : 4					
	011	1 : 16	1 : 8					
	100	1 : 32	1 : 16					
	101	1 : 64	1 : 32					
	110	1 : 128	1 : 64					
	111	1 : 256	1 : 128					

Note 1: Individual weak pull-up on RB pins can be enabled/disabled from the weak pull-up PORTB Register (WPUB).

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 4-2: PROGRAM MEMORY DATA HIGH (PMDATH: 10Eh)

U-0	U-0	R-x	R-x	R-x	R-x	R-x	R-x
—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8
bit 7		bit 0					

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **PMD<13:8>:** The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 4-3: PROGRAM MEMORY DATA LOW (PMDATL: 10Ch)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	
PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	
bit 7								bit 0

bit 7-0 **PMD<7:0>:** The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 4-4: PROGRAM MEMORY ADDRESS HIGH (PMADRH: 10Fh)

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	PMA11	PMA10	PMA9	PMA8
bit 7				bit 0			

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **PMA<11:8>:** PMR Address bits

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 4-5: PROGRAM MEMORY ADDRESS LOW (PMADRL: 10Dh)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	
bit 7								bit 0

bit 7-0 **PMA<7:0>:** PMR Address bits

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

EXAMPLE 9-1: Loading the SSPBUF (SSPSR) Register

The SSPSR is not directly readable or writable, and can only be accessed by addressing the SSPBUF register. Additionally, the MSSP STATUS register (SSPSTAT) indicates the various status conditions.

- SDI is automatically controlled by the SPI module
- SDO must have TRISB<5> cleared
- SCK (Master mode) must have TRISB<2> cleared
- SCK (Slave mode) must have TRISB<2> set
- \overline{SS} must have TRISB<1> set, and ANSEL<5> cleared

9.1.3 TYPICAL CONNECTION

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

FIGURE 9-2: SPI MASTER/SLAVE CONNECTION



9.2 MSSP I²C Operation

The MSSP module in I²C mode fully implements all master and slave functions (including general call support) and provides interrupts on START and STOP bits in hardware to determine when the bus is free (multi-master function). The MSSP module implements the Standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used to transfer data. They are the SCL pin (clock) and the SDA pin (data). The MSSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>). The SCL and SDA pins are "glitch" filtered when operating as inputs. This filter functions in both the 100 kHz and 400 kHz modes. When these pins operate as outputs in the 100 kHz mode, there is a slow rate control of the pin that is independent of device frequency.

Before selecting any I²C mode, the SCL and SDA pins must be programmed as inputs by setting the appropriate TRIS bits. This allows the MSSP module to configure and drive the I/O pins as required by the I²C protocol.

The MSSP module has six registers for I²C operation. They are listed below.

- SSP Control Register (SSPCON)
- SSP Control Register2 (SSPCON2)
- SSP STATUS Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows for control of the I²C operation. Four mode selection bits (SSPCON<3:0>) configure the MSSP as any one of the following I²C modes:

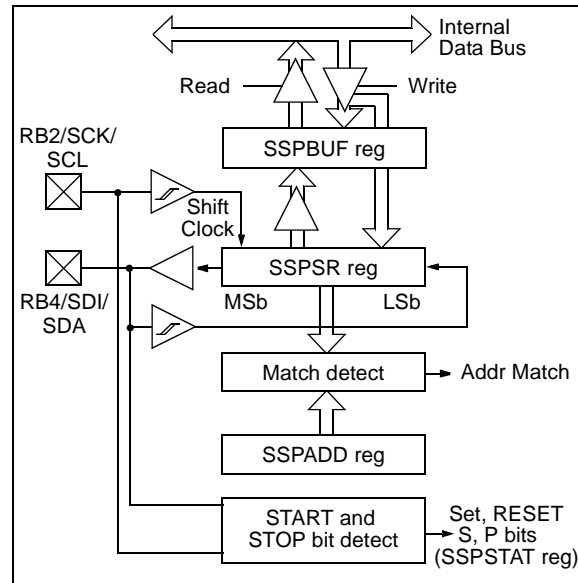
- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Master mode
- $SCL\ Freq = FOSC / [4 \cdot (SSPADD + 1)]$
- I²C Slave mode with START and STOP interrupts (7-bit address)
- I²C Slave mode with START and STOP interrupts (10-bit address)
- Firmware Controlled Master mode

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START (S) or STOP (P) bit. It specifies whether the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer.

SSPBUF is the register to which the transfer data is written, and from which the transfer data is read. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled, buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is

transferred from the SSPSR register to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read a receiver overflow occurs, in which case, the SSPOV bit (SSPCON<6>) is set and the byte in the SSPSR is lost.

FIGURE 9-7: I²C SLAVE MODE BLOCK DIAGRAM



9.2.1 UPWARD COMPATIBILITY WITH SSP MODULE

The MSSP module includes three SSP modes of operation to maintain upward compatibility with the SSP module. These modes are:

- Firmware controlled Master mode (slave idle)
- 7-bit Slave mode with START and STOP condition interrupts.
- 10-bit Slave mode with START and STOP condition interrupts.

The firmware controlled Master mode enables the START and STOP condition interrupts but all other I²C functions are generated through firmware including:

- Generating the START and STOP conditions
- Generating the SCL clock
- Supplying the SDA bits in the proper time and phase relationship to the SCL signal.

In firmware controlled Master mode, the SCL and SDA lines are manipulated by clearing and setting the corresponding TRIS bits. The output level is always low irrespective of the value(s) in the PORT register. A '1' is output by setting the TRIS bit and a '0' is output by clearing the TRIS bit

The 7-bit and 10-bit Slave modes with START and STOP condition interrupts operate identically to the MSSP Slave modes except that START and STOP conditions generate SSPIF interrupts.

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11.3 Selecting the A/D Conversion Clock

The A/D conversion cycle requires 13TAD: 1 TAD for settling time, and 12 TAD for conversion. The source of the A/D conversion clock is software selected. If neither the internal VRH nor VRL are used for the A/D converter, the four possible options for TAD are:

- 2 TOSC
- 8 TOSC
- 32 TOSC
- A/D RC oscillator

If the VRH or VRL are used for the A/D converter reference, then the TAD requirement is automatically increased by a factor of 8.

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μ s. Table 11-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

The ADIF bit is set on the rising edge of the 14th TAD. The GO/DONE bit is cleared on the falling edge of the 14th TAD.

TABLE 11-1: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Reference Source	A/D Clock Source (TAD)		Device Frequency			
	Operation	ADCS<1:0>	20 MHz	5 MHz	4 MHz	1.25 MHz
External VREF or Analog Supply	2 TOSC	00	100 ns ⁽²⁾	400 ns ⁽²⁾	500 ns ⁽²⁾	1.6 μ s
	8 TOSC	01	400 ns ⁽²⁾	1.6 μ s	2.0 μ s	6.4 μ s
	32 TOSC	10	1.6 μ s	6.4 μ s ⁽³⁾	8.0 μ s ⁽³⁾	25.6 μ s ⁽³⁾
	A/D RC	11	2 - 6 μ s ^(1,4)	2 - 6 μ s ^(1,4)	2 - 6 μ s ^(1,4)	2 - 6 μ s ^(1,4)
Internal VRH or VRL	16 TOSC	00	800 ns ⁽²⁾	3.2 μ s ⁽²⁾	4 μ s ⁽²⁾	12.8 μ s
	64 TOSC	01	3.2 μ s ⁽²⁾	12.8 μ s	16 μ s	51.2 μ s ⁽³⁾
	256 TOSC	10	12.8 μ s	51.2 μ s ⁽³⁾	64 μ s ⁽³⁾	204.8 μ s ⁽³⁾
	A/D RC	11	16 - 48 μ s ^(4,5)	16 - 48 μ s ^(4,5)	16 - 48 μ s ^(4,5)	16 - 48 μ s ^(4,5)

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical TAD time of 4 μ s for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during SLEEP.

5: A/D RC clock source has a typical TAD time of 32 μ s for VDD > 3.0V.

12.8 Time-out Sequence

On power-up, the time-out sequence is as follows: First PWRT time-out is invoked by the POR pulse. When the PWRT delay expires, the Oscillator Start-up Timer is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 12-6, Figure 12-7, Figure 12-8 and Figure 12-9 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 12-8). This is useful for testing purposes or to synchronize more than one PIC® microcontroller operating in parallel.

Table 12-5 shows the RESET conditions for some special function registers, while Table 12-6 shows the RESET conditions for all the registers.

12.9 Power Control/STATUS Register (PCON)

The Power Control/STATUS Register, PCON, has two status bits that provide indication of which power-up type RESET occurred.

Bit0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. The $\overline{\text{BOR}}$ bit is unknown upon a POR. $\overline{\text{BOR}}$ must be set by the user and checked on subsequent RESETS to see if bit $\overline{\text{BOR}}$ cleared, indicating a BOR occurred.

Bit1 is $\overline{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 12-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$		
XT, HS, LP	TPWRT + 1024TOSC	1024TOSC	TPWRT + 1024TOSC	1024TOSC
EC, ER, INTRC	TPWRT	—	TPWRT	—

TABLE 12-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 12-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- 1-0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	---- 1-uu
$\overline{\text{MCLR}}$ Reset during SLEEP	000h	0001 0uuu	---- 1-uu
WDT Reset	000h	0000 1uuu	---- 1-uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- u-uu
Brown-out Reset	000h	0001 1uuu	---- 1-u0
Interrupt wake-up from SLEEP, GIE = 0	PC + 1	uuu1 0uuu	---- u-uu
Interrupt wake-up from SLEEP, GIE = 1	0004h	uuu1 0uuu	---- u-uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

COMF	Complement f
Syntax:	[<i>label</i>] COMF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(\bar{f}) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	$k \rightarrow PC<10:0>$ $PCLATH<4:3> \rightarrow PC<12:11>$
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

DECf	Decrement f
Syntax:	[<i>label</i>] DECf f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

INCF	Increment f
Syntax:	[<i>label</i>] INCF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination});$ skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead making it a 2TCY instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination}),$ skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead making it a 2TCY instruction.

TABLE 14-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	PIC18FXXX	24CXX/ 25CXX/ 93CXX	HCXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	MPLAB® C17 C Compiler											✓	✓	✓					
	MPLAB® C18 C Compiler													✓	✓	✓	✓		
Emulators	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	ICEPIC™ In-Circuit Emulator	✓	✓	✓	✓		✓	✓	✓		✓								
Debugger	MPLAB® ICD In-Circuit Debugger				✓*		✓*			✓					✓				
Programmers	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM™ 1 Demonstration Board		✓	✓			†		✓			✓							
	PICDEM™ 2 Demonstration Board				†		†							✓	✓				
	PICDEM™ 3 Demonstration Board										✓								
	PICDEM™ 14A Demonstration Board		✓																
	PICDEM™ 17 Demonstration Board												✓						
	KEELOQ® Evaluation Kit																✓		
	KEELOQ® Transponder Kit																✓		
	microID™ Programmer's Kit																	✓	
	125 kHz microID™ Developer's Kit																	✓	
	125 kHz Anticollision microID™ Developer's Kit																	✓	
	13.56 MHz Anticollision microID™ Developer's Kit																	✓	
	MCP2510 CAN Developer's Kit																	✓	✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

PIC16C717/770/771

15.2 DC Characteristics: PIC16C717/770/771 & PIC16LC717/770/771 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended Operating voltage V_{DD} range as described in Section 15.1 and Section 15.2.							
DC CHARACTERISTICS							
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033	V_{IL}	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR OSC1 (in XT, HS, LP and EC)	V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	— — — — —	$0.15V_{DD}$ $0.8V$ $0.2V_{DD}$ $0.2V_{DD}$ $0.3V_{DD}$	V V V V V	For entire V_{DD} range $4.5V \leq V_{DD} \leq 5.5V$ For entire V_{DD} range
D040 D040A D041 D042 D042A	V_{IH}	Input High Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR OSC1 (XT, HS, LP and EC)	2.0 $(0.25V_{DD} + 0.8V)$ $0.8V_{DD}$ $0.8V_{DD}$ $0.7V_{DD}$	— — — — —	V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}	V V V V V	$4.5V \leq V_{DD} \leq 5.5V$ For entire V_{DD} range For entire V_{DD} range
D070	IPURB	PORTB weak pull-up current per pin	50	250	400	μA	$V_{DD} = 5V$, $V_{PIN} = V_{SS}$
D060 D060A D061 D063	I_{IL} I_{IL}	Input Leakage Current ^(1,2) I/O ports (with digital functions) I/O ports (with analog functions) RA5/MCLR/VPP OSC1	— — — —	— — — —	± 1 ± 100 ± 5 ± 5	μA nA μA μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS, LP and EC osc configuration
D080	V_{OL}	Output Low Voltage I/O ports	—	—	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5V$
D090	V_{OH}	Output High Voltage I/O ports ⁽²⁾	$V_{DD} - 0.7$	—	—	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5V$
D150*	V_{OD}	Open Drain High Voltage	—	—	10.5	V	RA4 pin
D100 D101 D102	COS C2 C10 CB	Capacitive Loading Specs on Output Pins* OSC2 pin All I/O pins and OSC2 (in RC mode) SCL, SDA in I ² C mode	— — —	— — —	15 50 400	pF pF pF	In XT, HS and LP modes when external clock is used to drive OSC1.
	CVRH CVRL	VRH pin VRL pin	— —	— —	200 200	pF pF	VRH output enabled VRL output enabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

TABLE 15-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC16C717/770/771 AND PIC16LC717/770/771

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
		Operating Voltage V_{DD} range is described in Section and Section					
Parameter No.	Sym	Characteristic	Min	Typ ^{(1)*}	Max	Units	Conditions
	FIRC	Internal Calibrated RC Frequency	3.65	4.00	4.28	MHz	$V_{DD} = 5.0\text{V}$
		Internal RC Frequency*	3.55	4.00	4.31	MHz	$V_{DD} = 2.5\text{V}$

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

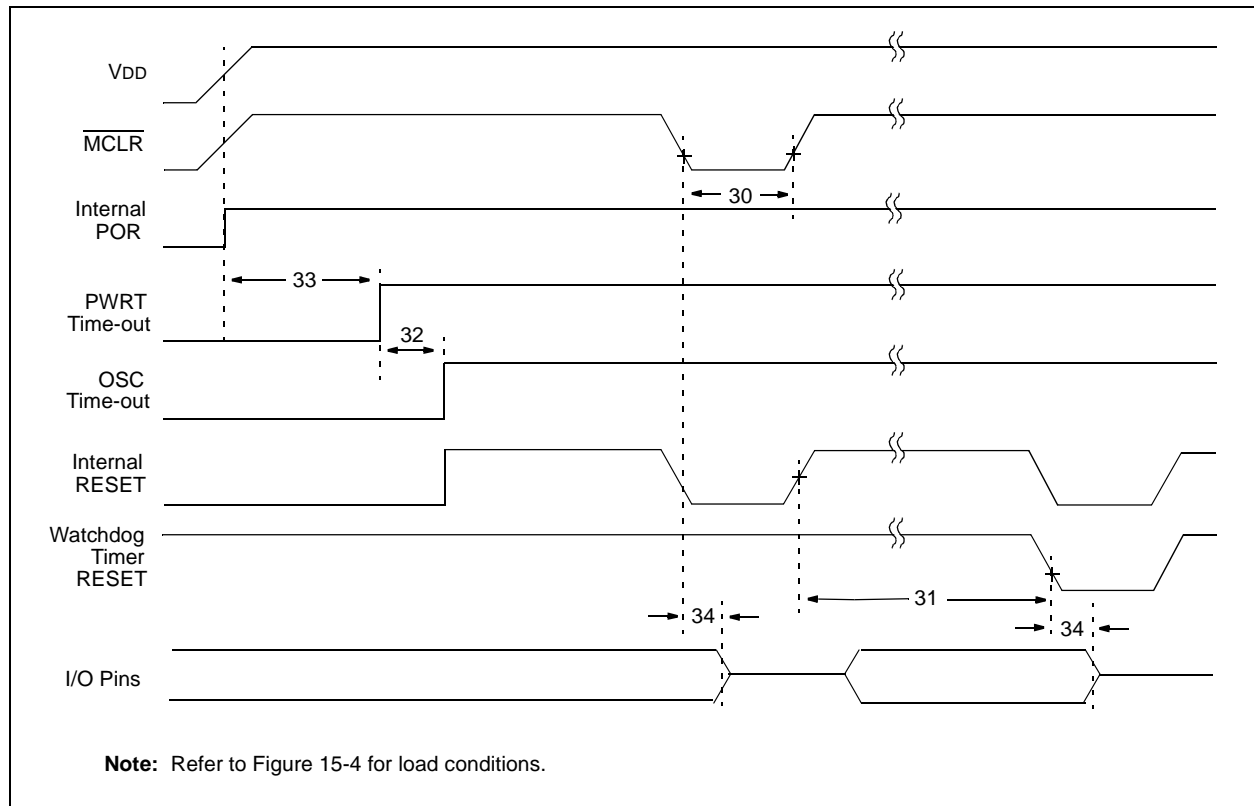
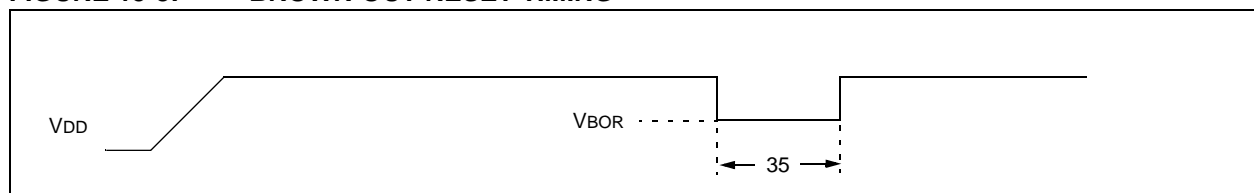


FIGURE 15-8: BROWN-OUT RESET TIMING



PIC16C717/770/771

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TMCL	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +85°C
31*	TWDT	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32*	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	TPWRT	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34*	TIOZ	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	μs	
35*	TBOR	Brown-out Reset pulse width	100	—	—	μs	VDD ≤ VBOR (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-9: BROWN-OUT RESET CHARACTERISTICS

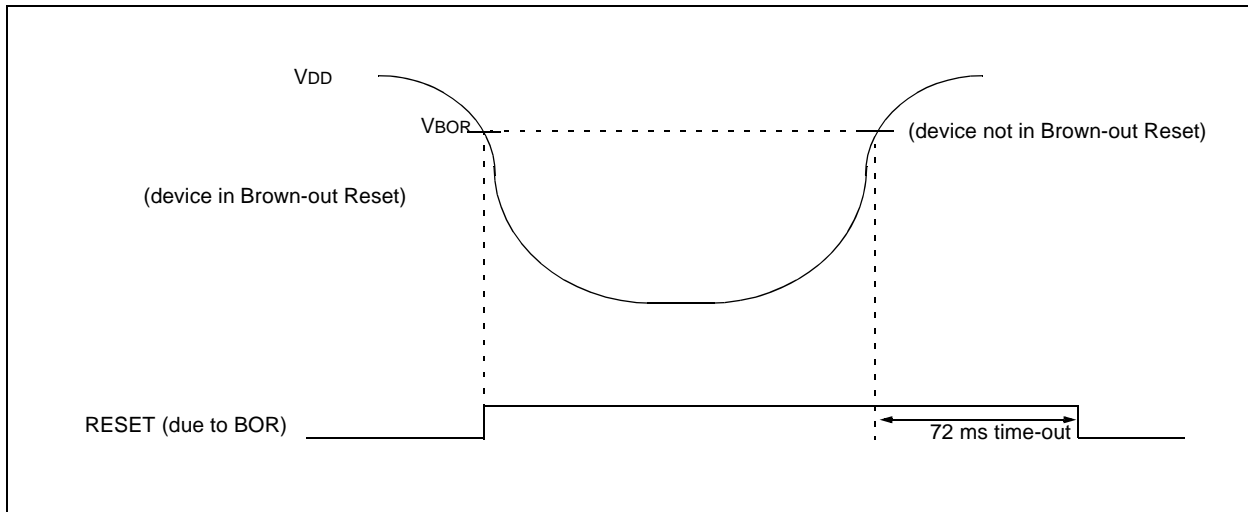
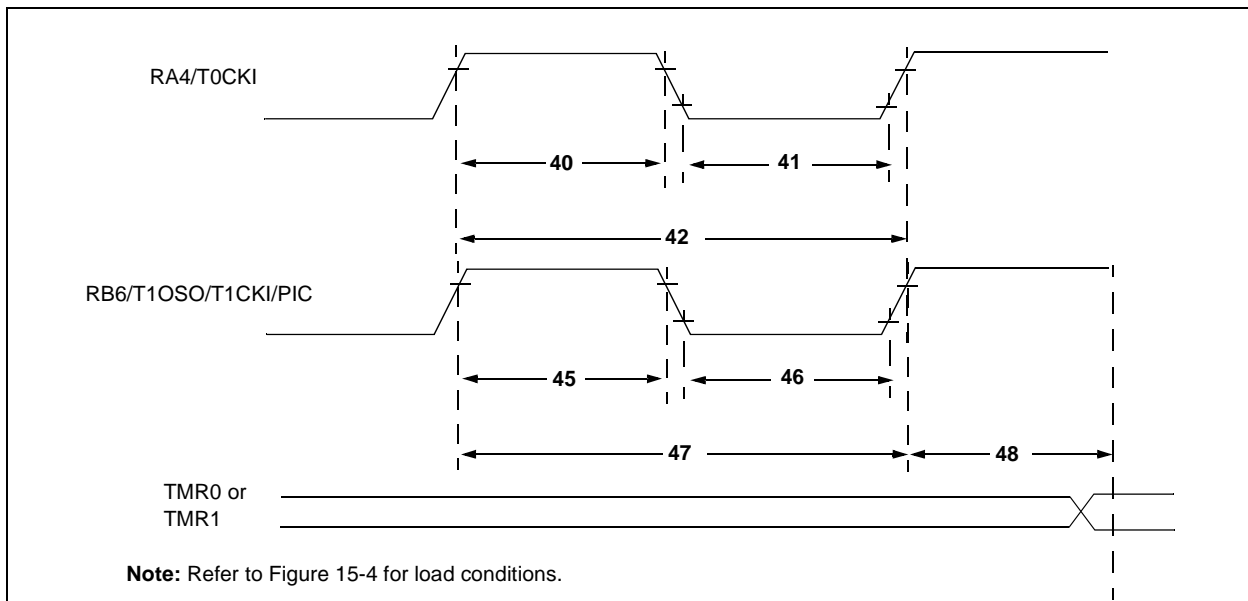


FIGURE 15-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



PIC16C717/770/771

FIGURE 15-19: SPI MASTER MODE TIMING (CKE = 1)

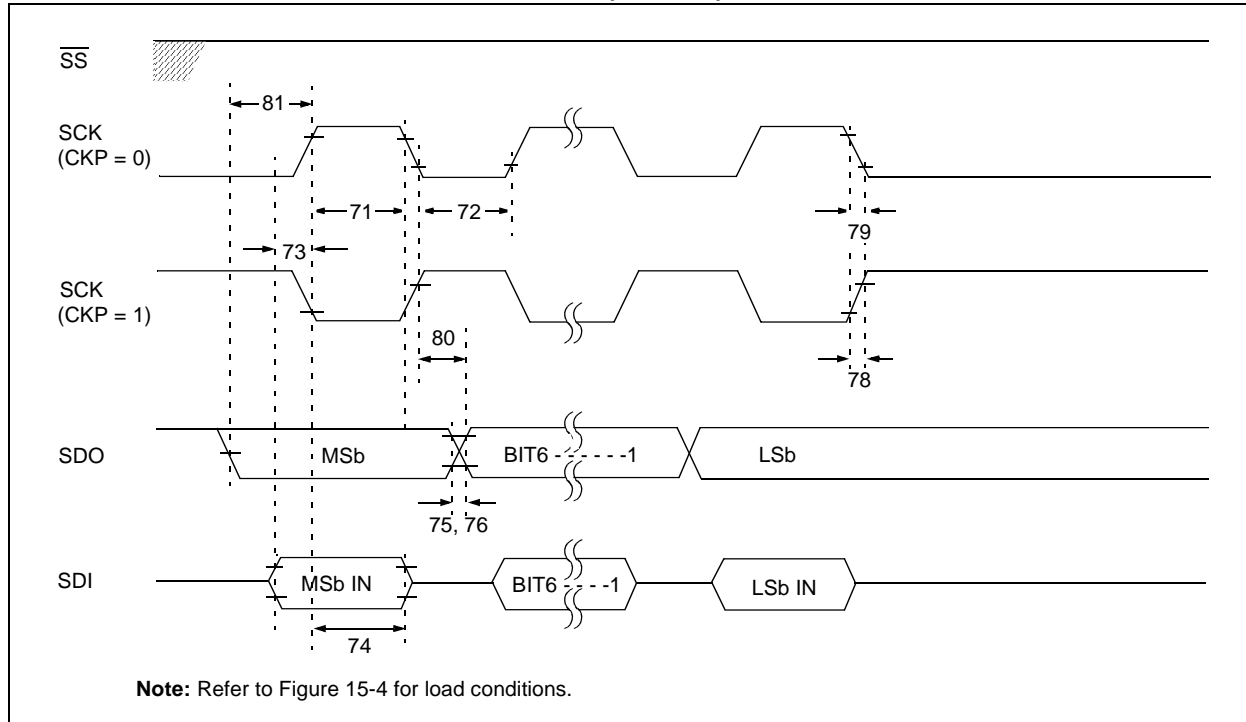


TABLE 15-18: SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
71*	TscH	SCK input high time	1.25Tcy + 30	—	—	ns	
71A*		Continuous	40	—	—	ns	Note 1
72*	TscL	SCK input low time	1.25Tcy + 30	—	—	ns	
72A*		Continuous	40	—	—	ns	Note 1
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	—	ns	
73A*	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5Tcy + 40	—	—	ns	Note 1
74*	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
75*	TdoR	SDO data output rise time	—	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
78*	TscR	SCK output rise time (Master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (Master mode)	—	10	25	ns	
80*	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

17.0 PACKAGING INFORMATION

17.1 Package Marking Information

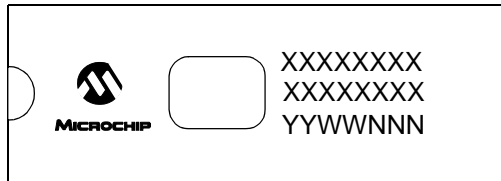
18-Lead PDIP



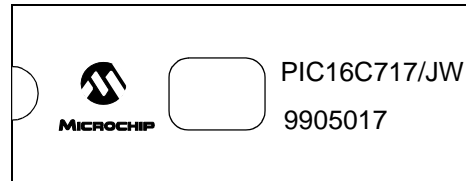
Example



18-Lead CERDIP Windowed



Example



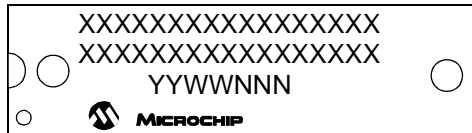
18-Lead SOIC



Example



20-Lead PDIP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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NOTES:

