What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
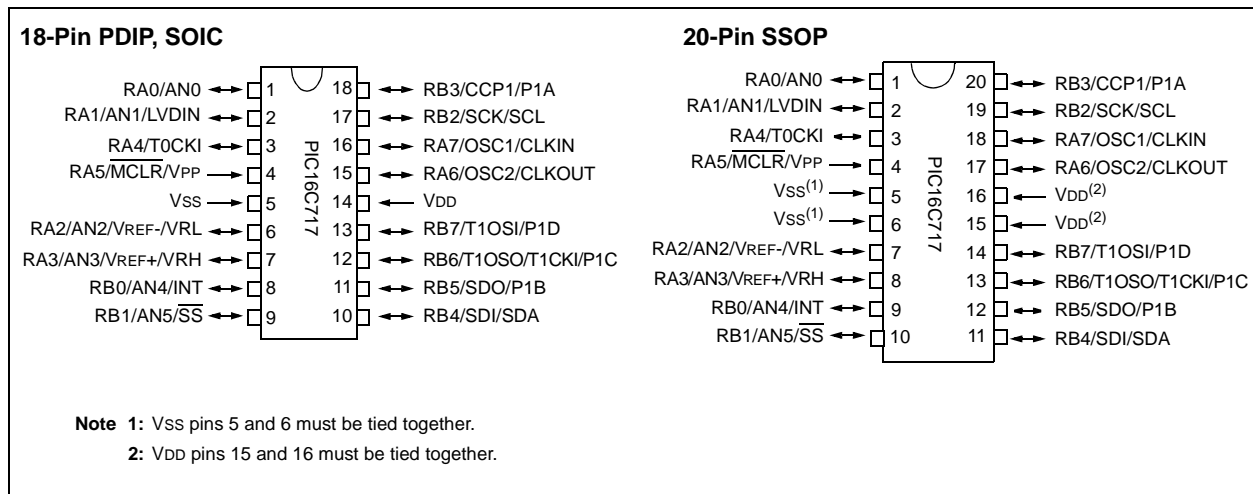
Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c771-i-so

PIC16C717/770/771

Pin Diagrams

18-Pin PDIP, SOIC

```
                              ___
RA0/AN0          ←→  [ 1      \_/    18 ]  ←→  RB3/CCP1/P1A
RA1/AN1/LVDIN    ←→  [ 2            17 ]  ←→  RB2/SCK/SCL
RA4/T0CKI        ←→  [ 3            16 ]  ←→  RA7/OSC1/CLKIN
RA5/MCLR/VPP     →   [ 4    PIC16C717  15 ]  ←→  RA6/OSC2/CLKOUT
VSS              ←   [ 5            14 ]  ←   VDD
RA2/AN2/VREF-/VRL ←→ [ 6            13 ]  ←→  RB7/T1OSI/P1D
RA3/AN3/VREF+/VRH ←→ [ 7            12 ]  ←→  RB6/T1OSO/T1CKI/P1C
RB0/AN4/INT      ←→  [ 8            11 ]  ←→  RB5/SDO/P1B
RB1/AN5/SS       ←→  [ 9            10 ]  ←→  RB4/SDI/SDA
```

20-Pin SSOP

```
                              ___
RA0/AN0          ←→  [ 1      \_/    20 ]  ←→  RB3/CCP1/P1A
RA1/AN1/LVDIN    ←→  [ 2            19 ]  ←→  RB2/SCK/SCL
RA4/T0CKI        ←→  [ 3            18 ]  ←→  RA7/OSC1/CLKIN
RA5/MCLR/VPP     →   [ 4            17 ]  ←→  RA6/OSC2/CLKOUT
VSS(1)           →   [ 5    PIC16C717  16 ]  ←   VDD(2)
VSS(1)           →   [ 6            15 ]  ←   VDD(2)
RA2/AN2/VREF-/VRL ←→ [ 7            14 ]  ←→  RB7/T1OSI/P1D
RA3/AN3/VREF+/VRH ←→ [ 8            13 ]  ←→  RB6/T1OSO/T1CKI/P1C
RB0/AN4/INT      ←→  [ 9            12 ]  ←→  RB5/SDO/P1B
RB1/AN5/SS       ←→  [ 10           11 ]  ←→  RB4/SDI/SDA
```

Note 1: V_{SS} pins 5 and 6 must be tied together.
2: V_{DD} pins 15 and 16 must be tied together.

Key Features PICmicro™ Mid-Range MCU Family Reference Manual, (DS33023)	PIC16C717	PIC16C770	PIC16C771
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR, MCLR, WDT (PWRT, OST)	POR, BOR, MCLR, WDT (PWRT, OST)	POR, BOR, MCLR, WDT (PWRT, OST)
Program Memory (14-bit words)	2K	2K	4K
Data Memory (bytes)	256	256	256
Interrupts	10	10	10
I/O Ports	Ports A,B	Ports A,B	Ports A,B
Timers	3	3	3
Enhanced Capture/Compare/PWM (ECCP) modules	1	1	1
Serial Communications	MSSP	MSSP	MSSP
12-bit Analog-to-Digital Module	—	6 input channels	6 input channels
10-bit Analog-to-Digital Module	6 input channels	—	—
Instruction Set	35 Instructions	35 Instructions	35 Instructions

2.0   MEMORY ORGANIZATION

There are two memory blocks in each of these PIC® microcontrollers. Each block (Program Memory and Data Memory) has its own bus, so that concurrent access can occur.

Additional information on device memory may be found in the PICmicro™ Mid-Range MCU Family Reference Manual, (DS33023).

2.1   Program Memory Organization

The PIC16C717/770/771 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16C717 and the PIC16C770 have 2K x 14 words of program memory. The PIC16C771 has 4K x 14 words of program memory. Accessing a location above the physically implemented address will cause a wrap-around.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1:   PROGRAM MEMORY MAP AND STACK OF THE PIC16C717 AND PIC16C770
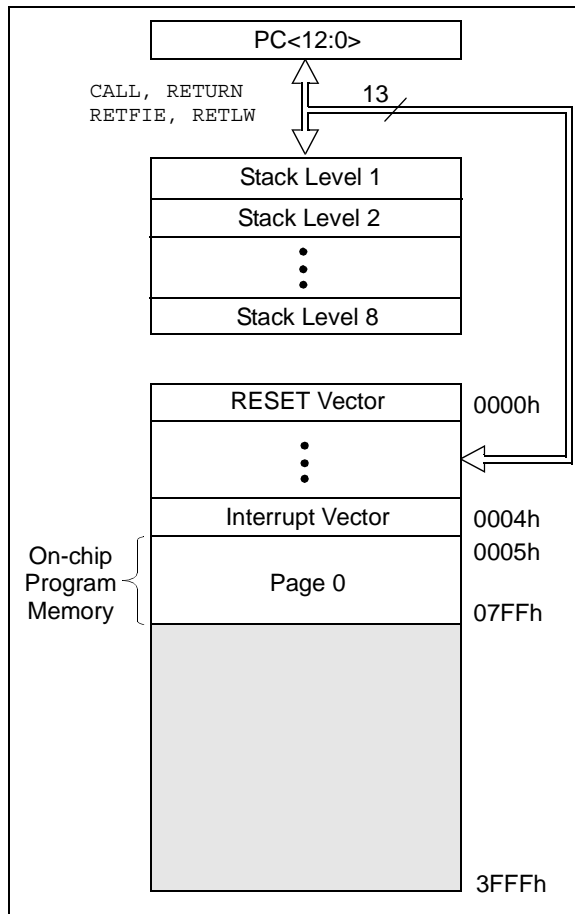
FIGURE 2-2:   PROGRAM MEMORY MAP AND STACK OF THE PIC16C771
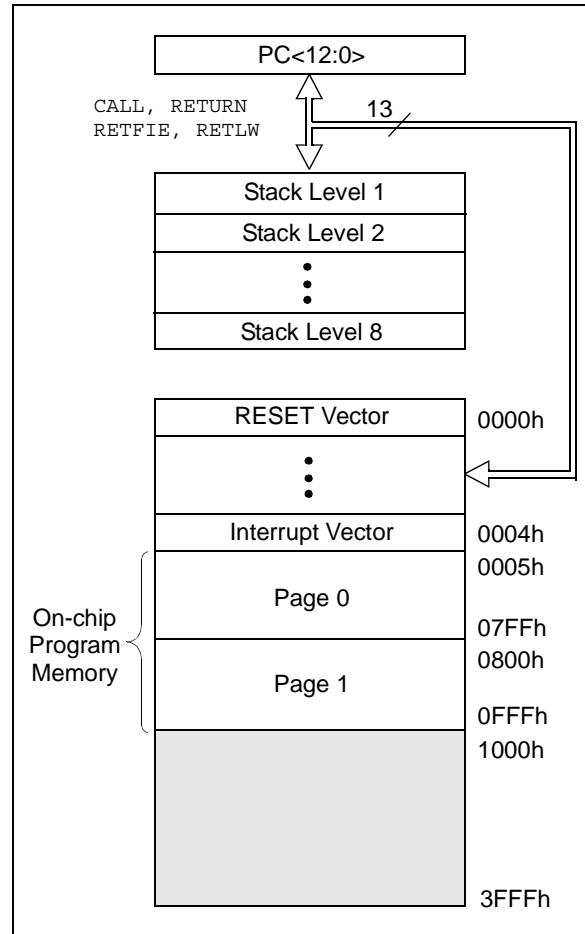
2.2   Data Memory Organization

The data memory is partitioned into multiple banks, which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

| RP1 | RP0 | (STATUS<6:5>)

= 00 → Bank0
= 01 → Bank1
= 10 → Bank2
= 11 → Bank3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some frequently used special function registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1   GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly, through the File Select Register FSR.

FIGURE 3-4: **BLOCK DIAGRAM OF RA5/MCLR/Vᴘᴘ**
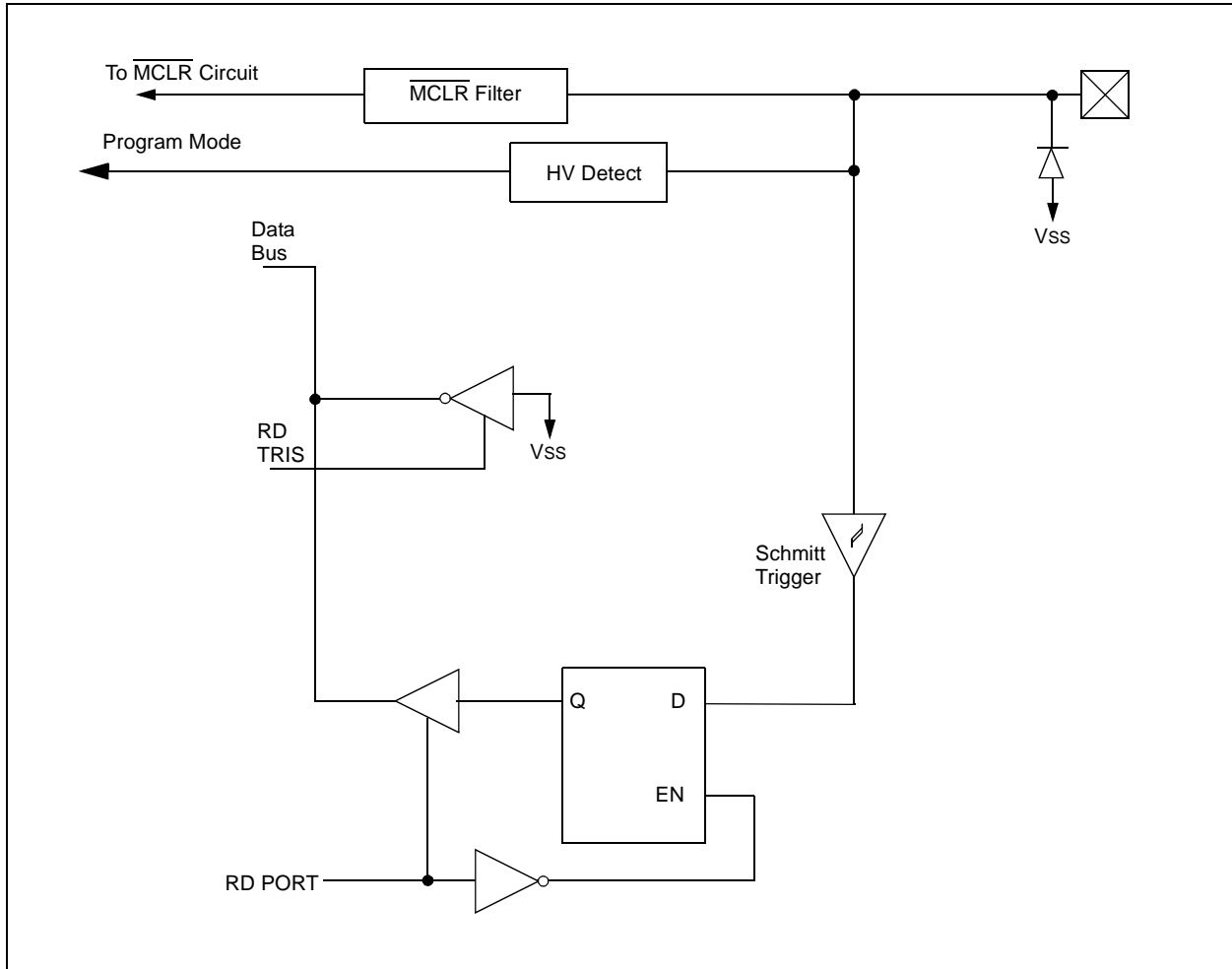
PIC16C717/770/771

TABLE 3-1: PORTA FUNCTIONS

Name	Function	Input Type	Output Type	Description
RA0/AN0	RA0	ST	CMOS	Bi-directional I/O
	AN0	AN		A/D input
RA1/AN1/LVDIN	RA1	ST	CMOS	Bi-directional I/O
	AN1	AN		A/D input
	LVDIN	AN		LVD input reference
RA2/AN2/VREF-/VRL	RA2	ST	CMOS	Bi-directional I/O
	AN2	AN		A/D input
	VREF-	AN		Negative analog reference input
	VRL		AN	Internal voltage reference low output
RA3/AN3/VREF+/VRH	RA3	ST	CMOS	Bi-directional I/O
	AN3	AN		A/D input
	VREF+	AN		Positive analog reference input
	VRH		AN	Internal voltage reference high output
RA4/T0CKI	RA4	ST	OD	Bi-directional I/O
	T0CKI	ST		TMR0 clock input
RA5/$\overline{\text{MCLR}}$/VPP	RA5	ST		Input port
	$\overline{\text{MCLR}}$	ST		Master clear
	VPP	Power		Programming voltage
RA6/OSC2/CLKOUT	RA6	ST	CMOS	Bi-directional I/O
	OSC2		XTAL	Crystal/resonator
	CLKOUT		CMOS	FOSC/4 output
RA7/OSC1/CLKIN	RA7	ST	CMOS	Bi-directional I/O
	OSC1	XTAL		Crystal/resonator
	CLKIN	ST/AN		External clock input/ER resistor connection

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	uuuu 0000
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
9Dh	ANSEL	—	—	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

PIC16C717/770/771

6.1.1 TIMER1 COUNTER OPERATION

In this mode, Timer1 is being incremented via an external source. Increments occur on a rising edge. After Timer1 is enabled in Counter mode, the module must first have a falling edge before the counter begins to increment.
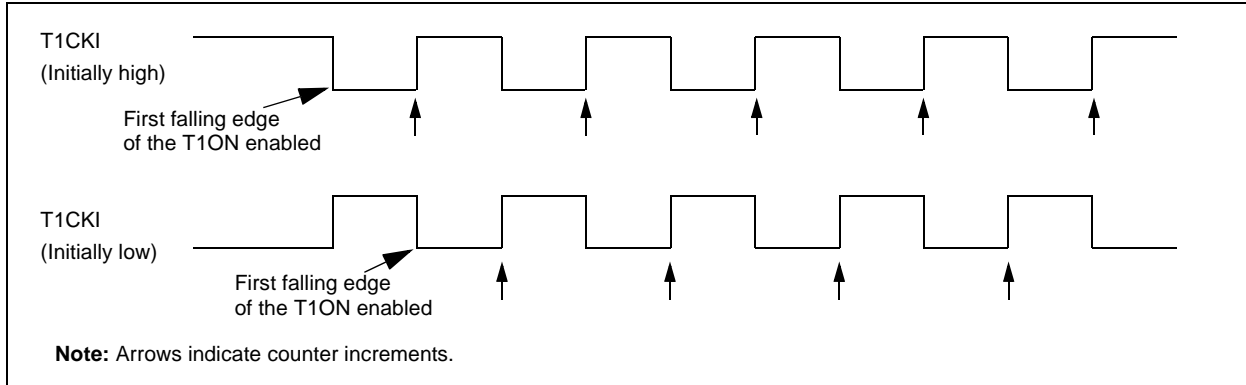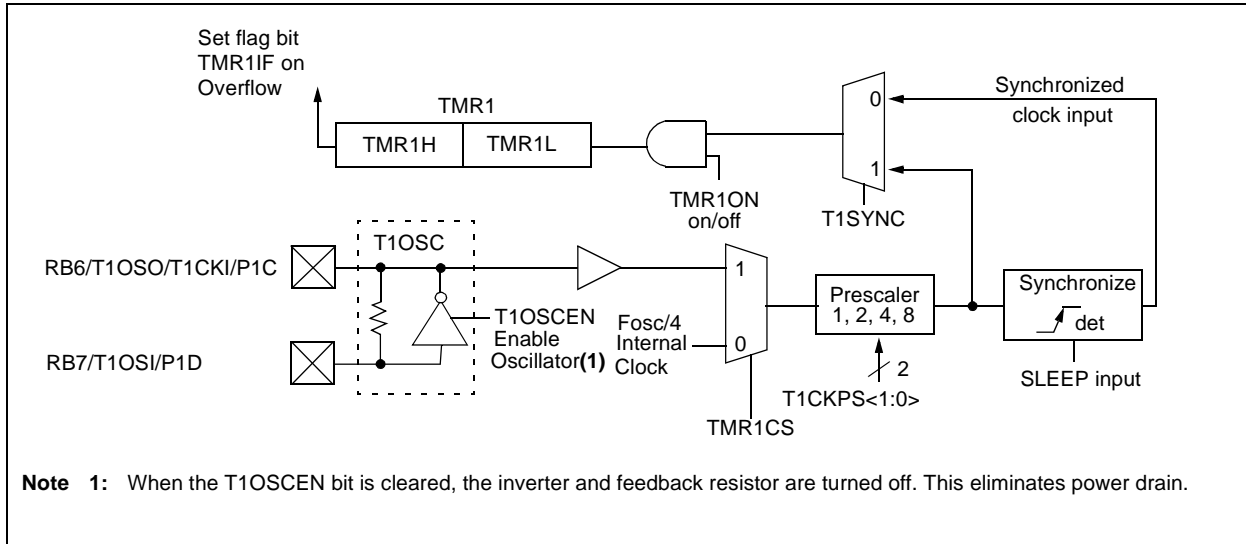
FIGURE 6-1: TIMER1 INCREMENTING EDGE

FIGURE 6-2: TIMER1 BLOCK DIAGRAM

Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

NOTES:

8.2.3   SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only an ECCP interrupt is generated (if enabled).

8.2.4   SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of ECCP resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special event trigger output of ECCP module will also start an A/D conversion if the A/D module is enabled.

Note:	The special event trigger will not set the interrupt flag bit TMR1IF (PIR1<0>).

FIGURE 8-2:   COMPARE MODE OPERATION BLOCK DIAGRAM

Special event trigger will:
RESET Timer1, but not set interrupt flag bit TMR1IF (PIR1<0>).
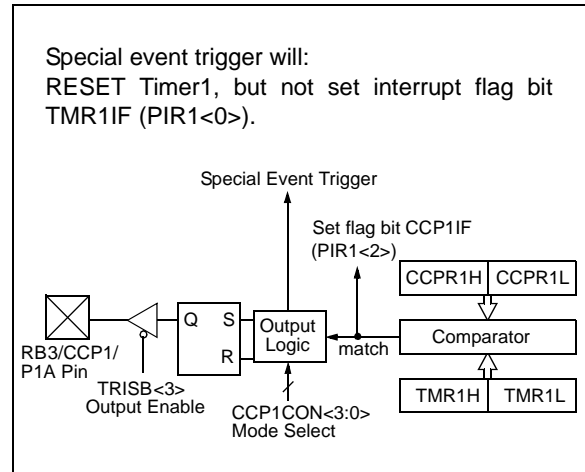
TABLE 8-2:   REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
PIR1	PSPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
TRISB	PORTB Data Direction Register								1111 1111	1111 1111
TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1register								xxxx xxxx	uuuu uuuu
T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
CCP1CON	PWM1M1	PWM1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

PIC16C717/770/771

8.3.5   PROGRAMMABLE DEADBAND DELAY

In half-bridge or full-bridge applications, driven by half-bridge outputs (see Figure 8-7), the power switches normally require longer time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches will be on for a short period of time, until one switch completely turns off. During this time, a very high current, called shoot-through current, will flow through both power switches,

shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on the power switch is normally delayed to allow the other switch to completely turn off.

In the Half-Bridge Output mode, a digitally programmable deadband delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 8-6 for illustration. The P1DEL register sets the amount of delay.

REGISTER 8-2:   PWM DELAY REGISTER (P1DEL: 97H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1DEL7	P1DEL6	P1DEL5	P1DEL4	P1DEL3	P1DEL2	P1DEL1	P1DEL0
bit 7							bit 0

bit 7-0   **P1DEL<7:0>: PWM Delay Count for Half-Bridge Output Mode:** Number of $F_{OSC}/4$ ($T_{OSC} \bullet 4$) cycles between the P1A transition and the P1B transition.
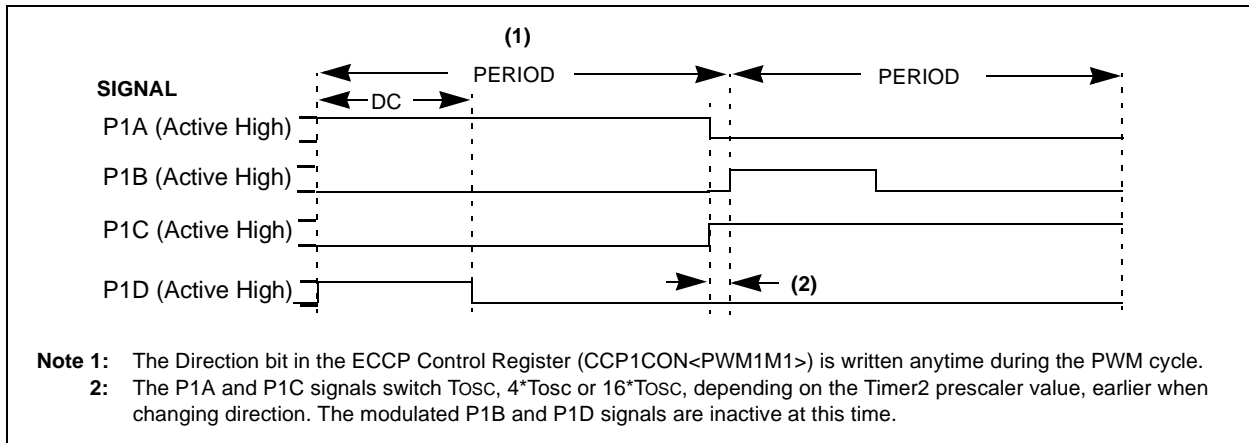
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

8.3.6   DIRECTION CHANGE IN FULL-BRIDGE OUTPUT MODE

In the Full-Bridge Output mode, the PWM1M1 bit in the CCP1CON register allows user to control the Forward/Reverse direction. When the application firmware changes this direction control bit, the ECCP module will assume the new direction on the next PWM cycle. The current PWM cycle still continues, however, the non-

modulated outputs, P1A and P1C signals, will transition to the new direction TOSC, 4•TOSC or 16•TOSC (for Timer2 prescale T2CKRS<1:0> = 00, 01 and 1x respectively) earlier, before the end of the period. During this transition cycle, the modulated outputs, P1B and P1D, will go to the inactive state. See Figure 8-10 for illustration.

FIGURE 8-10:   PWM DIRECTION CHANGE

Note 1:   The Direction bit in the ECCP Control Register (CCP1CON<PWM1M1>) is written anytime during the PWM cycle.
2:   The P1A and P1C signals switch T_{OSC}, 4*Tosc or 16*T_{OSC}, depending on the Timer2 prescaler value, earlier when changing direction. The modulated P1B and P1D signals are inactive at this time.

PIC16C717/770/771

9.1.4   MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 9-2) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI module is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor".

The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 9-3, Figure 9-5 and Figure 9-6, where the MSb is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- $F_{OSC}/4$ (or T_{CY})
- $F_{OSC}/16$ (or $4 \cdot T_{CY}$)
- $F_{OSC}/64$ (or $16 \cdot T_{CY}$)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 8.25 MHz.

Figure 9-3 shows the waveforms for Master mode. When CKE = 1, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

FIGURE 9-3:   SPI MODE WAVEFORM (MASTER MODE)
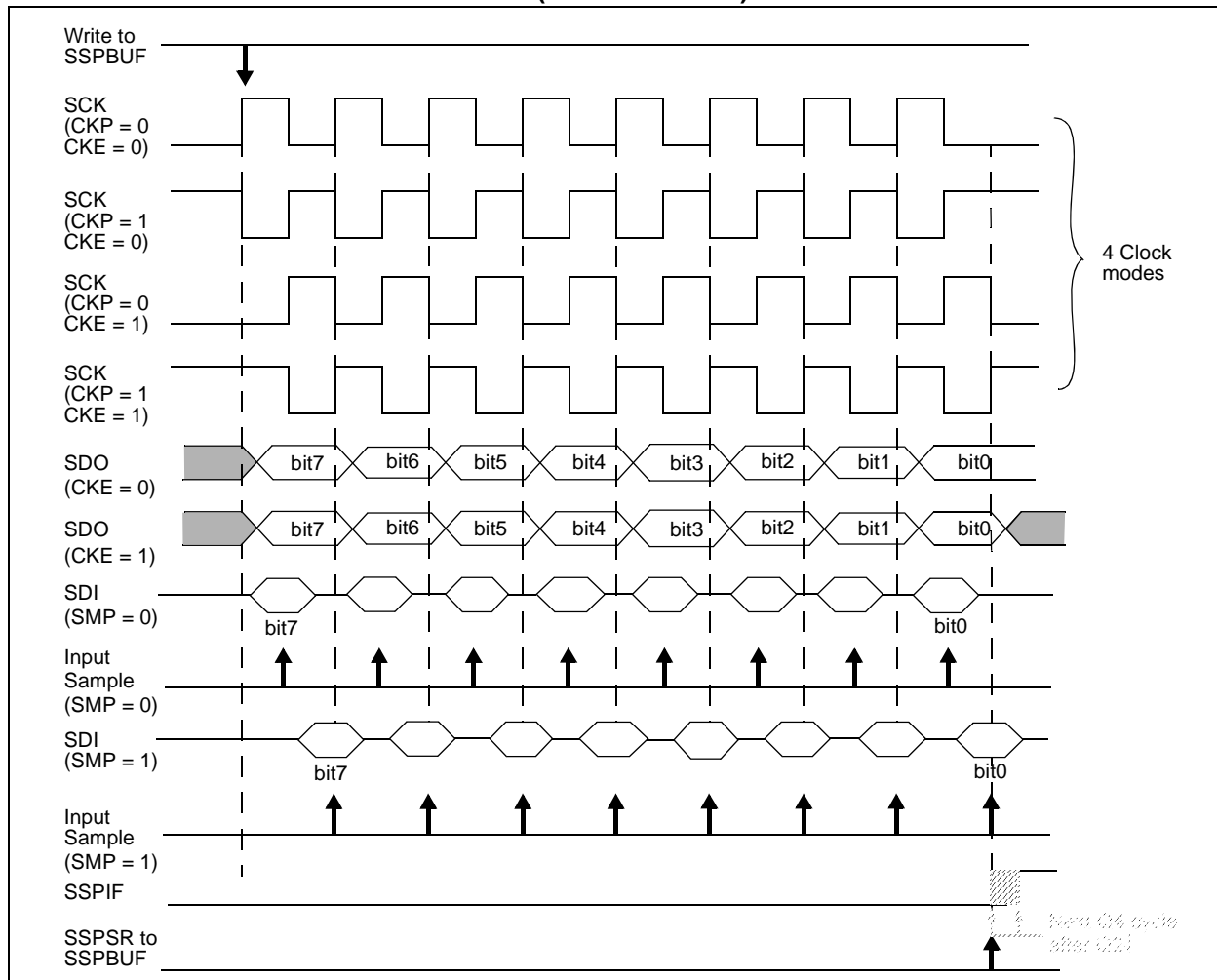
9.1.5   SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

9.1.6   SLAVE SELECT SYNCHRONIZATION

The $\overline{SS}$ pin allows a Synchronous Slave mode. The SPI must be in Slave mode with $\overline{SS}$ pin control enabled (SSPCON<3:0> = 0100). The pin must not be driven low for the $\overline{SS}$ pin to function as an input. TRISB<1> must be set. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the

SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/ pull-down resistors may be desirable, depending on the application.

> **Note 1:** When the SPI module is in Slave mode with $\overline{SS}$ pin control enabled, (SSP-CON<3:0> = 0100) the SPI module will RESET if the $\overline{SS}$ pin is set to VDD.
>
> **2:** If the SPI is used in Slave Mode with CKE = '1', then $\overline{SS}$ pin control must be enabled.

When the SPI module RESETS, the bit counter is forced to 0. This can be done by either forcing the $\overline{SS}$ pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 9-4:   SLAVE SYNCHRONIZATION WAVEFORM
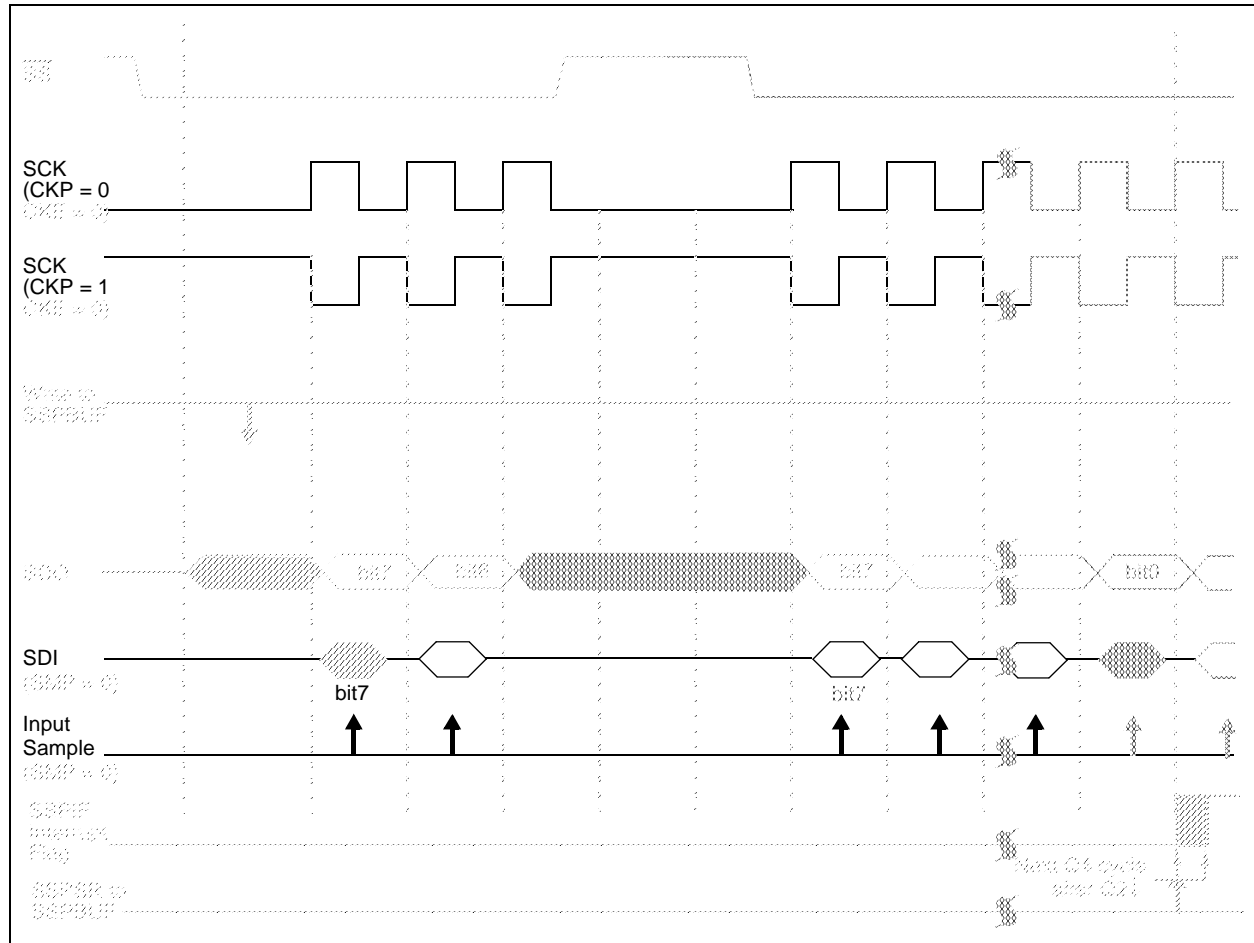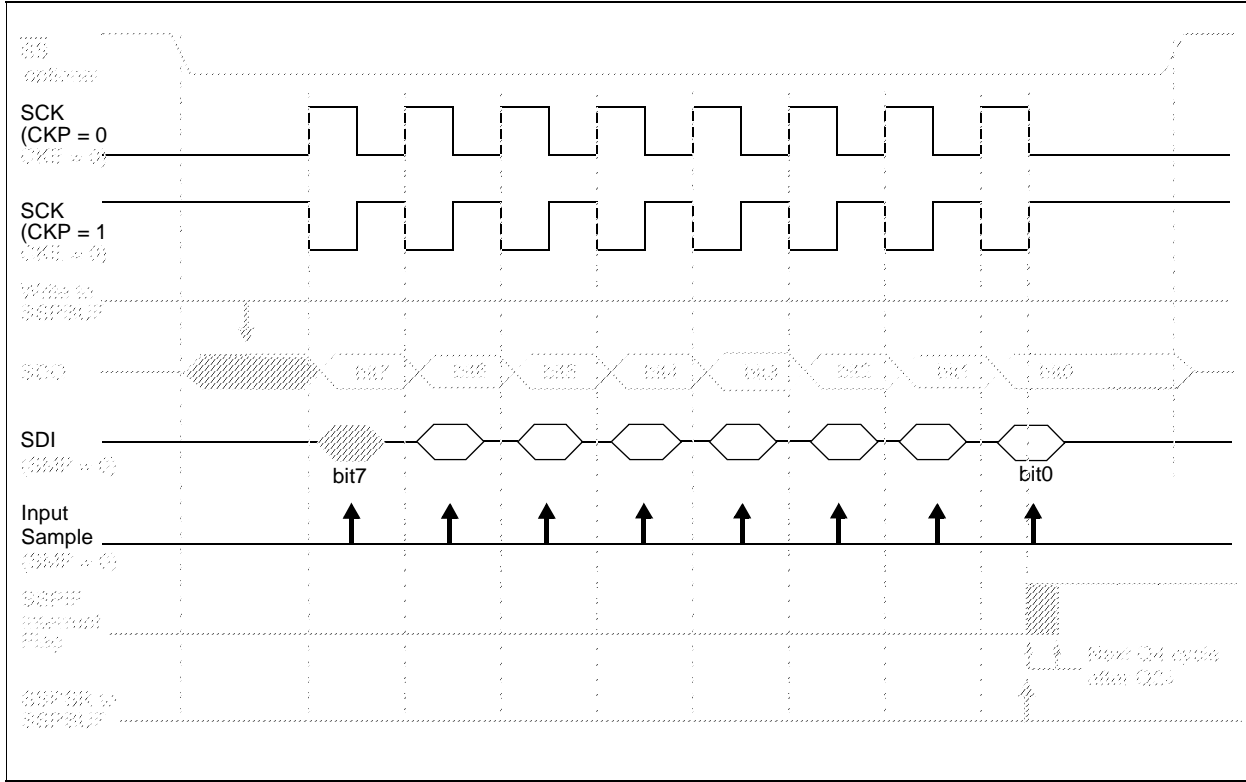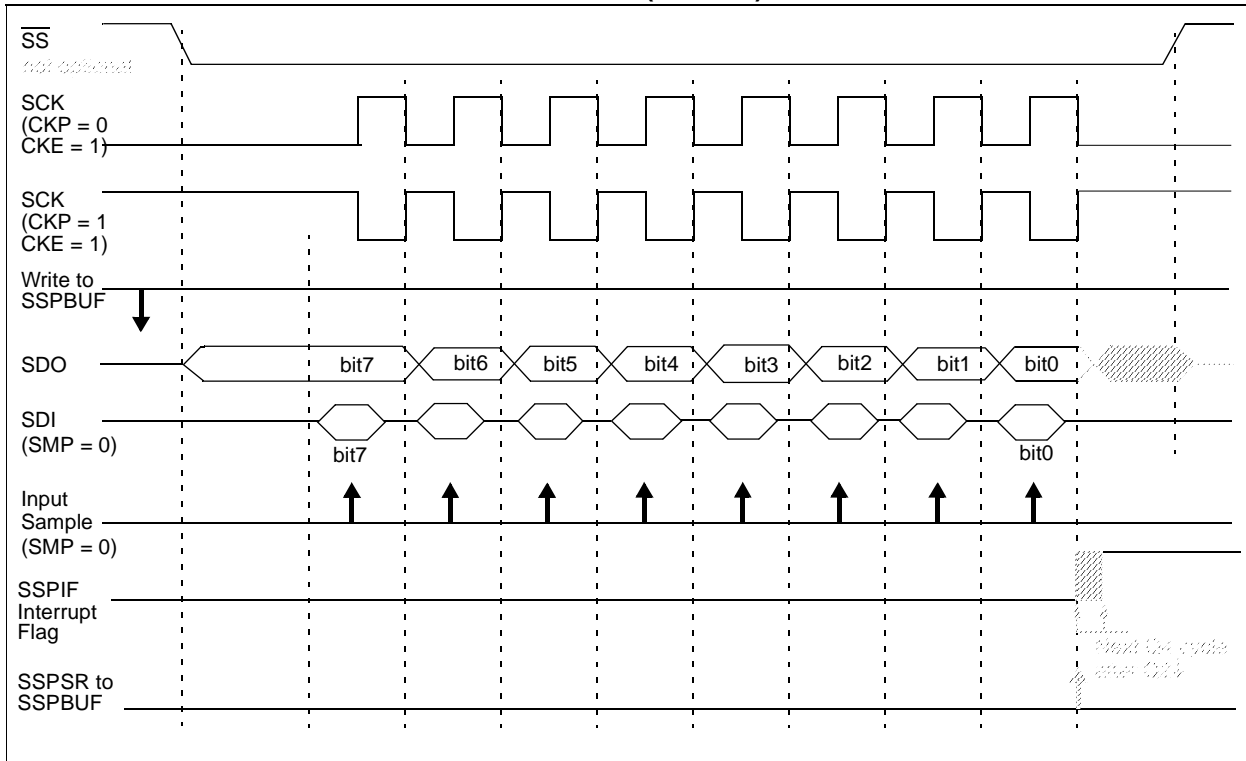
FIGURE 9-5: **SPI SLAVE MODE WAVEFORM (CKE = 0)**

FIGURE 9-6: **SPI SLAVE MODE WAVEFORM (CKE = 1)**

9.2.2.4 SLAVE TRANSMISSION

When the R/$\overline{\text{W}}$ bit of the incoming address byte is set and an address match occurs, the R/$\overline{\text{W}}$ bit of the SSP-STAT register is set. The received address is loaded into the SSPBUF register on the falling edge of the eighth SCL pulse. The $\overline{\text{ACK}}$ pulse will be sent on the ninth bit, and the SCL pin is held low. The slave module automatically stretches the clock by holding the SCL line low so that the master will be unable to assert another clock pulse until the slave is finished preparing the transmit data. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. The CKP bit (SSPCON<4>) must then be set to release the SCL pin from the forced low condition. The eight data bits are shifted out on the falling edges of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 9-10).

The $\overline{\text{ACK}}$ or NACK signal from the master-receiver is latched on the rising edge of the ninth SCL input pulse. The master-receiver terminates slave transmission by sending a NACK. If the SDA line is high (NACK), then the data transfer is complete. When the NACK is latched by the slave, the slave logic is RESET which also resets the R/$\overline{\text{W}}$ bit to '0'. The slave module then monitors for another occurrence of the START bit. The slave firmware knows not to load another byte into the SSPBUF register by sensing that the buffer is empty (BF = 0) and the R/$\overline{\text{W}}$ bit has gone low. If the SDA line is low ($\overline{\text{ACK}}$), the R/$\overline{\text{W}}$ bit remains high indicating that the next transmit data must be loaded into the SSPBUF register.

An MSSP interrupt (SSPIF flag) is generated for each data transfer byte on the falling edge of the ninth clock pulse. The SSPIF flag bit must be cleared in software. The SSPSTAT register is used to determine the status of the byte transfer.
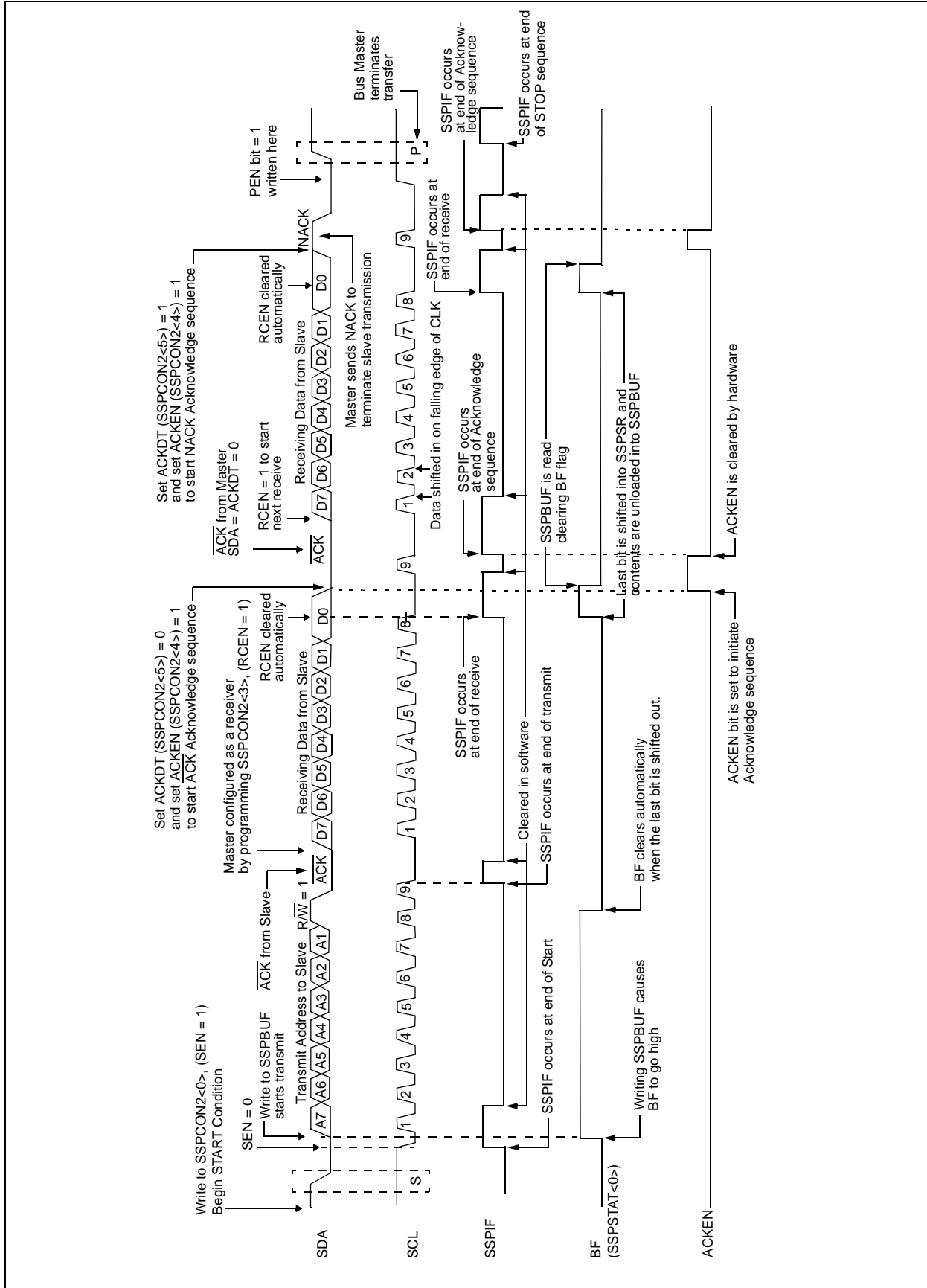
For more information about the I^{2}C Slave mode, refer to Application Note AN734, "*Using the PIC® SSP for Slave I^{2}C™ Communication*".

FIGURE 9-10: **I^{2}C SLAVE MODE WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)**
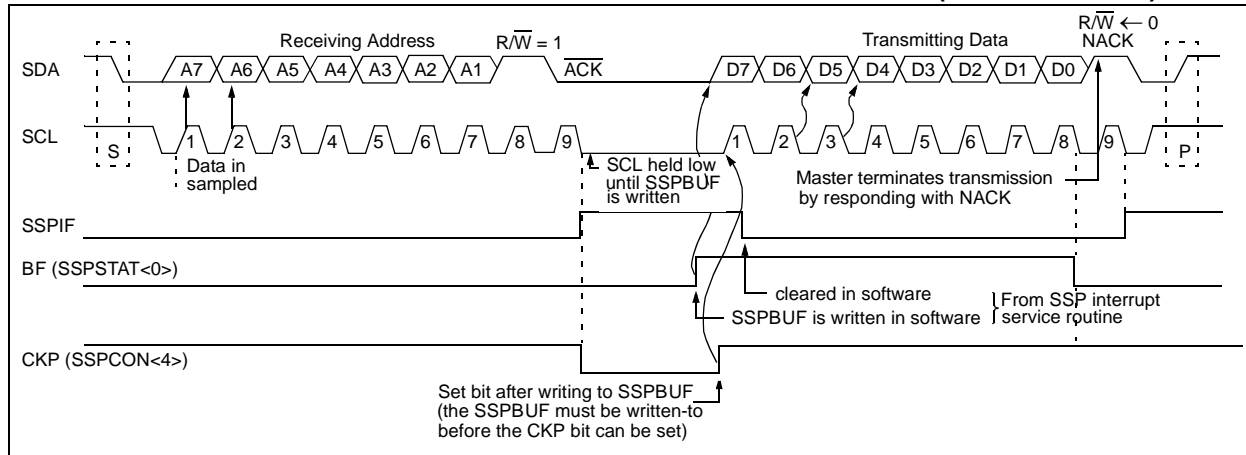
PIC16C717/770/771

FIGURE 9-19:   I²C MASTER WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

Advance Information   © 1999-2013 Microchip Technology Inc.

PIC16C717/770/771

FIGURE 12-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1
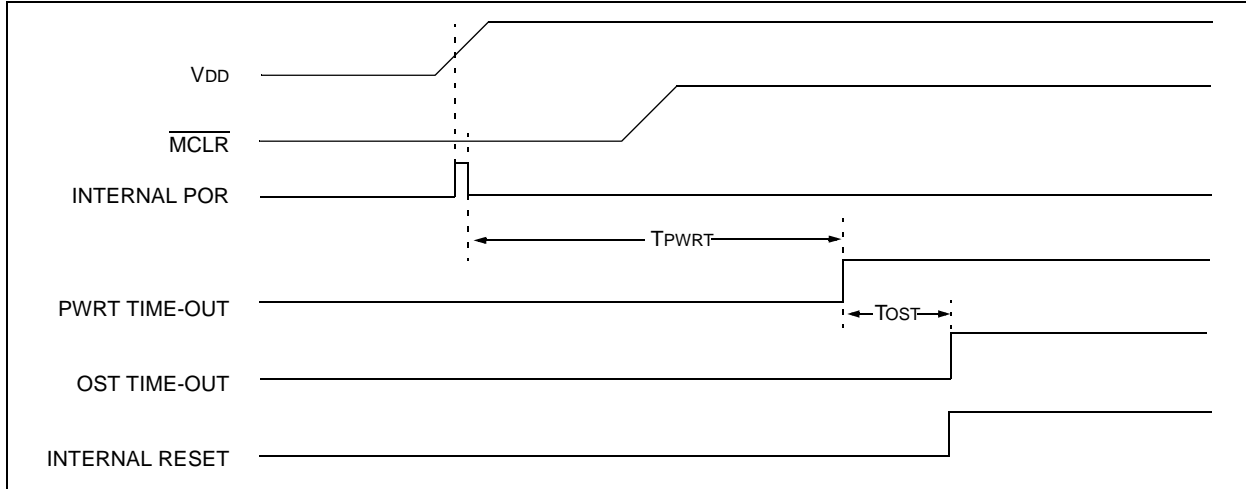

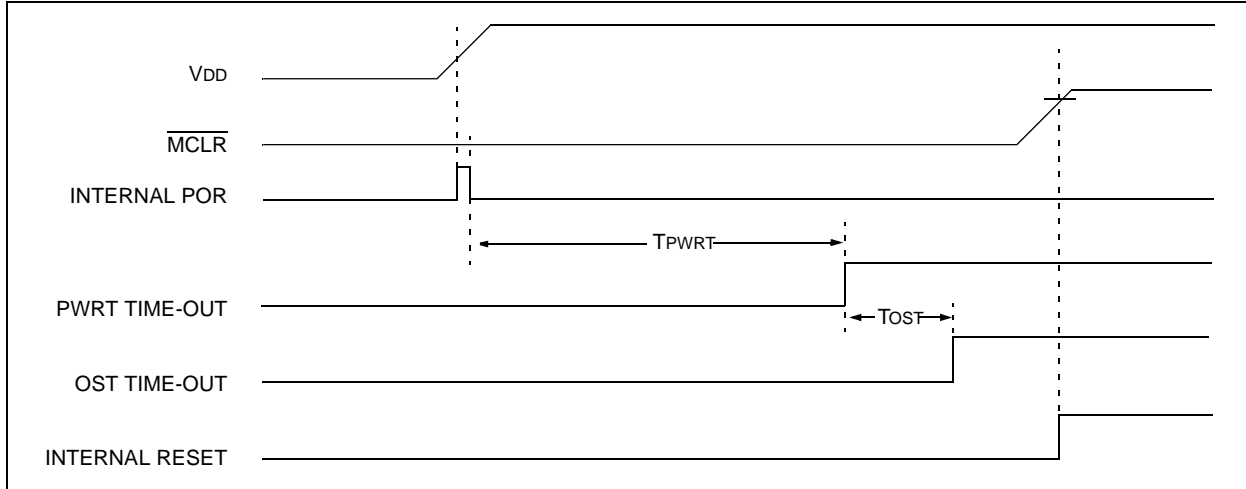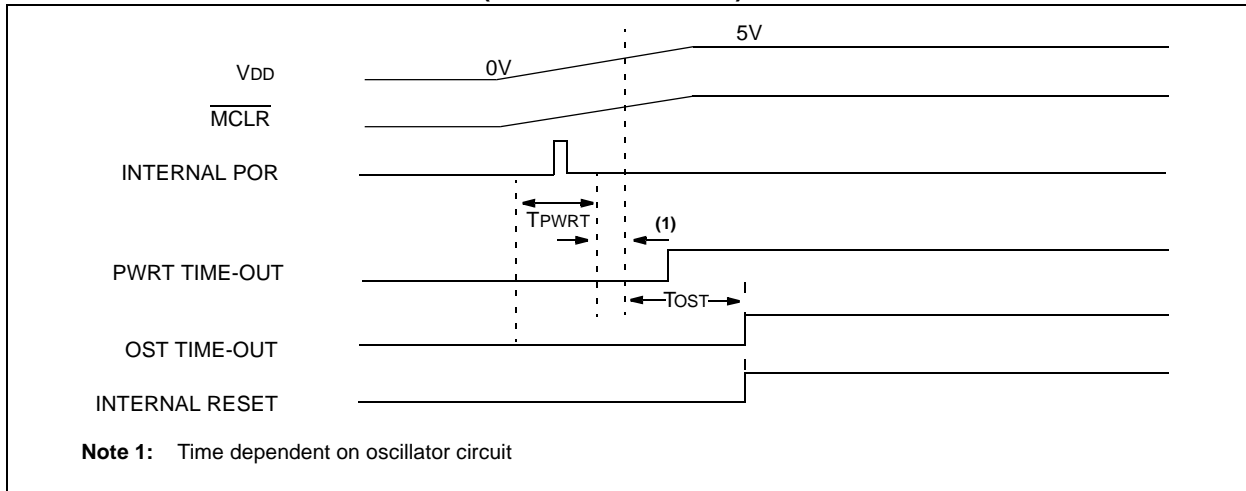**FIGURE 12-8:** TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

FIGURE 12-9: SLOW V_{DD} RISE TIME ($\overline{\text{MCLR}}$ TIED TO V_{DD})

Note 1: Time dependent on oscillator circuit

15.5   Master SSP SPI Mode Timing Waveforms and Requirements

FIGURE 15-18:   **SPI MASTER MODE TIMING (CKE = 0)**
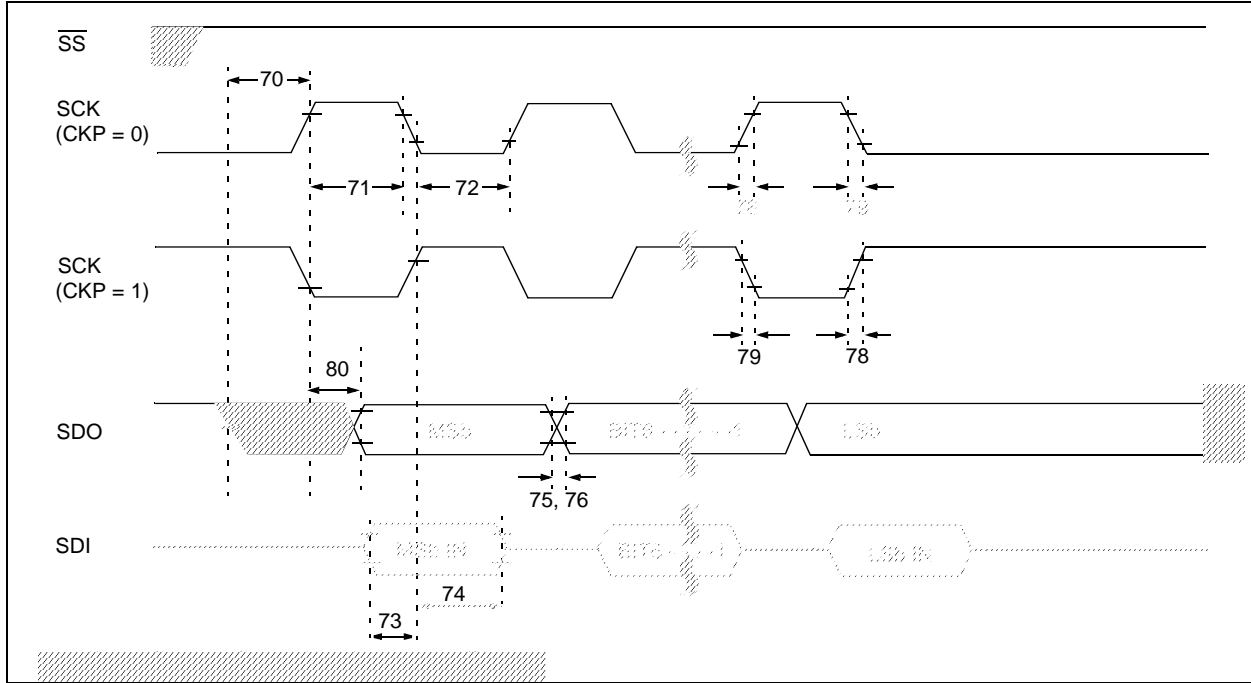
TABLE 15-17:   SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK↓ or SCK↑ input		TCY	—	—	ns	
71*	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A*			Single Byte	40	—	—	ns	**Note 1**
72*	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A*			Single Byte	40	—	—	ns	**Note 1**
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A*	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	**Note 1**
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75*	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX	—	20	45	ns	
76*	TdoF	SDO data output fall time		—	10	25	ns	
78*	TscR	SCK output rise time (Master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX	—	20	45	ns	
79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX	—	—	100	ns	

   *   These parameters are characterized but not tested.
   †   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
 Note 1: Specification 73A is only required if specifications 71A and 72A are used.

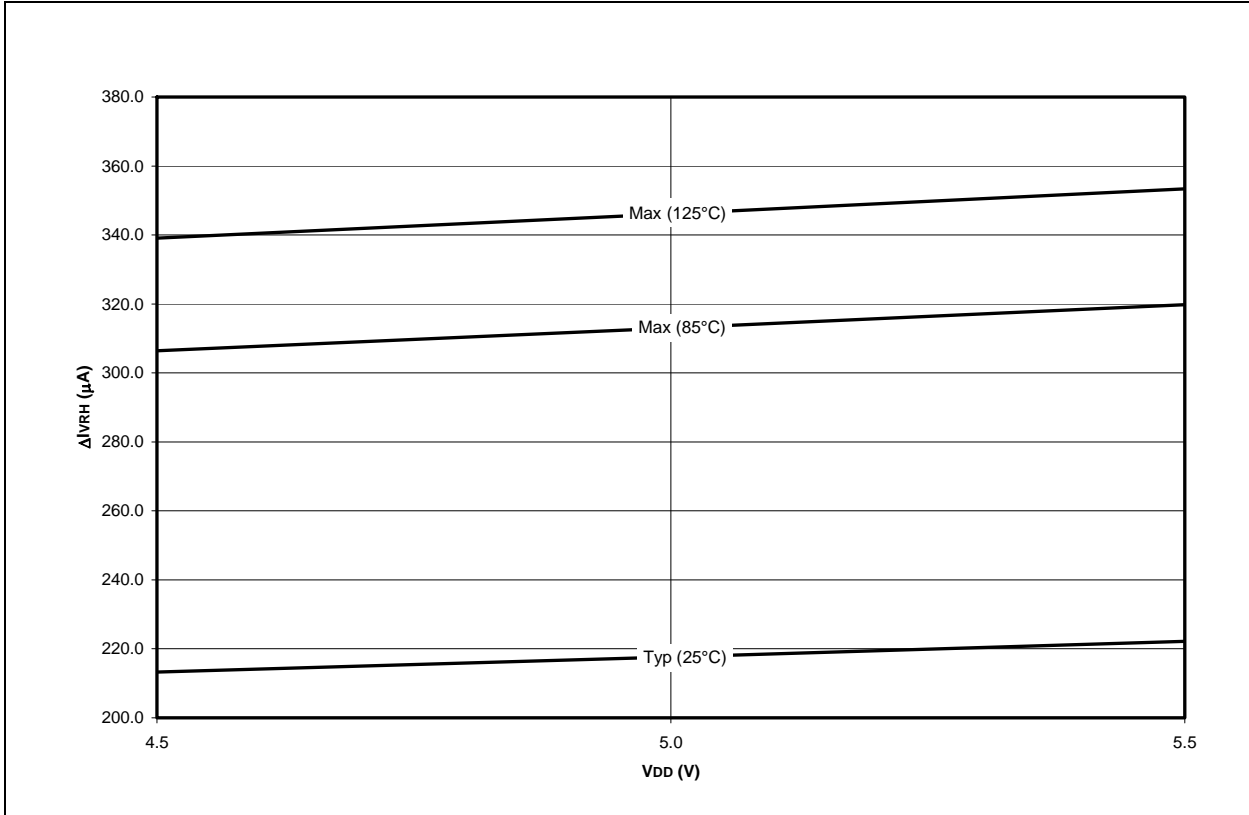**FIGURE 16-22:** **TYPICAL AND MAXIMUM ΔI**VRH **VS. V**DD **(-40°C TO +125°C)**

FIGURE 16-23: **TYPICAL AND MAXIMUM ΔI**LVD **VS. V**DD **(-40°C TO +125°C) (LVD TRIP = 3.0V)**
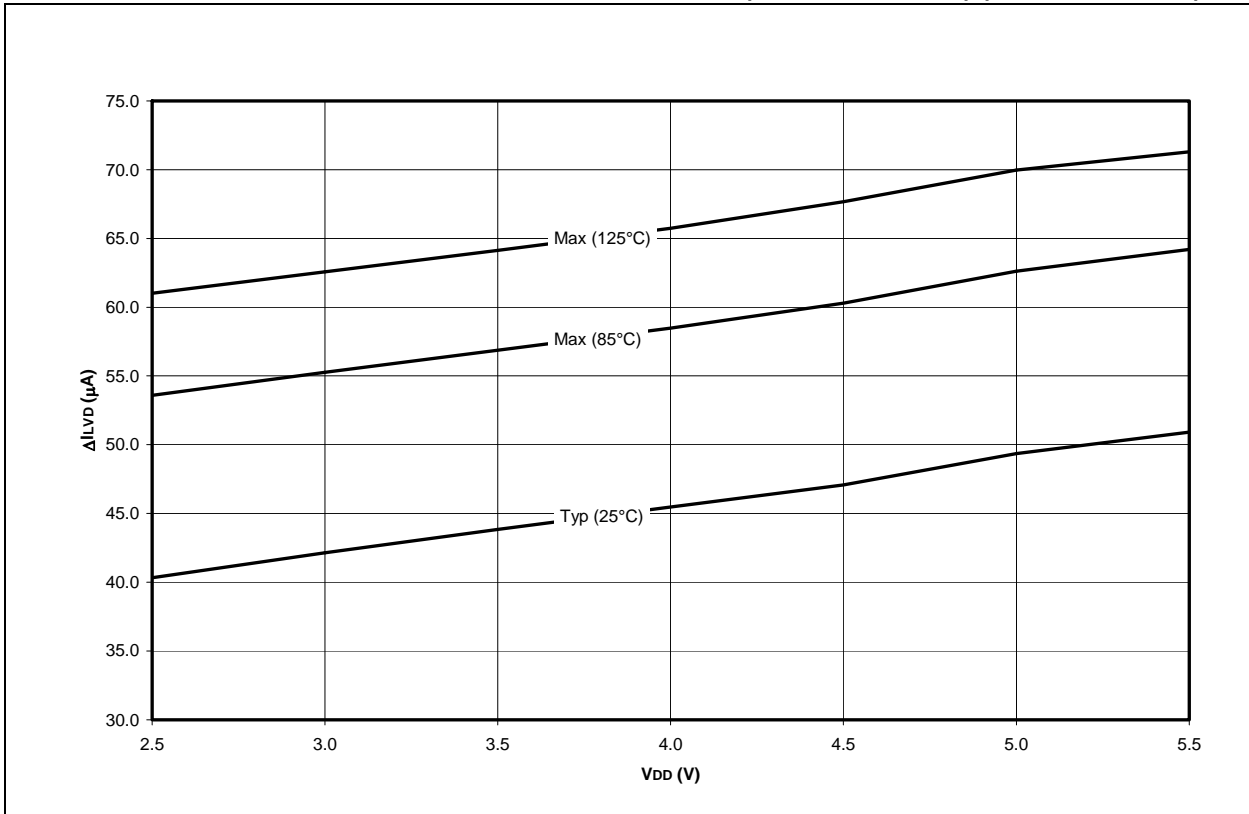
FIGURE 16-26: TYPICAL AND MAXIMUM ∆I$_{BOR}$ VS. V$_{DD}$ (-40°C TO +125°C) (V$_{BOR}$ = 4.5V)
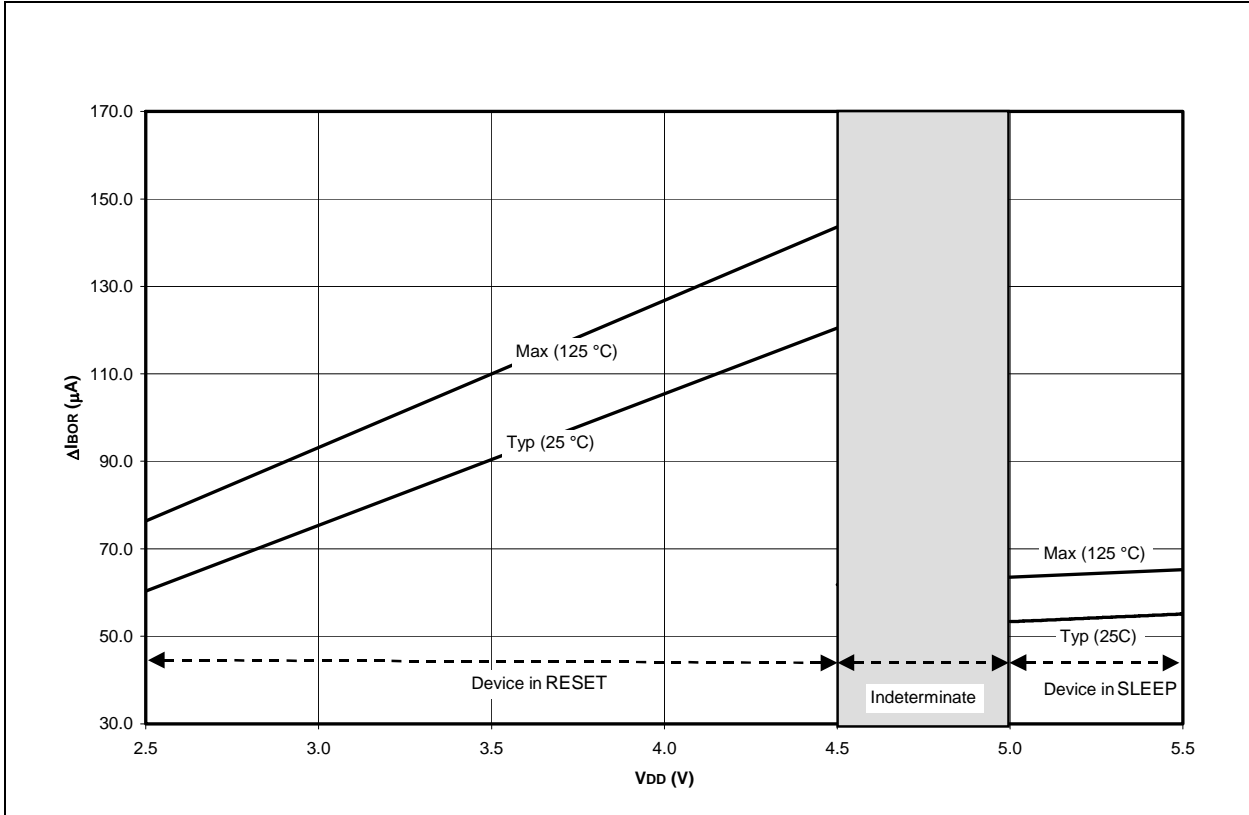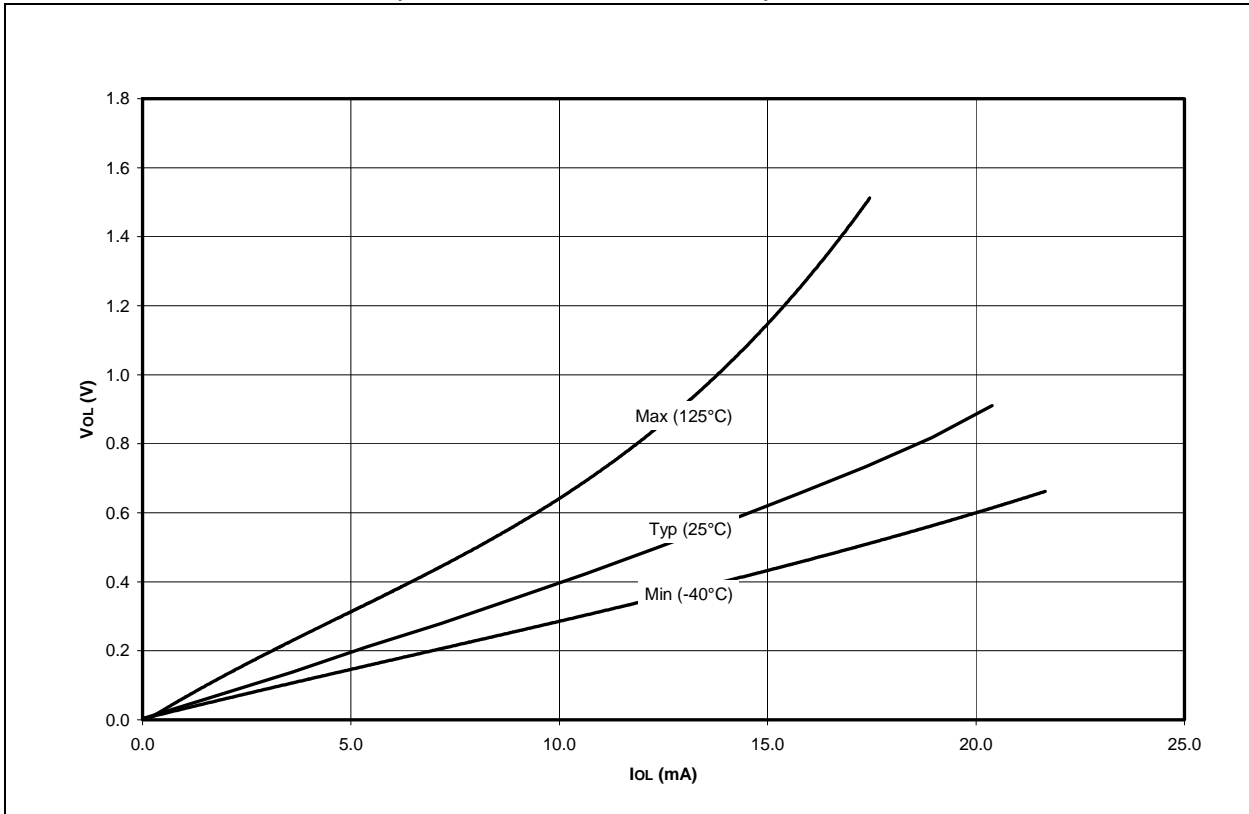

FIGURE 16-27: V$_{OL}$ VS. I$_{OL}$ (-40°C TO +125°C, V$_{DD}$ = 3.0V)

17.6   20-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

<u>DRAWING NOT AVAILABLE</u>

APPENDIX A: REVISION HISTORY

Version	Date	Revision Description
A	09/14/99	This is a new data sheet. However, the devices described in this data sheet are the upgrades to the devices found in the *PIC16C7X Data Sheet*, DS30390E.
B	1/22/02	Electrical Characteristics tables completed and characteristics graphs added. MSSP I^{2}C (Section 9.2) rewritten. General minor changes and corrections.
C	1/28/13	Added a note to each package outline drawing.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support