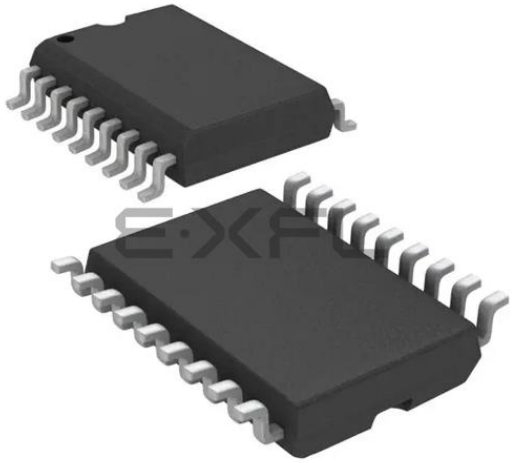

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc717-e-so

FIGURE 3-3: BLOCK DIAGRAM OF RA4/T0CKI

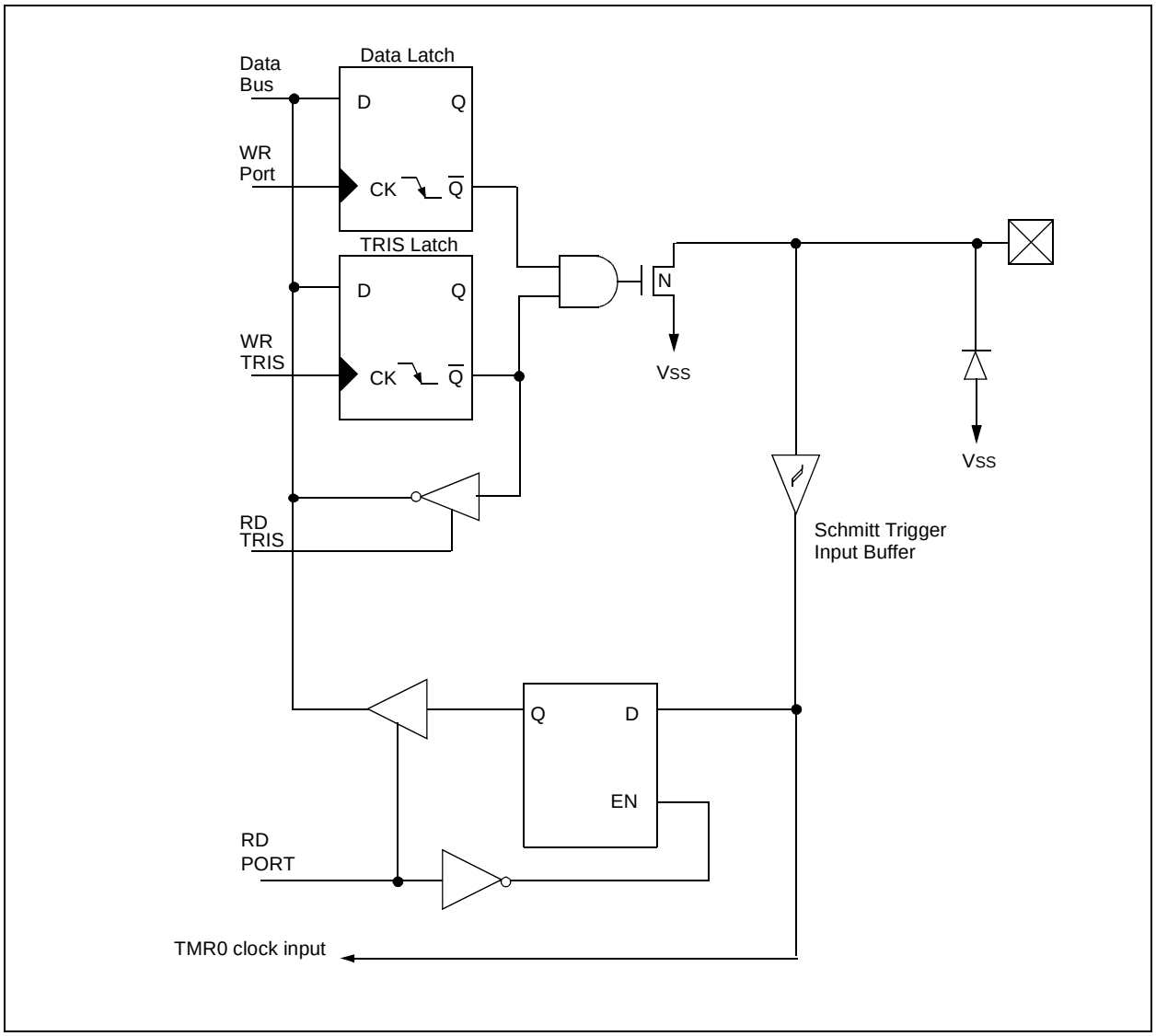
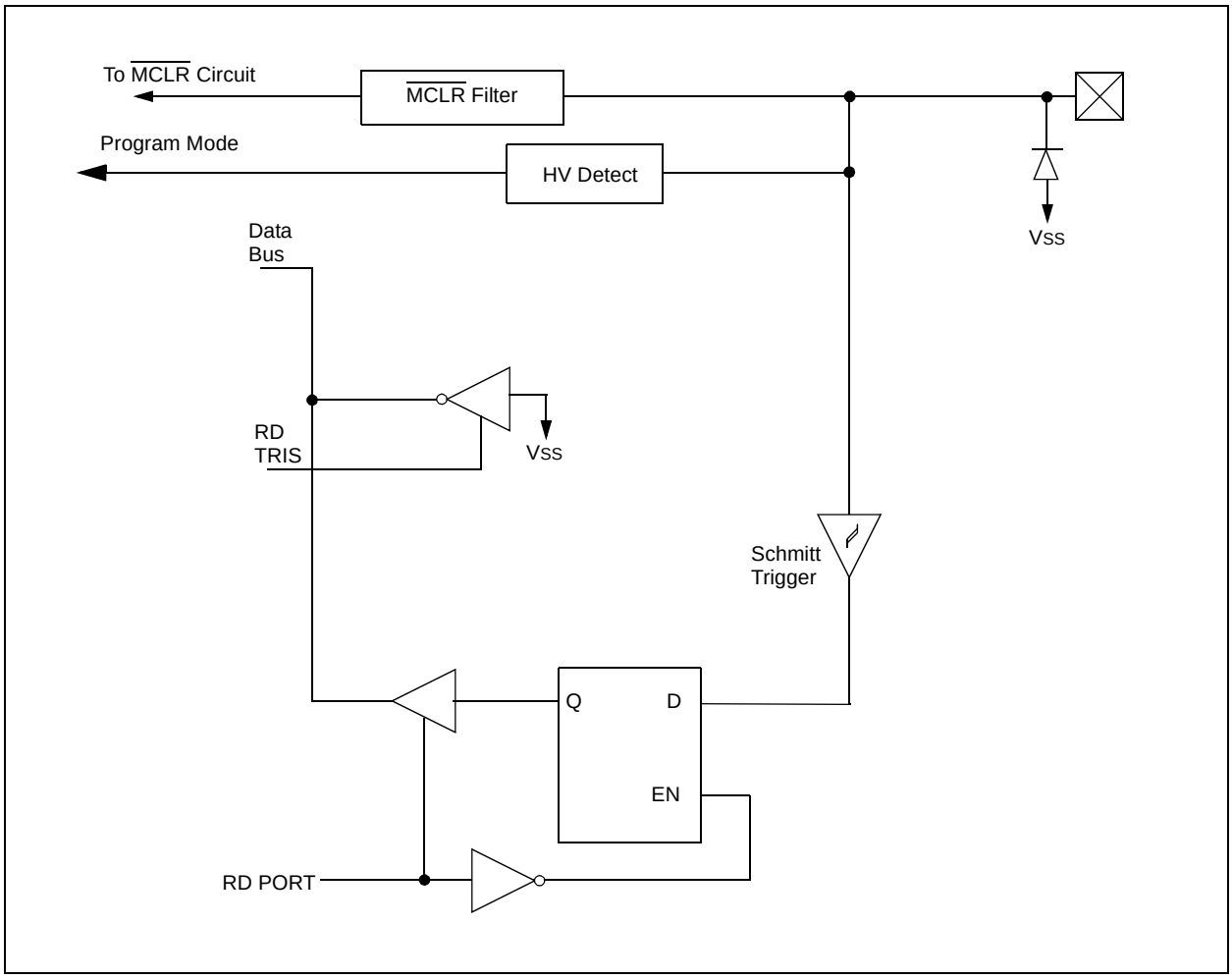


FIGURE 3-4: BLOCK DIAGRAM OF RA5/$\overline{MCLR}$/VPP

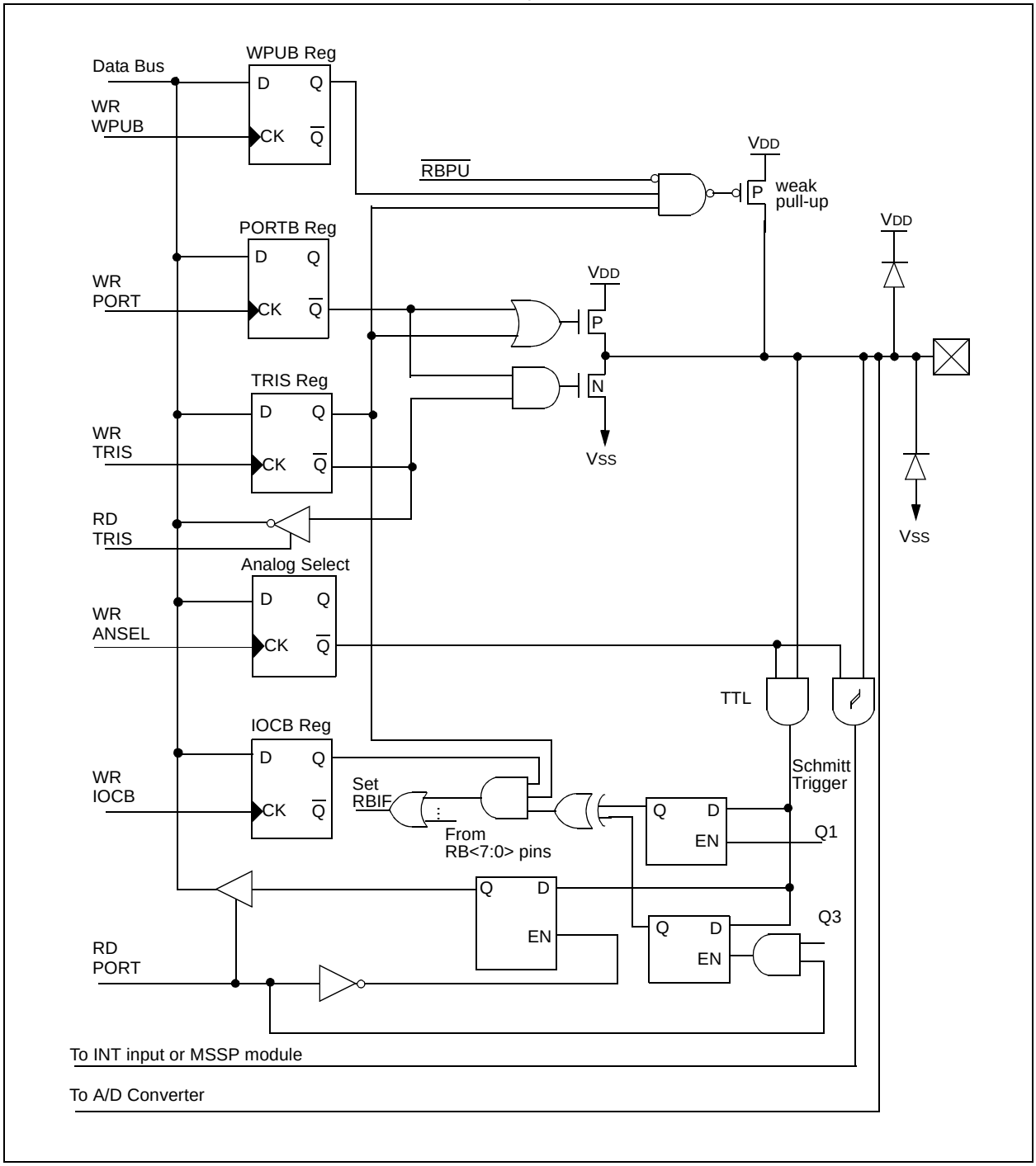


The RB0 pin is multiplexed with the A/D converter analog input 4 and the external interrupt input (RB0/AN4/INT). When the pin is used as analog input, the ANSEL register must have the proper value to select the RB0 pin as Analog mode.

The RB1 pin is multiplexed with the A/D converter analog input 5 and the MSSP module slave select input (RB1/AN5/$\overline{SS}$). When the pin is used as analog input, the ANSEL register must have the proper value to select the RB1 pin as Analog mode.

Note:	Upon RESET, the ANSEL register configures the RB1 and RB0 pins as analog inputs. Both RB1 and RB0 pins will read as '1'.

FIGURE 3-7: BLOCK DIAGRAM OF RB0/AN4/INT, RB1/AN5/$\overline{SS}$ PIN



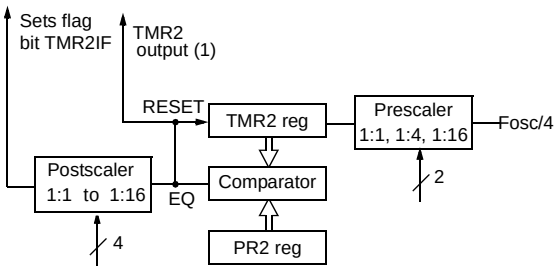
7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

7.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

FIGURE 7-1: Timer2 Block Diagram



Note: TMR2 register output can be software selected by the SSP Module as a baud clock.

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
11h	TMR2	Timer2 register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.

9.1 SPI Mode

The SPI mode allows eight bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ($\overline{SS}$)

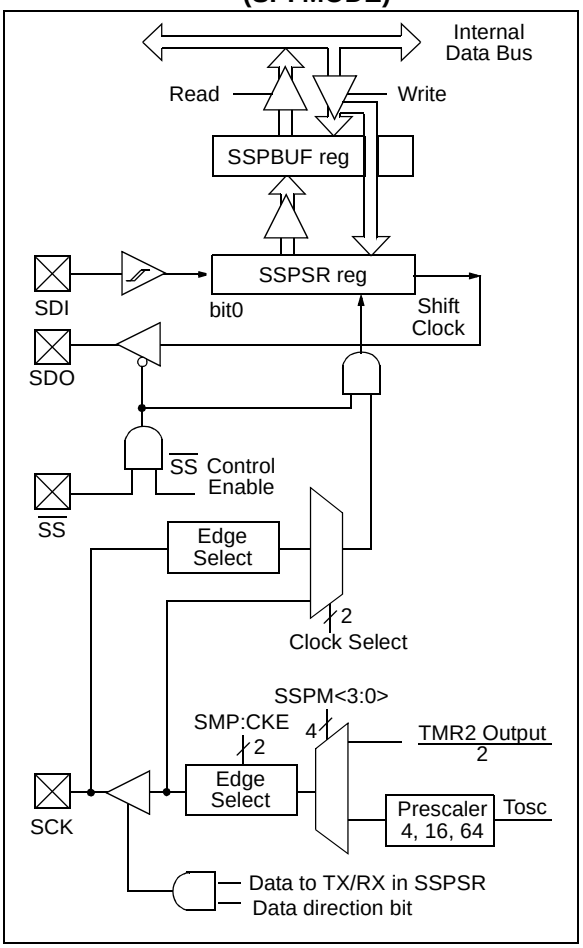
9.1.1 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data input sample phase (middle or end of data output time)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select Mode (Slave mode only)

Figure 9-1 shows the block diagram of the MSSP module when in SPI mode.

FIGURE 9-1: MSSP BLOCK DIAGRAM (SPI MODE)



The MSSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer Register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the eight bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit, BF (SSPSTAT<0>), and the interrupt flag bit, SSPIF (PIR1<3>), are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit WCOL (SSPCON<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

9.2.14 ACKNOWLEDGE SEQUENCE TIMING

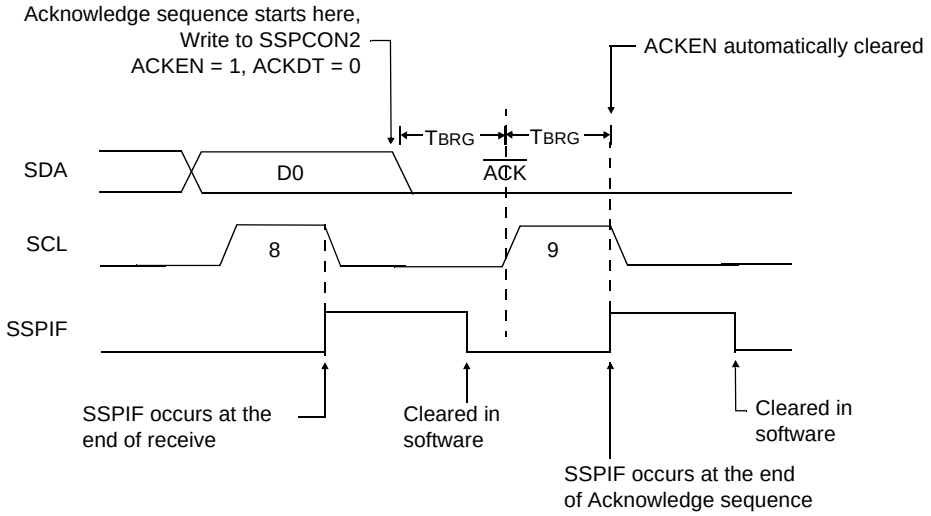
An Acknowledge sequence is enabled by setting the Acknowledge sequence enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit ACKDT (SSPCON2<5>) is presented on the SDA pin. If the user wishes to generate an Acknowledge (ACK), then the ACKDT bit should be cleared. Otherwise, the user should set the ACKDT bit (NACK) before starting an Acknowledge sequence. The baud rate generator is then loaded from SSPADD<6:0> and counts for one rollover period (TBRG). The SCL pin is then de-asserted (pulled high). When the SCL pin is sampled high (clock arbitration), the baud rate generator is reloaded and counts for another TBRG. At the completion of the TBRG period, the following events occur (see Figure 9-20):

- The SCL pin is pulled low.
- The ACKEN bit is automatically cleared.
- The baud rate generator is turned off.
- The MSSP module goes into IDLE mode.

9.2.14.1 WCOL STATUS FLAG

If the user writes the SSPBUF when an Acknowledge sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 9-20: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one baud rate generator period.

9.2.17.2 BUS COLLISION DURING A REPEATED START CONDITION

During a Repeated START condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level.

b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the master module de-asserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0>, and counts down to '0'. The SCL pin is then de-asserted, and when sampled high, the SDA pin is sampled. If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0'). If however SDA is sampled high, then the BRG is reloaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs, because no two masters can assert SDA at exactly the same time.

If, however, SCL goes from high to low before the BRG times out and SDA has not already been asserted, then a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated START condition.

If at the end of the BRG time-out both SCL and SDA are still high, the SDA pin is driven low, the BRG is reloaded, and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated START condition is complete (Figure 9-27).

FIGURE 9-27: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

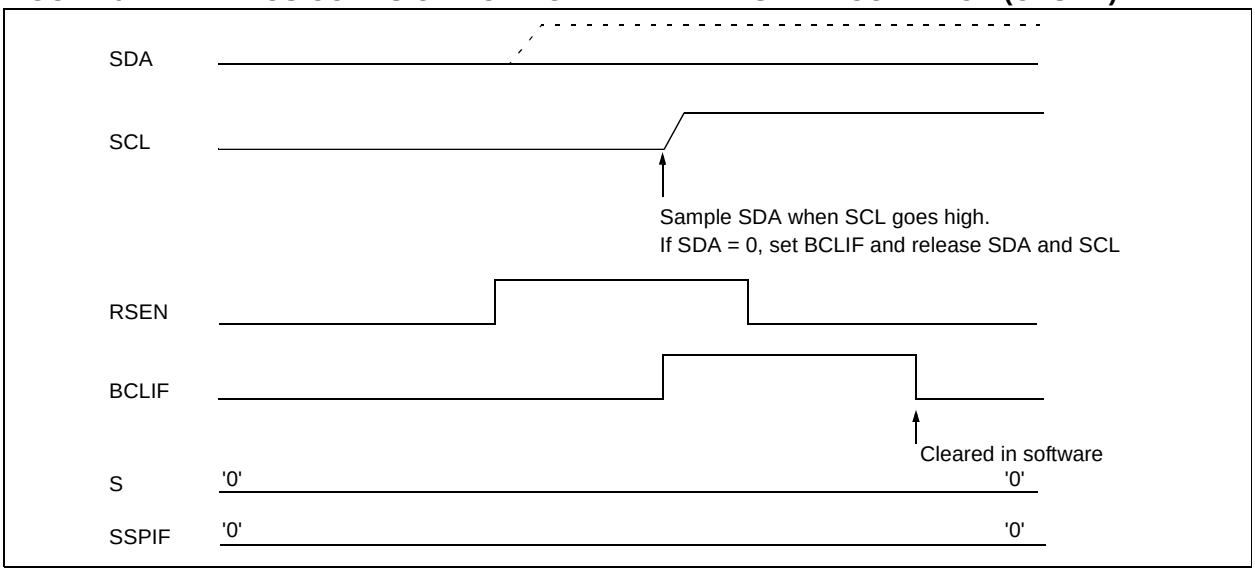
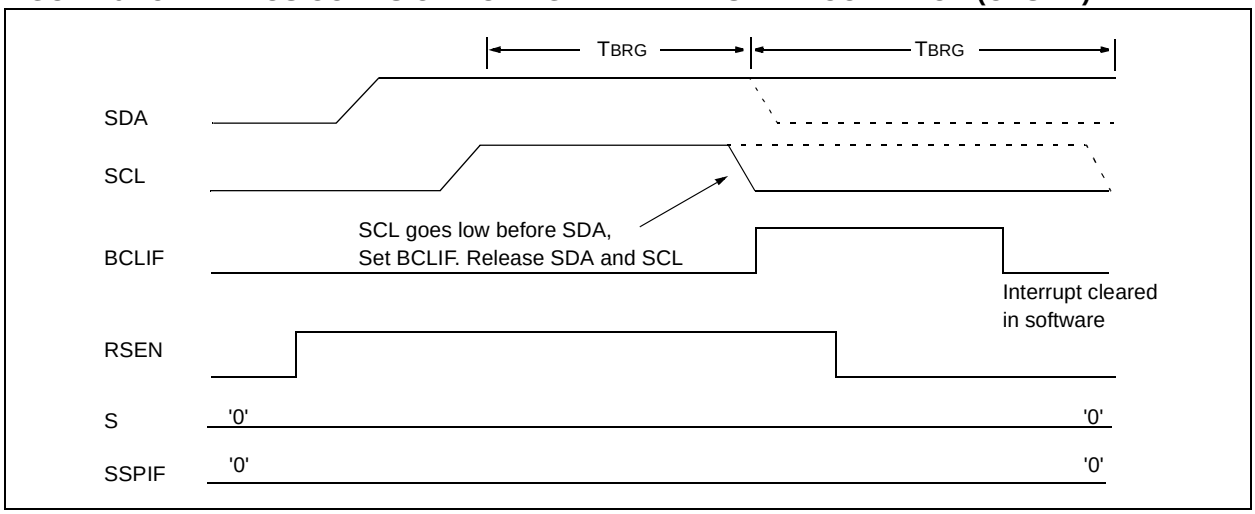


FIGURE 9-28: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



9.2.18 CONNECTION CONSIDERATIONS FOR I²C BUS

For Standard mode I²C bus devices, the values of resistors R_p and R_s in Figure 9-31 depends on the following parameters

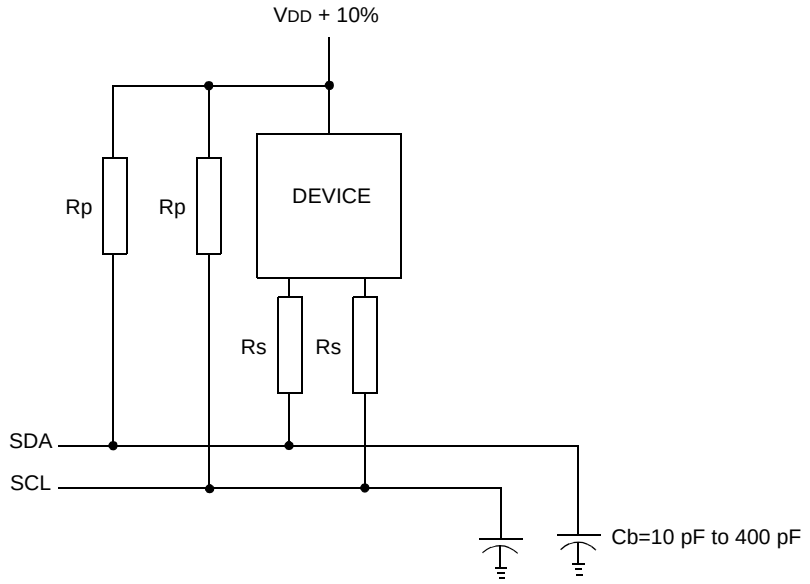
- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA at VOL max = 0.4V for the specified output stages. For example, with a supply voltage of VDD = 5V±10% and VOL max = 0.4V at 3 mA, $R_{p\ min}$ = (5.5-0.4)/0.003 = 1.7 kΩ. VDD as a function of R_p is shown in Figure 9-31. The desired noise margin of 0.1VDD for the low level limits the maximum value of R_s. Series resistors are optional and used to improve ESD susceptibility.

The bus capacitance is the total capacitance of wire, connections, and pins. This capacitance limits the maximum value of R_p due to the specified rise time (Figure 9-31).

The SMP bit is the slew rate control enabled bit. This bit is in the SSPSTAT register, and controls the slew rate of the I/O pins when in I²C mode (master or slave).

FIGURE 9-31: SAMPLE DEVICE CONFIGURATION FOR I²C BUS



Note: I²C devices with input levels related to VDD must have one common supply line to which the pull-up resistor is also connected.

TABLE 9-3: REGISTERS ASSOCIATED WITH I²C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	$\overline{MCLR}$, WDT
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
0Dh	PIR2	LVDIF	—	—	—	BCLIF	—	—	CCP2IF	0--- 0--0	0--- 0--0
8Dh	PIE2	LVDIE	—	—	—	BCLIE	—	—	CCP2IE	0--- 0--0	0--- 0--0
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
93h	SSPADD	Synchronous Serial Port (I²C Mode) Address Register								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the MSSP in I²C mode.

10.3 Low Voltage Detect (LVD)

This module is used to generate an interrupt when the supply voltage falls below a specified “trip” voltage. This module operates completely under software control. This allows a user to power the module on and off to periodically monitor the supply voltage, and thus minimize total current consumption.

The LVD module is enabled by setting the LVDEN bit in the LVDCON register. The “trip point” voltage is the minimum supply voltage level at which the device can operate before the LVD module asserts an interrupt. When the supply voltage is equal to or less than the trip point, the module will generate an interrupt signal setting interrupt flag bit LVDIF. If interrupt enable bit LVDIE was set, then an interrupt is generated. The LVD interrupt can wake the device from SLEEP. The "trip point" voltage is software programmable to any one of 16 values, five of which are reserved (See Figure 10-1). The trip point is selected by programming the LV<3:0> bits (LVDCON<3:0>).

Note:	The LVDIF bit can not be cleared until the supply voltage rises above the LVD trip point. If interrupts are enabled, clear the LVDIE bit once the first LVD interrupt occurs to prevent reentering the interrupt service routine immediately after exiting the ISR.

Once the LV bits have been programmed for the specified trip voltage, the low-voltage detect circuitry is then enabled by setting the LVDEN (LVDCON<4>) bit.

If the bandgap reference voltage is previously unused by either the brown-out circuitry or the voltage reference circuitry, then the bandgap circuit requires a time to start-up and become stable before a low voltage condition can be reliably detected. The low-voltage interrupt flag is prevented from being set until the bandgap has reached a stable reference voltage.

When the bandgap is stable the BGST (LVDCON<5>) bit is set indicating that the low-voltage interrupt flag bit is released to be set if VDD is equal to or less than the LVD trip point.

10.3.1 EXTERNAL ANALOG VOLTAGE INPUT

The LVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when LV<3:0> = 1111. When these bits are set the comparator input is multiplexed from an external input pin (RA1/AN1/LVDIN).

11.4 A/D Conversions

Example 11-1 shows an example that performs an A/D conversion. The port pins are configured as analog inputs. The analog reference V_{REF+} is the device AV_{DD} and the analog reference V_{REF-} is the device AV_{SS}. The A/D interrupt is enabled and the A/D conversion clock is T_{RC}. The conversion is performed on the AN0 channel.

EXAMPLE 11-1: PERFORMING AN A/D CONVERSION

```
    BSF     STATUS, RP0    ;Select Bank 1
    CLRF    ADCON1         ;Configure A/D Voltage Reference
    MOVLW   0x01
    MOVWF   ANSEL          ;disable AN0 digital input buffer
    MOVWF   TRISA          ;RA0 is input mode
    BSF     PIE1, ADIE     ;Enable A/D interrupt
    BCF     STATUS, RP0    ;Select Bank 0
    MOVLW   0xC1           ;RC clock, A/D is on,
                           ;Ch 0 is selected
    MOVWF   ADCON0         ;
    BCF     PIR1, ADIF     ;Clear A/D Int Flag
    BSF     INTCON, PEIE   ;Enable Peripheral
    BSF     INTCON, GIE    ;Enable All Interrupts
;
; Ensure that the required sampling time for the
; selected input channel has lapsed. Then the
; conversion may be started.
    BSF     ADCON0, GO     ;Start A/D Conversion
            :              ;The ADIF bit will be
                           ;set and the GO/DONE bit
            :              ;cleared upon completion-
                           ;of the A/D conversion.
; Wait for A/D completion and read ADRESH:ADRESL for result.
```

REGISTER 12-1: CONFIGURATION WORD FOR 16C717/770/771 DEVICE

$\overline{CP}$	$\overline{CP}$	BORV1	BORV0	$\overline{CP}$	$\overline{CP}$	—	BODEN	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	FOSC1	FOSC0
bit13													bit0

bit 13-12, 9-8 **$\overline{CP}$: Program Memory Code Protection**
1 = Code protection off
0 = All program memory is protected(2)

bit 11-10: **BORV<1:0>:** Brown-out Reset Voltage bits
00 = V_{BOR} set to 4.5V
01 = V_{BOR} set to 4.2V
10 = V_{BOR} set to 2.7V
11 = V_{BOR} set to 2.5V

bit 7: **Unimplemented:** Read as '1'

bit 6: **BODEN:** Brown-out Detect Reset Enable bit(1)
1 = Brown-out Detect Reset enabled
0 = Brown-out Detect Reset disabled

bit 5: **MCLRE**: RA5/$\overline{MCLR}$ pin function select
1 = RA5/$\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = RA5/$\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to V_{DD}

bit 4: **$\overline{PWRTE}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0: **FOSC<2:0>:** Oscillator Selection bits
000 = LP oscillator: Crystal/Resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = XT oscillator: Crystal/Resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
010 = HS oscillator: Crystal/Resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN function on RA7/OSC1/CLKIN
100 = INTRC oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
101 = INTRC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
110 = ER oscillator: I/O function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN
111 = ER oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN

Note 1: Enabling Brown-out Reset automatically enables the Power-up Timer (PWRT), regardless of the value of bit $\overline{PWRTE}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.
2: All of the $\overline{CP}$ bits must be given the same value to enable code protection.

Legend			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

13.1 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

IORLW	Inclusive OR Literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k $\rightarrow$ (W)
Status Affected:	None
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 127$
Operation:	(W) $\rightarrow$ (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

14.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

14.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable V_{DD} and V_{PP} supplies, which allow it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

14.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

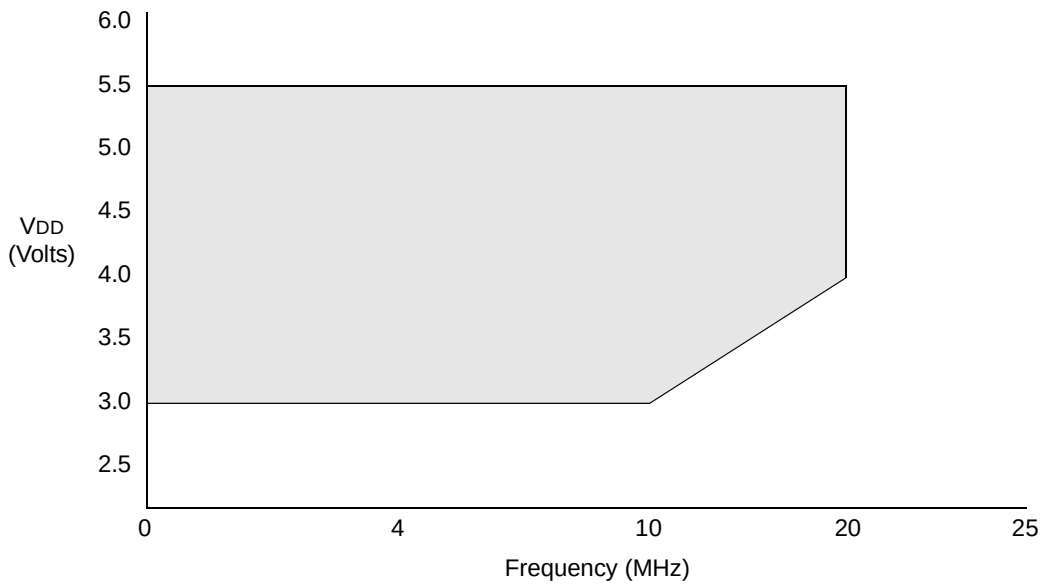
14.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

14.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I^2C™ bus and separate headers for connection to an LCD module and a keypad.

FIGURE 15-3: PIC16LC717/770/771 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ 0°C, +70°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 16-22: TYPICAL AND MAXIMUM ΔIVRH VS. VDD (-40°C TO +125°C)

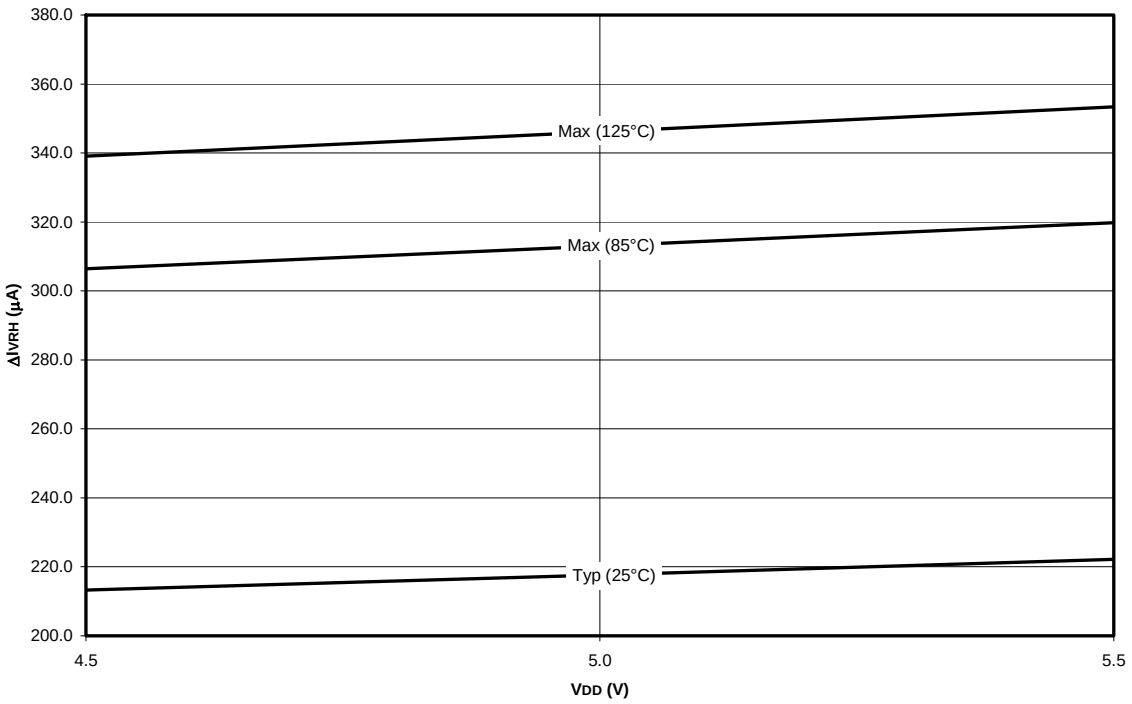
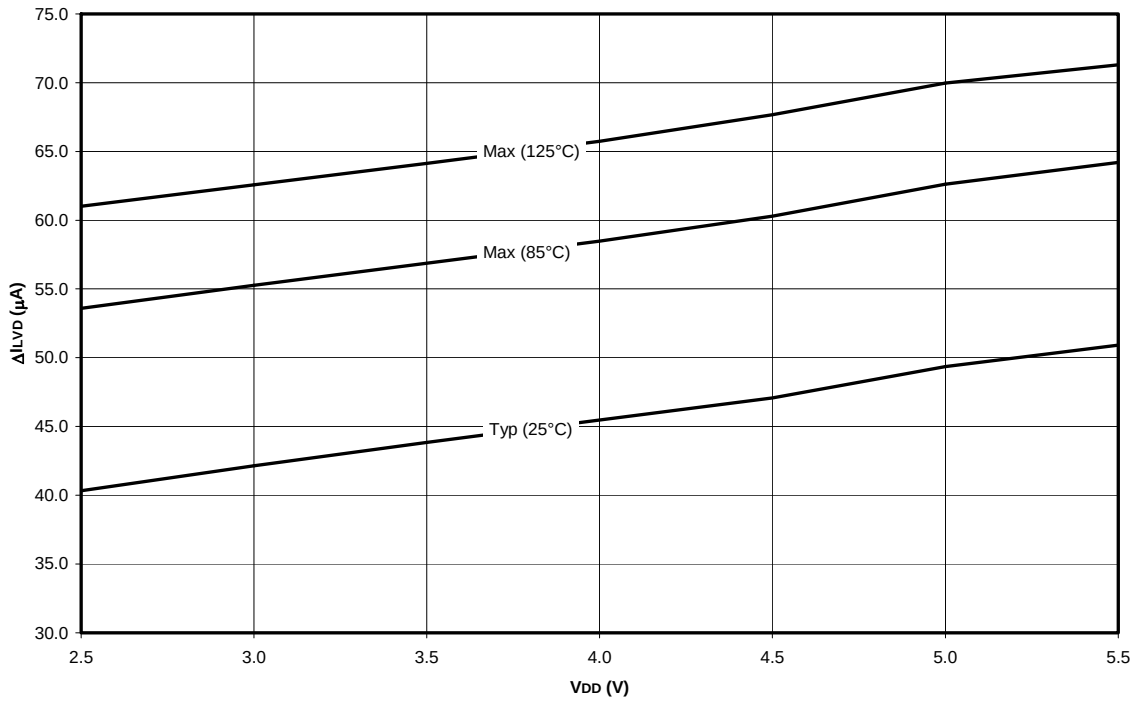


FIGURE 16-23: TYPICAL AND MAXIMUM ΔILVD VS. VDD (-40°C TO +125°C) (LVD TRIP = 3.0V)



NOTES:

APPENDIX A: REVISION HISTORY

Version	Date	Revision Description
A	09/14/99	This is a new data sheet. However, the devices described in this data sheet are the upgrades to the devices found in the *PIC16C7X Data Sheet*, DS30390E.
B	1/22/02	Electrical Characteristics tables completed and characteristics graphs added. MSSP I^2C (Section 9.2) rewritten. General minor changes and corrections.
C	1/28/13	Added a note to each package outline drawing.

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PIC16C717/770/771 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16C771 :	VDD range 4.0V to 5.5V
	PIC16C771T :	VDD range 4.0V to 5.5V (Tape/Reel)
	PIC16LC771 :	VDD range 2.5V to 5.5V
	PIC16LC771T:	VDD range 2.5V to 5.5V (Tape/Reel)
Temperature Range:	- =	0°C to +70°C
	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package	JW =	Windowed CERDIP
	SO =	SOIC
	P =	PDIP
	SS =	SSOP
Pattern	QTP, SQTP, Code or Special Requirements. Blank for OTP and Windowed devices.	

Examples:

a) PIC16C771/P Commercial Temp., PDIP package, normal VDD limits

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)