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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lc717-e-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic16lc717-e-ss</a>

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# PIC16C717/770/771

**FIGURE 2-3: REGISTER FILE MAP**

File Address		File Address		File Address		File Address	
Indirect addr. <sup>(*)</sup>	00h	Indirect addr. <sup>(*)</sup>	80h	Indirect addr. <sup>(*)</sup>	100h	Indirect addr. <sup>(*)</sup>	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh		18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh		18Eh
TMR1H	0Fh		8Fh	PMADRH	10Fh		18Fh
T1CON	10h		90h		110h		190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h		116h		196h
CCP1CON	17h	P1DEL	97h		117h		197h
	18h		98h		118h		198h
	19h		99h		119h		199h
	1Ah		9Ah		11Ah		19Ah
	1Bh	REFCON	9Bh		11Bh		19Bh
	1Ch	LVDCON	9Ch		11Ch		19Ch
	1Dh	ANSEL	9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes			
			EFh		16Fh		1EFh
		accesses 70h-7Fh	F0h	accesses 70h - 7Fh	170h	accesses 70h - 7Fh	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

 Unimplemented data memory locations, read as '0'.  
 \* Not a physical register.

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## 2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The special function registers can be classified into two sets; core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in that peripheral feature section.

**TABLE 2-1: PIC16C717/770/771 SPECIAL FUNCTION REGISTER SUMMARY**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
<b>Bank 0</b>											
00h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
01h	TMR0	Timer0 module's register								xxxx xxxx	45
02h <sup>(3)</sup>	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	22
03h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	14
04h <sup>(3)</sup>	FSR	Indirect data memory address pointer								xxxx xxxx	23
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	25
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xx11	33
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter				---	0 0000	22
0Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBFIF	0000 000x	16
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	0---0000	18
0Dh	PIR2	LVDIF	—	—	—	BCLIF	—	—	—	0---0---	20
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	47
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	47
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	47
11h	TMR2	Timer2 module's register								0000 0000	51
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	51
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	70
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	67
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	54
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	54
17h	CCP1CON	PWM1M1	PWM1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	53
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	A/D High Byte Result Register								xxxx xxxx	107
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	$\overline{GO/DONE}$	CHS3	ADON	0000 0000	107

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.

Shaded locations are unimplemented, read as '0'.

**Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

**2:** Other (non Power-up) Resets include external RESET through MCLR and Watchdog Timer Reset.

**3:** These registers can be addressed from any bank.

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**TABLE 2-1: PIC16C717/770/771 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 2											
100h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
101h	TMR0	Timer0 module's register								xxxx xxxx	45
102h <sup>(3)</sup>	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	22
103h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	14
104h <sup>(3)</sup>	FSR	Indirect data memory address pointer								xxxx xxxx	23
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xx11	33
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter				---0 0000	22	
10Bh <sup>(3)</sup>	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	16
10Ch	PMDATL	Program memory read data low								xxxx xxxx	
10Dh	PMADRL	Program memory read address low								xxxx xxxx	
10Eh	PMDATH	—	—	Program memory read data high				--xx xxxx			
10Fh	PMADRH	—	—	—	—	Program memory read address high			---- xxxx		
110h-11Fh	—	Unimplemented								—	—
Bank 3											
180h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	15
182h <sup>(3)</sup>	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	22
183h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	14
184h <sup>(3)</sup>	FSR	Indirect data memory address pointer								xxxx xxxx	23
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	33
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter				---0 0000	22	
18Bh <sup>(3)</sup>	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	16
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	
18Dh-18Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.

Shaded locations are unimplemented, read as '0'.

**Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

**2:** Other (non Power-up) Resets include external RESET through MCLR and Watchdog Timer Reset.

**3:** These registers can be addressed from any bank.

## 3.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

### 3.1 I/O Port Analog/Digital Mode

The PIC16C717/770/771 have two I/O ports: PORTA and PORTB. Some of these port pins are mixed-signal (can be digital or analog). When an analog signal is

present on a pin, the pin must be configured as an analog input to prevent unnecessary current draw from the power supply. The Analog Select Register (ANSEL) allows the user to individually select the Digital/Analog mode on these pins. When the Analog mode is active, the port pin will always read 0.

**Note 1:** On a Power-on Reset, the ANSEL register configures these mixed-signal pins as Analog mode.

**2:** If a pin is configured as Analog mode, the RA pin will always read '0' and RB pin will always read '1', even if the digital output is active.

#### REGISTER 3-1: ANALOG SELECT REGISTER (ANSEL: 9Dh)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
—	—	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	
bit 7								bit 0

bit 7-6 **Reserved:** Do not use

bit 5-0 **ANS<5:0>:** Analog Select between analog or digital function on pins AN<5:0>, respectively.  
 0 = Digital I/O. Pin is assigned to port or special function.  
 1 = Analog Input. Pin is assigned as analog input.

**Note:** Setting a pin to an analog input disables the digital input buffer on the pin. The corresponding TRIS bit should be set to Input mode when using pins as analog inputs.

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 - n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

### 3.2 PORTA and the TRISA Register

PORTA is a 8-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pins RA<3:0> are multiplexed with analog functions, such as analog inputs to the A/D converter, analog VREF inputs, and the onboard bandgap reference outputs. When the analog peripherals are using any of

these pins as analog input/output, the ANSEL register must have the proper value to individually select the Analog mode of the corresponding pins.

**Note:** Upon RESET, the ANSEL register configures the RA<3:0> pins as analog inputs. All RA<3:0> pins will read as '0'.

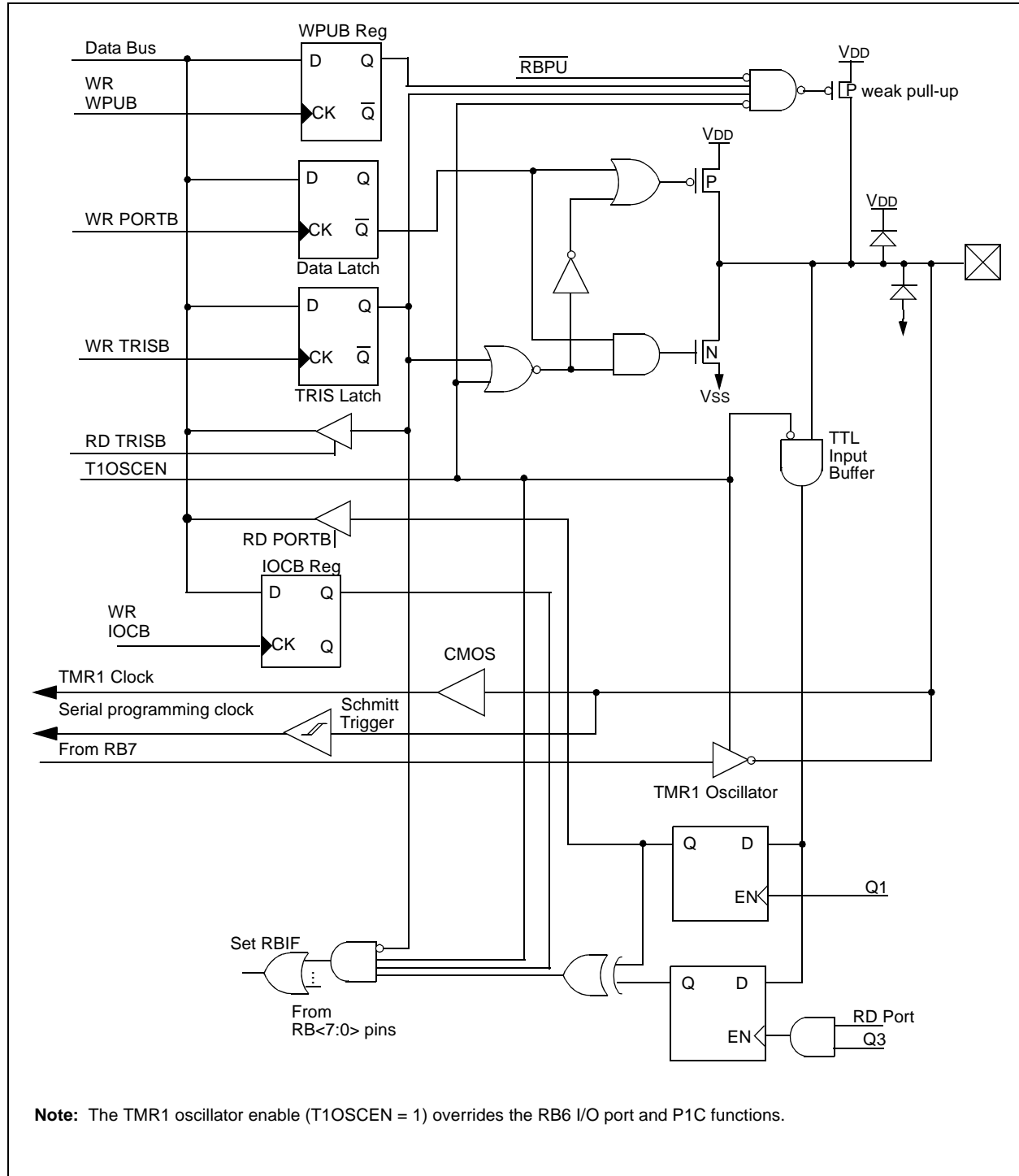
Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output.

Pin RA5 is multiplexed with the device RESET (MCLR) and programming input (VPP) functions. The RA5/MCLR/VPP input only pin has a Schmitt Trigger input buffer. All other RA port pins have Schmitt Trigger input buffers and full CMOS output buffers.

Pins RA6 and RA7 are multiplexed with the oscillator input and output functions.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

**FIGURE 3-9: BLOCK DIAGRAM OF RB6/T1OSO/T1CKI/P1C**



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NOTES:

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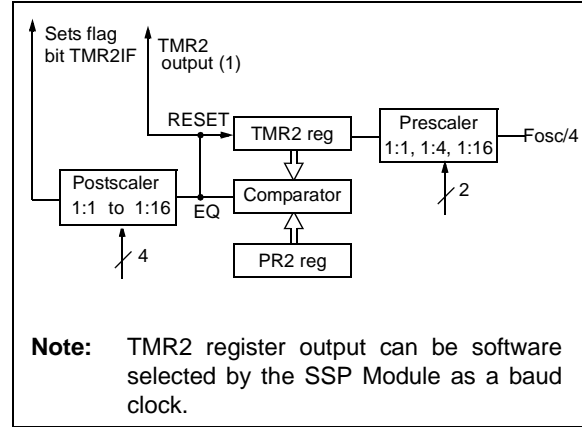
## 7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

## 7.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

**FIGURE 7-1: Timer2 Block Diagram**



**TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh,10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
11h	TMR2	Timer2 register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.

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## REGISTER 9-2: SYNC SERIAL PORT CONTROL REGISTER (SSPCON: 14h) (CONTINUED)

bit 3-0      **SSPM<3:0>**: Synchronous Serial Port Mode Select bits

0000 = SPI Master mode, clock = Fosc/4  
0001 = SPI Master mode, clock = Fosc/16  
0010 = SPI Master mode, clock = Fosc/64  
0011 = SPI Master mode, clock = TMR2 output/2  
0100 = SPI Slave mode, clock = SCK pin.  $\overline{SS}$  pin control enabled.  
0101 = SPI Slave mode, clock = SCK pin.  $\overline{SS}$  pin control disabled.  $\overline{SS}$  can be used as I/O pin.  
0110 = I<sup>2</sup>C Slave mode, 7-bit address  
0111 = I<sup>2</sup>C Slave mode, 10-bit address  
1000 = I<sup>2</sup>C Master mode, clock = Fosc / (4 • (SSPADD+1) )  
1001 = Reserved  
1010 = Reserved  
1011 = Firmware controlled Master mode (slave idle)  
1100 = Reserved  
1101 = Reserved  
1110 = 7-bit Slave mode with START and STOP condition interrupts  
1111 = 10-bit Slave mode with START and STOP condition interrupts

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

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## 9.2.17 MULTI-MASTER COMMUNICATION, BUS COLLISION, AND BUS ARBITRATION

Multi-master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, bus arbitration is initiated when one master outputs a '1' on SDA (by letting SDA float high) and another master asserts a '0'. If the expected data on SDA is a '1' and the data sampled on the SDA pin = '0', then a bus collision has taken place. The master that expected a '1' will set the Bus Collision Interrupt Flag, BCLIF, and reset the I<sup>2</sup>C port to its IDLE state. (Figure 9-23).

A bus collision during transmit results in the following events:

- The transmission is halted.
- The BF flag is cleared
- The SDA and SCL lines are de-asserted
- The restriction on writing to the SSPBUF during transmission is lifted.

When the user services the bus collision interrupt service routine, and if the I<sup>2</sup>C bus is free, the user can resume communication by asserting a START condition.

A bus collision during a START, Repeated START, STOP or Acknowledge condition results in the following events:

- The condition is aborted.
- The SDA and SCL lines are de-asserted.
- The respective control bits in the SSPCON2 register are cleared.

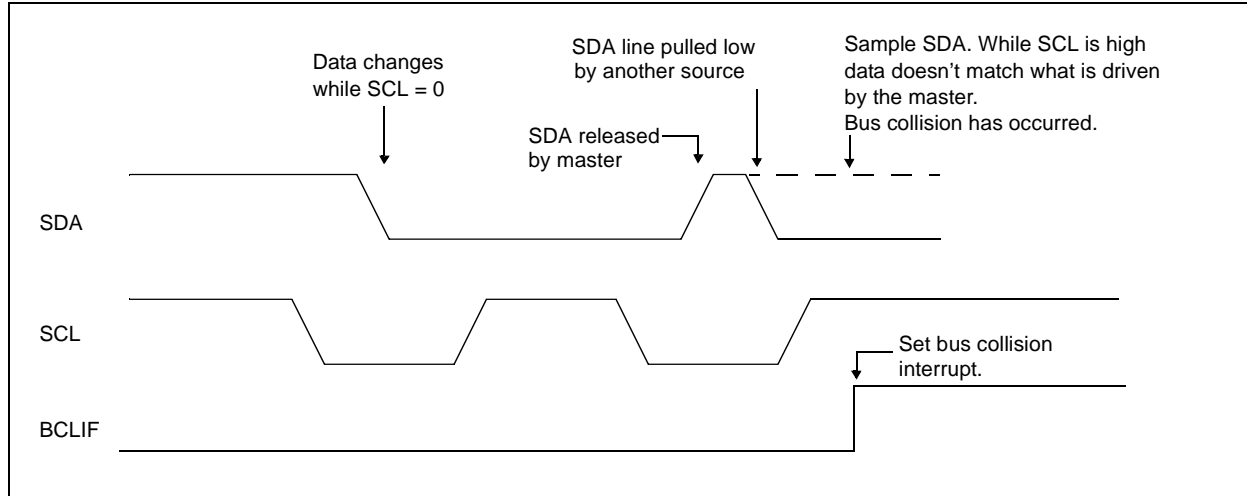
When the user services the bus collision interrupt service routine, and if the I<sup>2</sup>C bus is free, the user can resume communication by asserting a START condition.

The Master will continue to monitor the SDA and SCL pins, and if a STOP condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of START and STOP conditions allows the determination of when the bus is free. Control of the I<sup>2</sup>C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is idle and the S and P bits are cleared.

**FIGURE 9-23: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE**



## 9.2.18 CONNECTION CONSIDERATIONS FOR I<sup>2</sup>C BUS

For Standard mode I<sup>2</sup>C bus devices, the values of resistors  $R_p$  and  $R_s$  in Figure 9-31 depends on the following parameters

- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

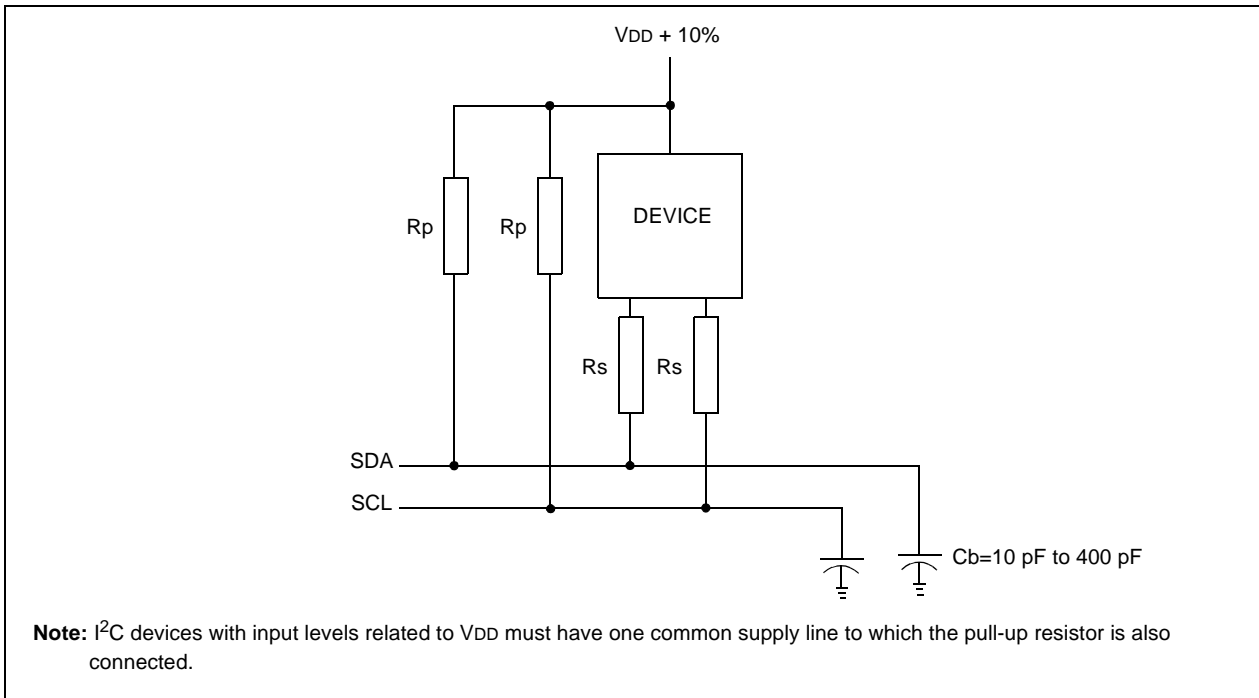
The supply voltage limits the minimum value of resistor  $R_p$  due to the specified minimum sink current of 3 mA at  $V_{OL\ max} = 0.4V$  for the specified output stages. For

example, with a supply voltage of  $V_{DD} = 5V \pm 10\%$  and  $V_{OL\ max} = 0.4V$  at 3 mA,  $R_{p\ min} = (5.5-0.4)/0.003 = 1.7\ k\Omega$ .  $V_{DD}$  as a function of  $R_p$  is shown in Figure 9-31. The desired noise margin of  $0.1V_{DD}$  for the low level limits the maximum value of  $R_s$ . Series resistors are optional and used to improve ESD susceptibility.

The bus capacitance is the total capacitance of wire, connections, and pins. This capacitance limits the maximum value of  $R_p$  due to the specified rise time (Figure 9-31).

The SMP bit is the slew rate control enabled bit. This bit is in the SSPSTAT register, and controls the slew rate of the I/O pins when in I<sup>2</sup>C mode (master or slave).

**FIGURE 9-31: SAMPLE DEVICE CONFIGURATION FOR I<sup>2</sup>C BUS**



**TABLE 9-3: REGISTERS ASSOCIATED WITH I<sup>2</sup>C OPERATION**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	MCLR, WDT
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
0Dh	PIR2	LVDIF	—	—	—	BCLIF	—	—	CCP2IF	0--- 0--0	0--- 0--0
8Dh	PIE2	LVDIE	—	—	—	BCLIE	—	—	CCP2IE	0--- 0--0	0--- 0--0
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	0000 0000
93h	SSPADD	Synchronous Serial Port (I <sup>2</sup> C Mode) Address Register								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the MSSP in I<sup>2</sup>C mode.

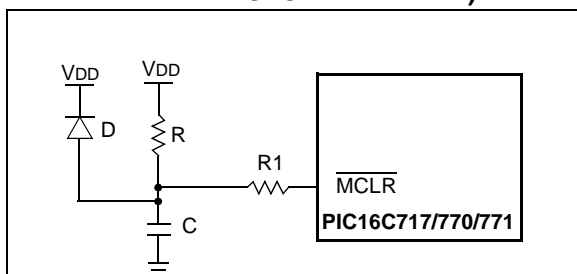
## 12.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when a VDD rise is detected (in the range of 1.5V - 2.1V). Enable the internal MCLR feature to eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details. For a long rise time, enable external MCLR function and use circuit as shown in Figure 12-5.

Two delay timers, (PWRT on OST), have been provided which hold the device in RESET after a POR (dependent upon device configuration) so that all operational parameters have been met prior to releasing the device to resume/begin normal operation.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions, or if necessary an external POR circuit may be implemented to delay end of RESET for as long as needed.

**FIGURE 12-5: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD RAMP)**



- Note 1:** External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- 2:**  $R < 40\text{ k}\Omega$  is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
  - 3:**  $R1 = 100\Omega$  to  $1\text{ k}\Omega$  will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).
  - 4:** External MCLR must be enabled (MCLRE = 1).

## 12.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed TPWRT time-out on power-up type RESETS only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the RESET condition (VDD rises above BOR trip point). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

## 12.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on a power-up type RESET or a wake-up from SLEEP.

## 12.7 Programmable Brown-Out Reset (PBOR)

The Programmable Brown-out Reset module is used to generate a RESET when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV<1:0> configuration word bits.

Configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below the specified trip point for longer than TBOR, (parameter #35), the brown-out situation will RESET the chip. A RESET may not occur if VDD falls below the trip point for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer will be invoked at that point and will keep the chip in RESET an additional TPWRT. If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will again begin a TPWRT time delay. Even though the PWRT is always enabled when brown-out is enabled, the PWRT configuration word bit should be cleared (enabled) when brown-out is enabled.

# PIC16C717/770/771

TABLE 12-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Power-on Reset or Brown-out Reset	MCLR Reset or WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	0000 0000	uuuu uuuu	uuuu uuuu
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000h	0000h	PC + 1 <sup>(1)</sup>
STATUS	0001 1xxx	000q quuu <sup>(2)</sup>	uuuq quuu <sup>(2)</sup>
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	xxxx 0000	uuuu 0000	uuuu uuuu
PORTB	xxxx xx11	uuuu uu11	uuuu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuqq
PIR1	-0-- 0000	-0-- 0000	-0-- uuuu
PIR2	0--- 0---	0--- 0---	q--- q---
TMR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	--00 0000	--uu uuuu	--uu uuuu
TMR2	0000 0000	0000 0000	uuuu uuuu
T2CON	-000 0000	-000 0000	-uuu uuuu
SSPBUF	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	0000 0000	0000 0000	uuuu uuuu
CCPR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	0000 0000	0000 0000	uuuu uuuu
ADRESH	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	1111 1111	1111 1111	uuuu uuuu
TRISA	1111 1111	1111 1111	uuuu uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	-0-- 0000	-0-- 0000	-u-- uuuu
PIE2	0--- 0---	0--- 0---	u--- u---
PCON	---- 1-qq	---- 1-uu	---- u-uu
PR2	1111 1111	1111 1111	1111 1111
SSPADD	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	0000 0000	0000 0000	uuuu uuuu
WPUB	1111 1111	1111 1111	uuuu uuuu
IOCB	1111 0000	1111 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

**Note 1:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**2:** See Table 12-5 for RESET value for specific condition.

**TABLE 12-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)**

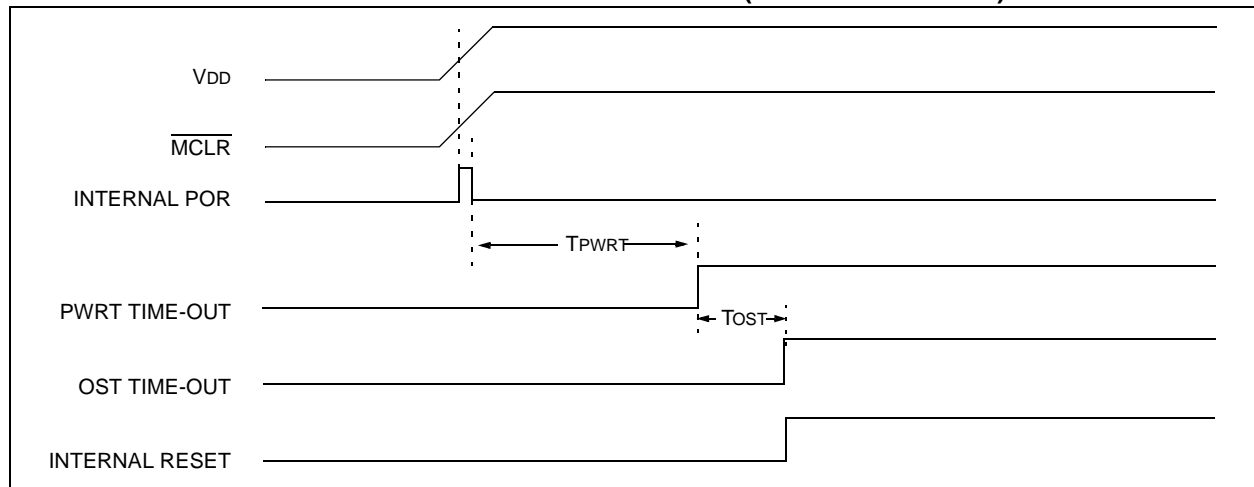
Register	Power-on Reset or Brown-out Reset	MCLR Reset or WDT Reset	Wake-up via WDT or Interrupt
P1DEL	0000 0000	0000 0000	uuuu uuuu
REFCON	0000 ----	0000 ----	uuuu ----
LVDCON	--00 0101	--00 0101	--uu uuuu
ANSEL	--11 1111	--11 1111	--uu uuuu
ADRESL	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	0000 0000	0000 0000	uuuu uuuu
PMDATL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMADRL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMDATH	--xx xxxx	--uu uuuu	--uu uuuu
PMADRH	---- xxxx	---- uuuu	---- uuuu
PMCON1	1--- ---0	1--- ---0	1--- ---0

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

**Note 1:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**2:** See Table 12-5 for RESET value for specific condition.

**FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO V<sub>DD</sub>)**



## 12.12 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator, which does not require any external components. This oscillator is independent from the processor clock. If enabled, the WDT will run even if the main clock of the device has been stopped, for example, by execution of a *SLEEP* instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in *SLEEP* mode, a WDT time-out causes the device to

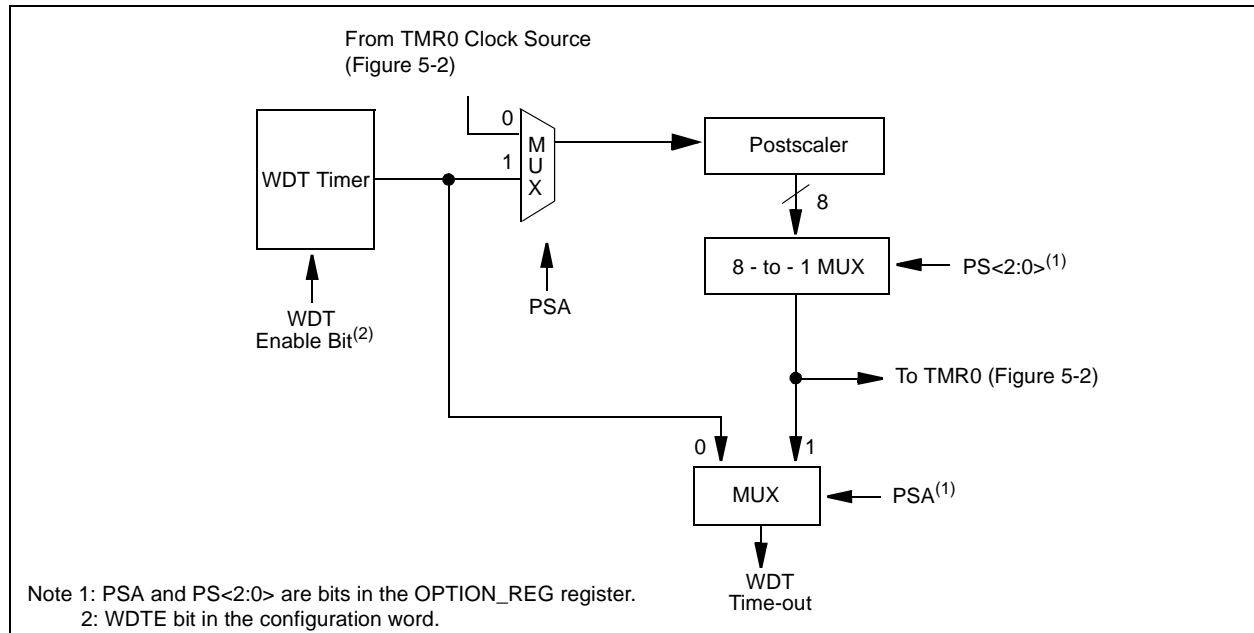
wake-up and continue with normal operation (Watchdog Timer Wake-up). The  $\overline{TO}$  bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

The WDT can be permanently disabled by programming the configuration bit WDTE to '0' (Section 12.1).

WDT time-out period values may be found in Table 15-4. Values for the WDT prescaler may be assigned using the OPTION\_REG register.

**Note:** The *SLEEP* instruction clears the WDT and the postscaler, if assigned to the WDT, restarting the WDT period.

**FIGURE 12-11: WATCHDOG TIMER BLOCK DIAGRAM**



**TABLE 12-7: SUMMARY OF WATCHDOG TIMER REGISTERS**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits <sup>(1)</sup>	—	BODEN	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0
81h,181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

**Note 1:** See Register 12-1 for the full description of the configuration word bits.

# PIC16C717/770/771

## 15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended)

PIC16LC717/770/771			<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
PIC16C717/770/771			<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.5	—	5.5	V	
D001	VDD	Supply Voltage	4.0	—	5.5	V	
D002*	VDR	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5	—	V	
D002*	VDR	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5	—	V	
D003*	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D003*	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004*	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D004*	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

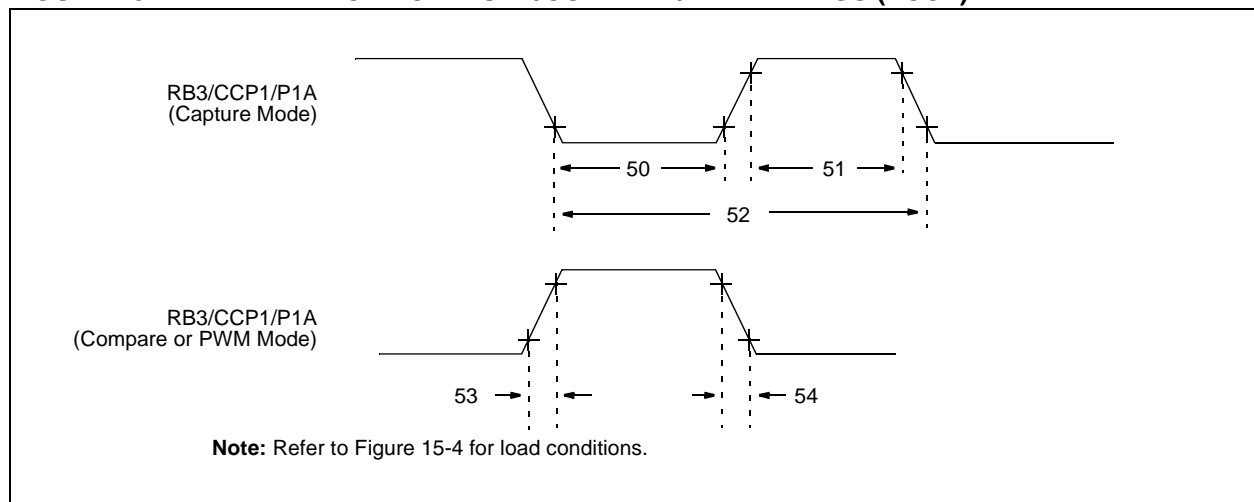
**TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS**

Param. No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
	With Prescaler			10	—	—	ns		
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
	With Prescaler			10	—	—	ns		
42*	Tt0P	T0CKI Period		No Prescaler	TCY + 40	—	—	ns	N = prescale value (2, 4, ..., 256)
	With Prescaler			Greater of: 20 or $\frac{TCY + 40}{N}$	—	—	ns		
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16C717/770/771	15	—	—	ns	
				PIC16LC717/770/771	25	—	—	ns	
			Asynchronous	PIC16C717/770/771	30	—	—	ns	
				PIC16LC717/770/771	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16C717/770/771	15	—	—	ns	
				PIC16LC717/770/771	25	—	—	ns	
			Asynchronous	PIC16C717/770/771	30	—	—	ns	
				PIC16LC717/770/771	50	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous	PIC16C717/770/771	Greater of: 30 OR $\frac{TCY + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
				PIC16LC717/770/771	Greater of: 50 OR $\frac{TCY + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16C717/770/771	60	—	—	ns	
				PIC16LC717/770/771	100	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	50	kHz	
48	Tcke2tmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 15-11: ENHANCED CAPTURE/COMPARE/PWM TIMINGS (ECCP)**



# PIC16C717/770/771

FIGURE 16-28:  $V_{OL}$  VS.  $I_{OL}$  (-40°C TO +125°C,  $V_{DD} = 5.0V$ )

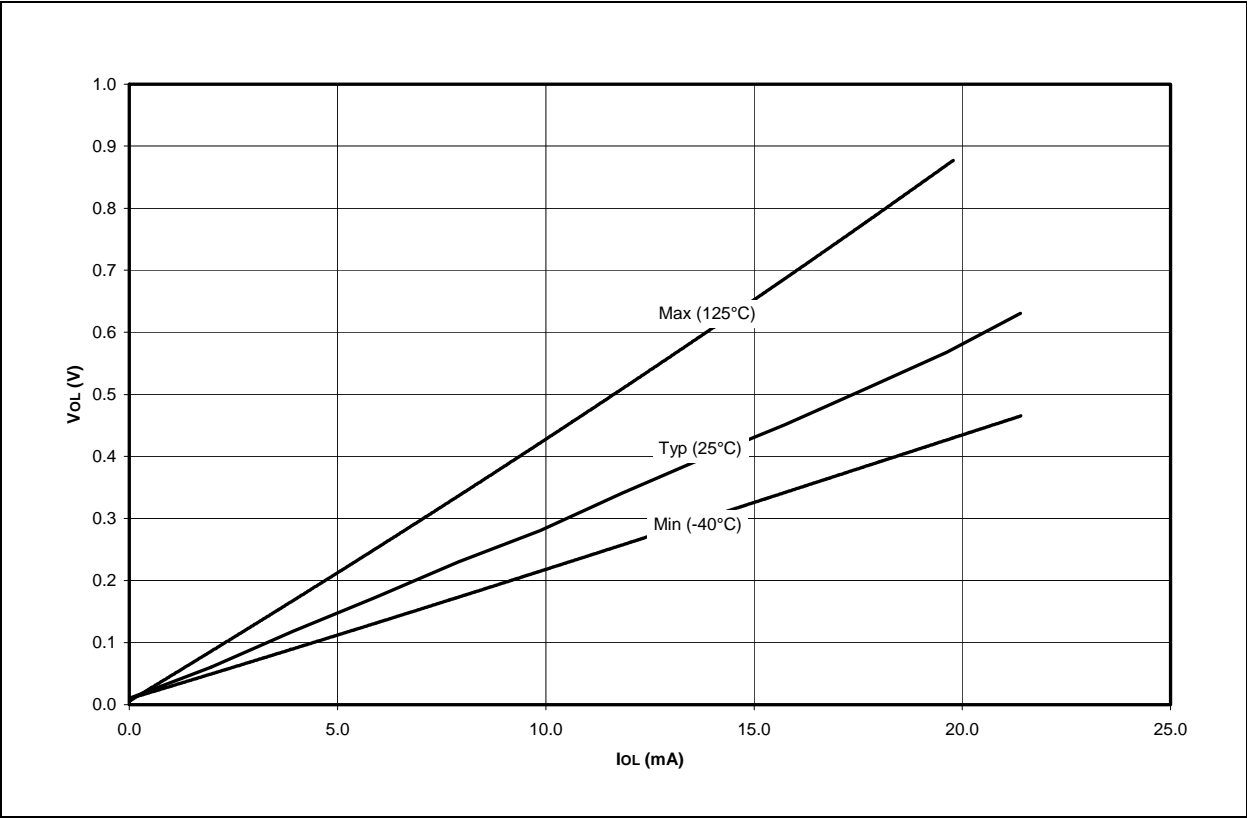
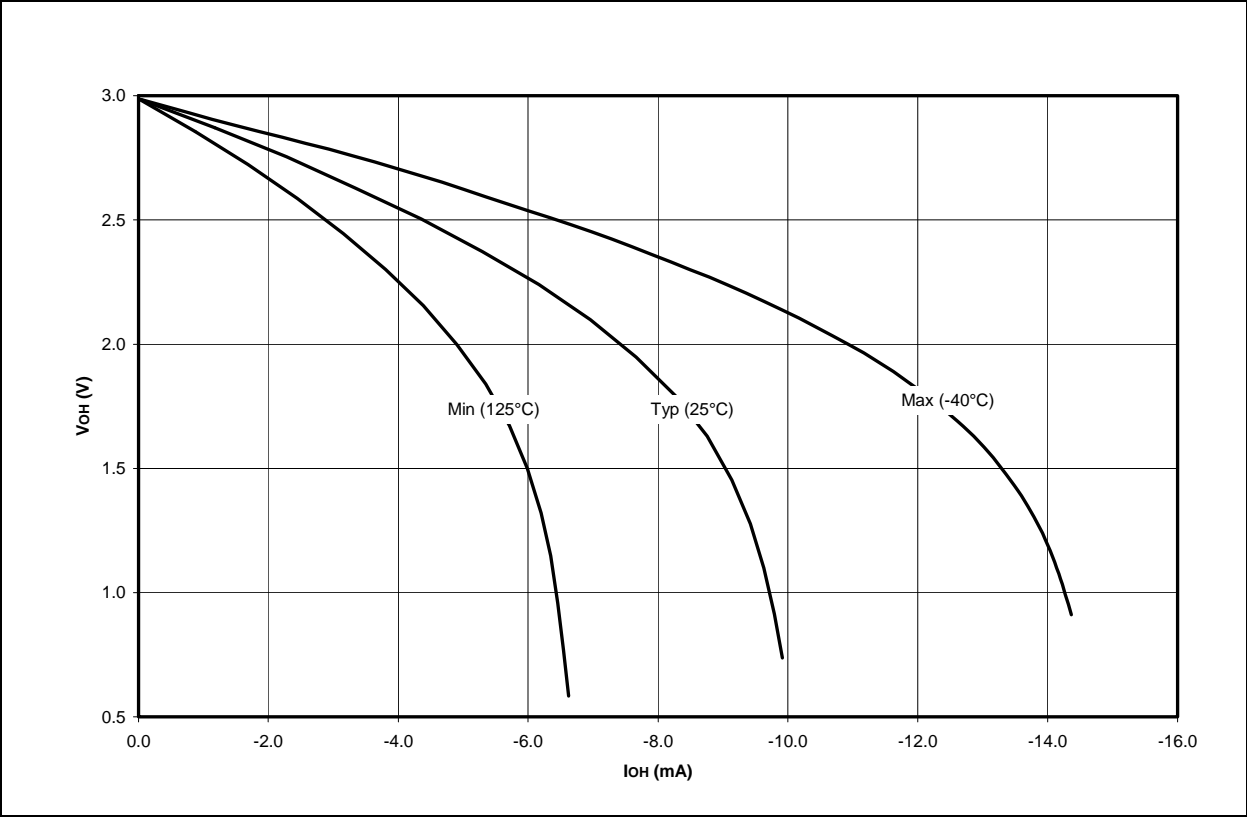
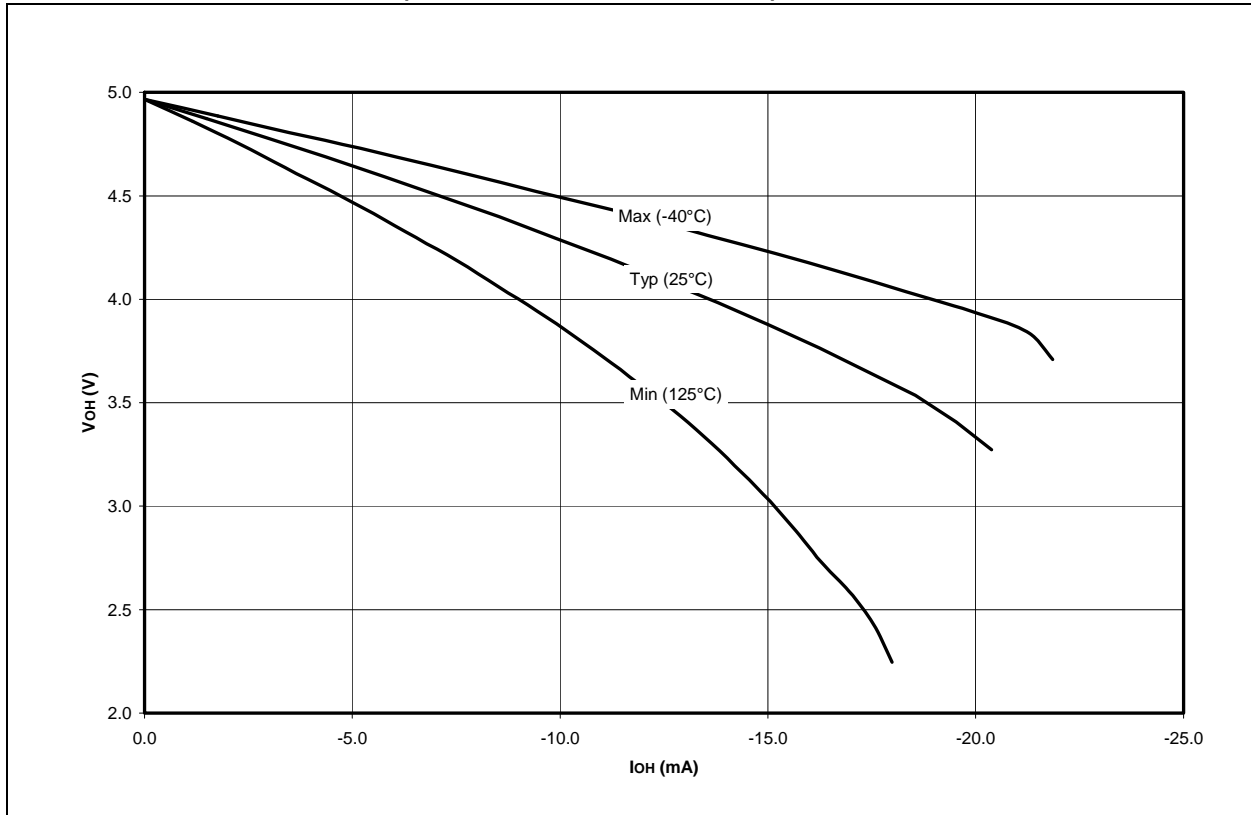


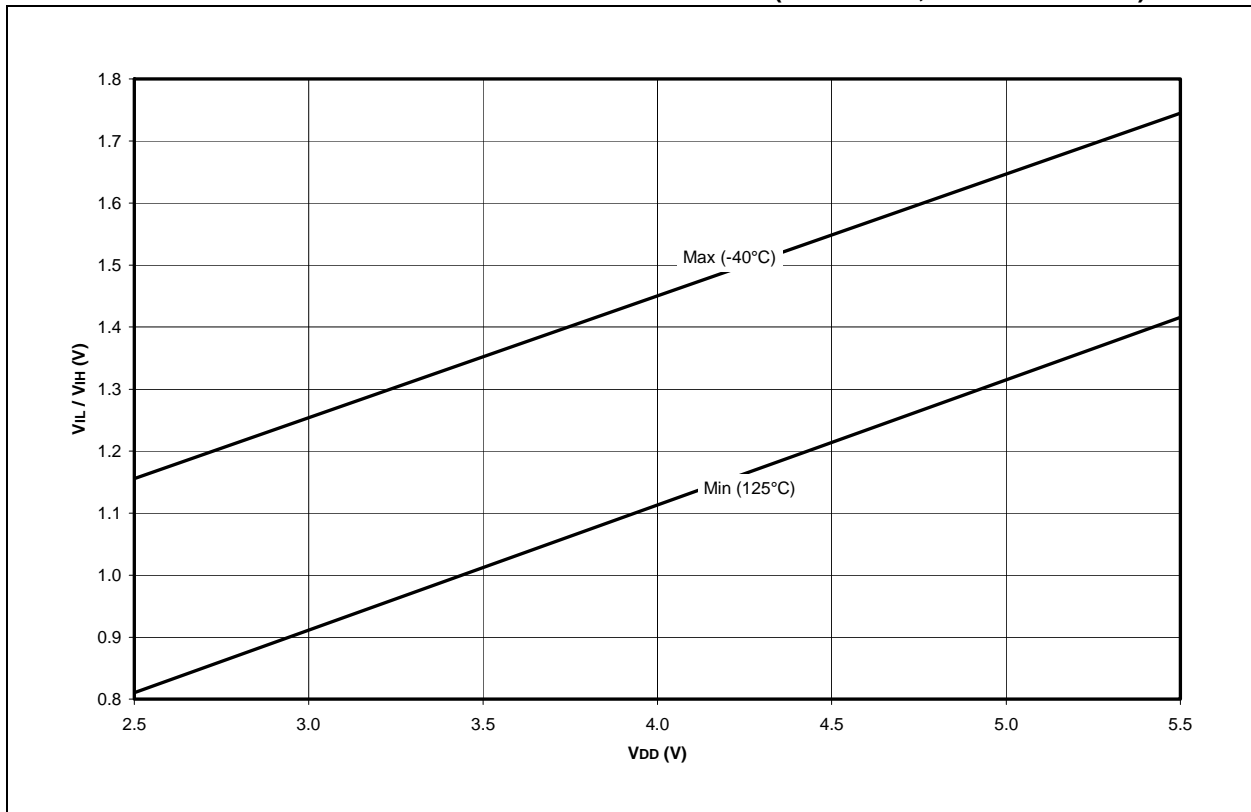
FIGURE 16-29:  $V_{OH}$  VS.  $I_{OH}$  (-40°C TO +125°C,  $V_{DD} = 3.0V$ )



**FIGURE 16-30:  $V_{OH}$  VS.  $I_{OH}$  ( $-40^{\circ}\text{C}$  TO  $+125^{\circ}\text{C}$ ,  $V_{DD} = 5.0\text{V}$ )**

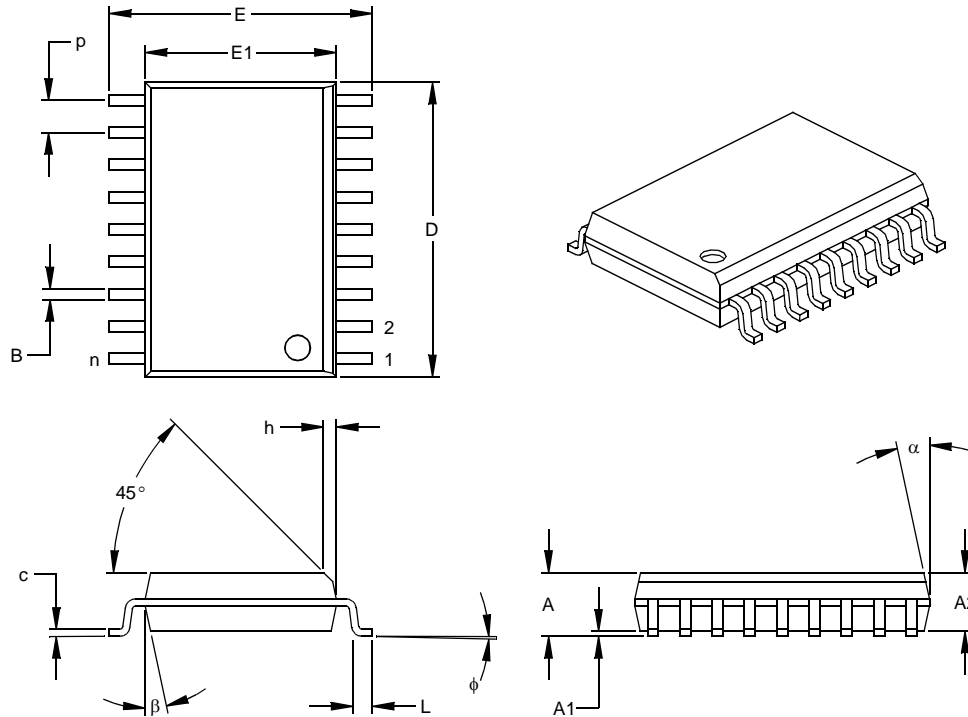


**FIGURE 16-31: MINIMUM AND MAXIMUM  $V_{IH}/V_{IL}$  VS.  $V_{DD}$  (TTL INPUT,  $-40^{\circ}\text{C}$  TO  $+125^{\circ}\text{C}$ )**



## 17.4 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-051