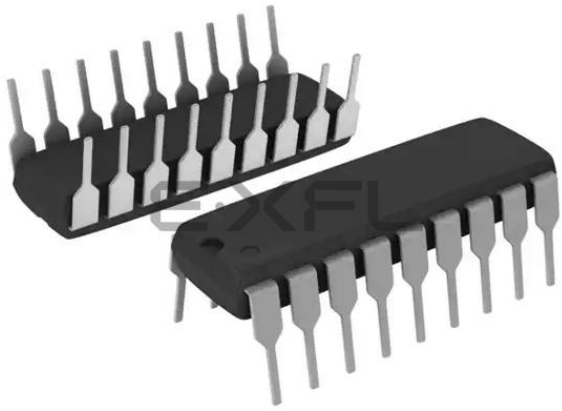

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc717-i-p

2.0 MEMORY ORGANIZATION

There are two memory blocks in each of these PIC® microcontrollers. Each block (Program Memory and Data Memory) has its own bus, so that concurrent access can occur.

Additional information on device memory may be found in the PICmicro™ Mid-Range MCU Family Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16C717/770/771 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16C717 and the PIC16C770 have 2K x 14 words of program memory. The PIC16C771 has 4K x 14 words of program memory. Accessing a location above the physically implemented address will cause a wrap-around.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK OF THE PIC16C717 AND PIC16C770

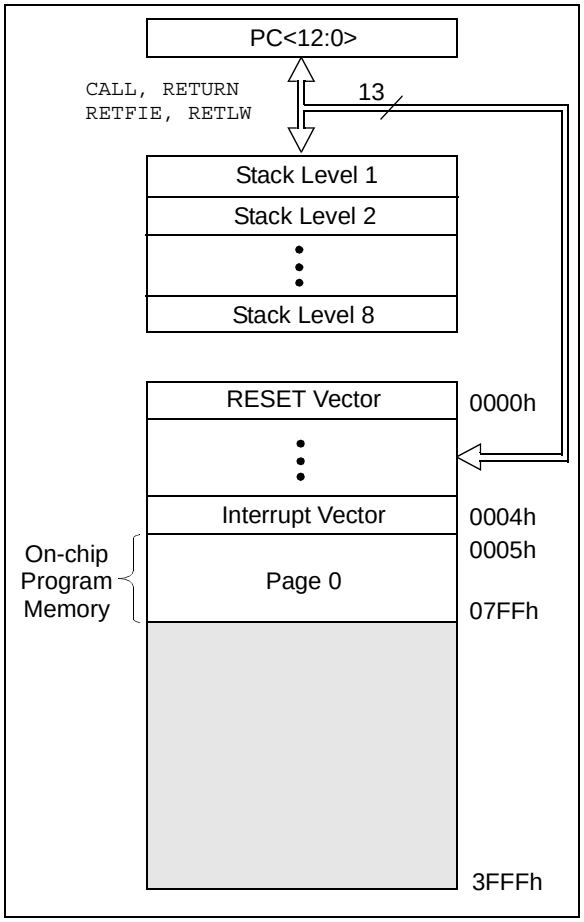
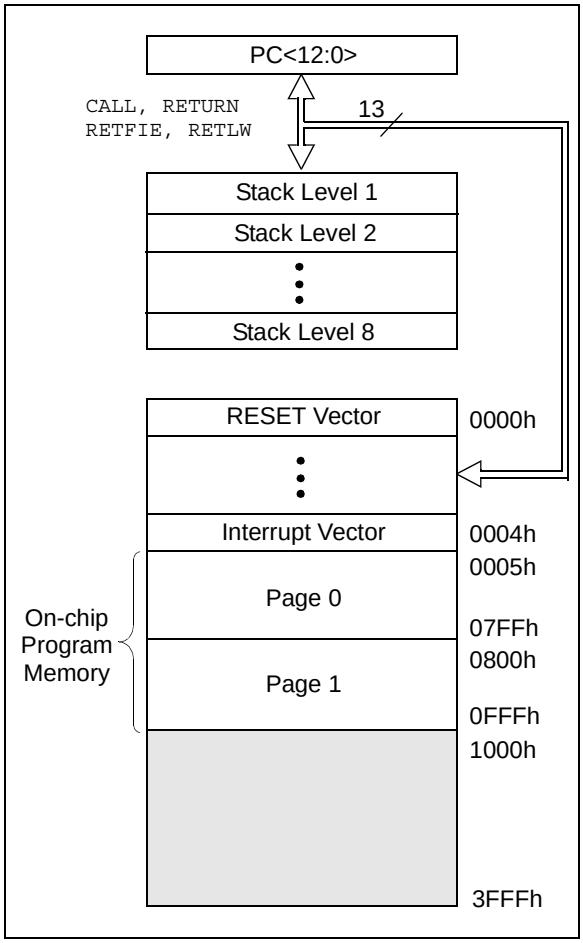


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK OF THE PIC16C771



2.2 Data Memory Organization

The data memory is partitioned into multiple banks, which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1	RP0	(STATUS<6:5>)

= 00 → Bank0
= 01 → Bank1
= 10 → Bank2
= 11 → Bank3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some frequently used special function registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly, through the File Select Register FSR.

3.3 PORTB and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

EXAMPLE 3-2: Initializing PORTB

```
BCF     STATUS, RP0 ;
CLRF    PORTB       ; Initialize PORTB by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                    ; RB<5:4> as outputs
                    ; RB<7:6> as inputs
MOVLW   0x30        ; Set RB<1:0> as analog
                      inputs
MOVWF   ANSEL       ;
BCF     STATUS, RP0 ; Return to Bank 0
```

Each of the PORTB pins has an internal pull-up, which can be individually enabled from the WPUB register. A single global enable bit can turn on/off the enabled pull-ups. Clearing the $\overline{\text{RBPU}}$ bit, (OPTION_REG<7>), enables the weak pull-up resistors. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Each of the PORTB pins, if configured as input, also has an interrupt-on-change feature, which can be individually selected from the IOCB register. The RBIE bit in the INTCON register functions as a global enable bit to turn on/off the interrupt-on-change feature. The selected inputs are compared to the old value latched on the last read of PORTB. The "mismatch" outputs are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

a) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

4.3 READING THE EPROM PROGRAM MEMORY

To read a program memory location, the user must write 2 bytes of the address to the PMADRH and PMADRL registers, then set control bit RD (PMCON1<0>). Once the read control bit is set, the Program Memory Read (PMR) controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following the "BSF PMCON1,RD" instruction to be ignored. The data is available, in the very next cycle, in the PMDATH and PMDATL registers; therefore it can be read as 2 bytes in the following instructions. PMDATH and PMDATL registers will hold this value until another Program Memory Read or until it is written to by the user.

Note: The two instructions that follow setting the PMCON1 read bit must be NOPs.

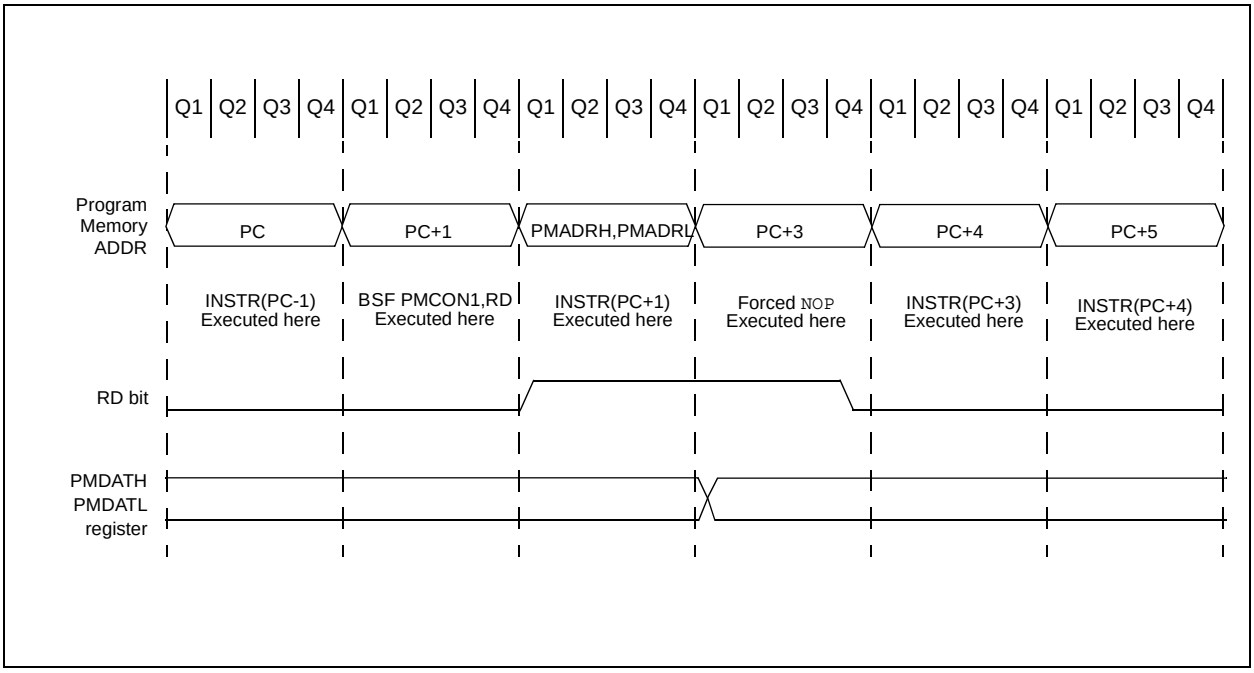
EXAMPLE 4-1: OTP PROGRAM MEMORY Read

```
    BSF     STATUS, RP1      ;
    BCF     STATUS, RP0      ; Bank 2
    MOVLW   MS_PROG_PM_ADDR  ;
    MOVWF   PMADRH           ; MS Byte of Program Memory Address to read
    MOVLW   LS_PROG_PM_ADDR  ;
    MOVWF   PMADRL           ; LS Byte of Program Memory Address to read
    BSF     STATUS, RP0      ; Bank 3
    BSF     PMCON1, RD       ; Program Memory Read
    NOP                      ; This instruction must be an NOP
    NOP                      ; This instruction must be an NOP
    next instruction         ; PMDATH:PMDATL now has the data
```

4.4 OPERATION DURING CODE PROTECT

When the device is code protected, the CPU can still perform the Program Memory Read function.

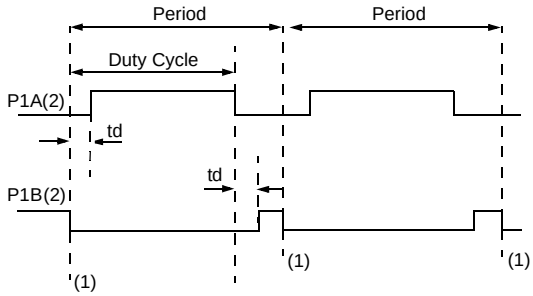
FIGURE 4-1: PROGRAM MEMORY READ CYCLE EXECUTION



8.3.4 OUTPUT POLARITY CONFIGURATION

The CCP1M<1:0> bits in the CCP1CON register allow user to choose the logic conventions (asserted high/ low) for each of the outputs. See Register 8-1 for further details.

FIGURE 8-6: HALF-BRIDGE PWM OUTPUT



td = Deadband Delay

Note 1: At this time, the TMR2 register is equal to the PR2 register.
2: Output signals are shown as asserted high.

The PWM output polarities must be selected before the PWM outputs are enabled. Charging the polarity configuration while the PWM outputs are active is not recommended, since it may result in unpredictable operation.

REGISTER 9-3: SYNC SERIAL PORT CONTROL REGISTER2 (SSPCON2: 91h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

bit 7 **GCEN:** General Call Enable bit (In I^2C Slave mode only)
1 = Enable interrupt when a general call address (0000h) is received in the SSPSR.
0 = General call address disabled.

bit 6 **ACKSTAT:** Acknowledge Status bit (In I^2C Master mode only)
In Master Transmit mode:
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 5 **ACKDT:** Acknowledge Data bit (In I^2C Master mode only)
In Master Receive mode:
Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
1 = Not Acknowledge (NACK)
0 = Acknowledge (ACK)

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (In I^2C Master mode only).
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence IDLE

bit 3 **RCEN:** Receive Enable bit (In I^2C Master mode only).
1 = Enables Receive mode for I^2C
0 = Receive IDLE

bit 2 **PEN:** STOP Condition Enable bit (In I^2C Master mode only).
SCK Release Control
1 = Initiate STOP condition on SDA and SCL pins. Automatically cleared by hardware.
0 = STOP condition IDLE

bit 1 **RSEN:** Repeated START Condition Enabled bit (In I^2C Master mode only)
1 = Initiate Repeated START condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated START condition IDLE

bit 0 **SEN:** START Condition Enabled bit (In I^2C Master mode only)
1 = Initiate START condition on SDA and SCL pins. Automatically cleared by hardware.
0 = START condition IDLE

Note: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the IDLE mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 11-2: A/D CONTROL REGISTER 1 (ADCON1: 9Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG2	VCFG1	VCFG0	Reserved	Reserved	Reserved	Reserved
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6-4 **VCFG<2:0>:** Voltage Reference Configuration bits

	A/D V_{REF+}	A/D V_{REF-}
000	AV_{DD}(1)	AV_{SS}(2)
001	External V_{REF+}	External V_{REF-}
010	Internal VRH	Internal VRL
011	External V_{REF+}	AV_{SS}(2)
100	Internal VRH	AV_{SS}(2)
101	AV_{DD}(1)	External V_{REF-}
110	AV_{DD}(1)	Internal VRL
111	Internal VRL	AV_{SS}

bit 3-0 **Reserved:** Do not use.

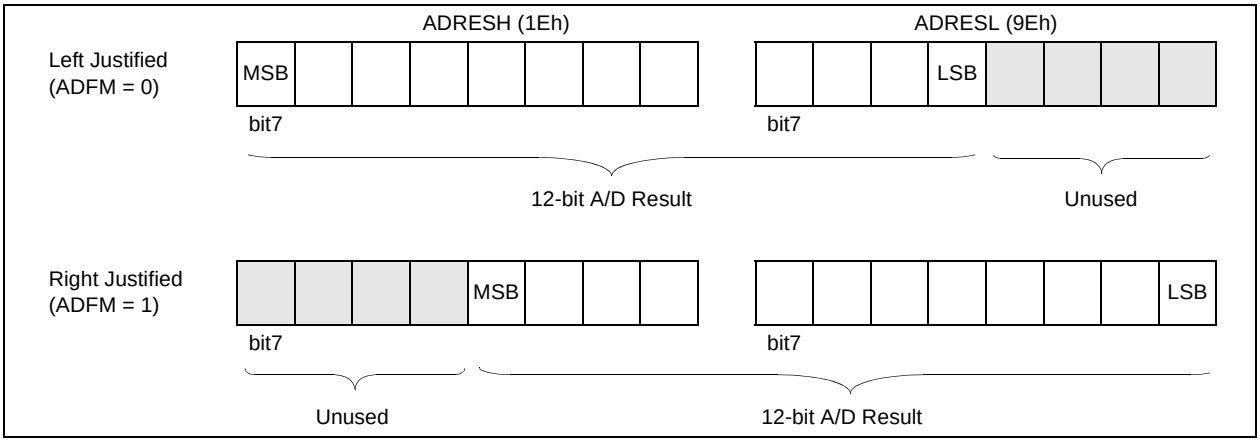
Note 1: This parameter is V_{DD} for the PIC16C717.
2: This parameter is V_{SS} for the PIC16C717.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The value that is in the ADRESH and ADRESL registers are not modified for a Power-on Reset. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

The A/D conversion results can be left justified (ADFM bit cleared), or right justified (ADFM bit set). Figure 11-1 through Figure 11-2 show the A/D result data format of the PIC16C717/770/771.

FIGURE 11-1: PIC16C770/771 12-BIT A/D RESULT FORMATS



11.3 Selecting the A/D Conversion Clock

The A/D conversion cycle requires 13TAD: 1 TAD for settling time, and 12 TAD for conversion. The source of the A/D conversion clock is software selected. If neither the internal VRH nor VRL are used for the A/D converter, the four possible options for TAD are:

- 2 TOSC
- 8 TOSC
- 32 TOSC
- A/D RC oscillator

If the VRH or VRL are used for the A/D converter reference, then the TAD requirement is automatically increased by a factor of 8.

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μs. Table 11-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

The ADIF bit is set on the rising edge of the 14th TAD. The GO/DONE bit is cleared on the falling edge of the 14th TAD.

TABLE 11-1: TAD VS. DEVICE OPERATING FREQUENCIES

A/D Reference Source	A/D Clock Source (TAD)		Device Frequency			
	Operation	**ADCS<1:0>**	**20 MHz**	**5 MHz**	**4 MHz**	**1.25 MHz**
External VREF or Analog Supply	2 TOSC	00	100 ns(2)	400 ns(2)	500 ns(2)	1.6 μs
	8 TOSC	01	400 ns(2)	1.6 μs	2.0 μs	6.4 μs
	32 TOSC	10	1.6 μs	6.4 μs(3)	8.0 μs(3)	25.6 μs(3)
	A/D RC	11	2 - 6 μs(1,4)	2 - 6 μs(1,4)	2 - 6 μs(1,4)	2 - 6 μs(1,4)
Internal VRH or VRL	16 TOSC	00	800 ns(2)	3.2 μs(2)	4 μs(2)	12.8 μs
	64 TOSC	01	3.2 μs(2)	12.8 μs	16 μs	51.2 μs(3)
	256 TOSC	10	12.8 μs	51.2 μs(3)	64 μs(3)	204.8 μs(3)
	A/D RC	11	16 - 48 μs(4,5)	16 - 48 μs(4,5)	16 - 48 μs(4,5)	16 - 48 μs(4,5)

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical TAD time of 4 μs for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during SLEEP.

5: A/D RC clock source has a typical TAD time of 32 μs for VDD > 3.0V.

11.5 A/D Converter Module Operation

Figure 11-4 shows the flowchart of the A/D converter module.

FIGURE 11-4: FLOW CHART OF A/D OPERATION

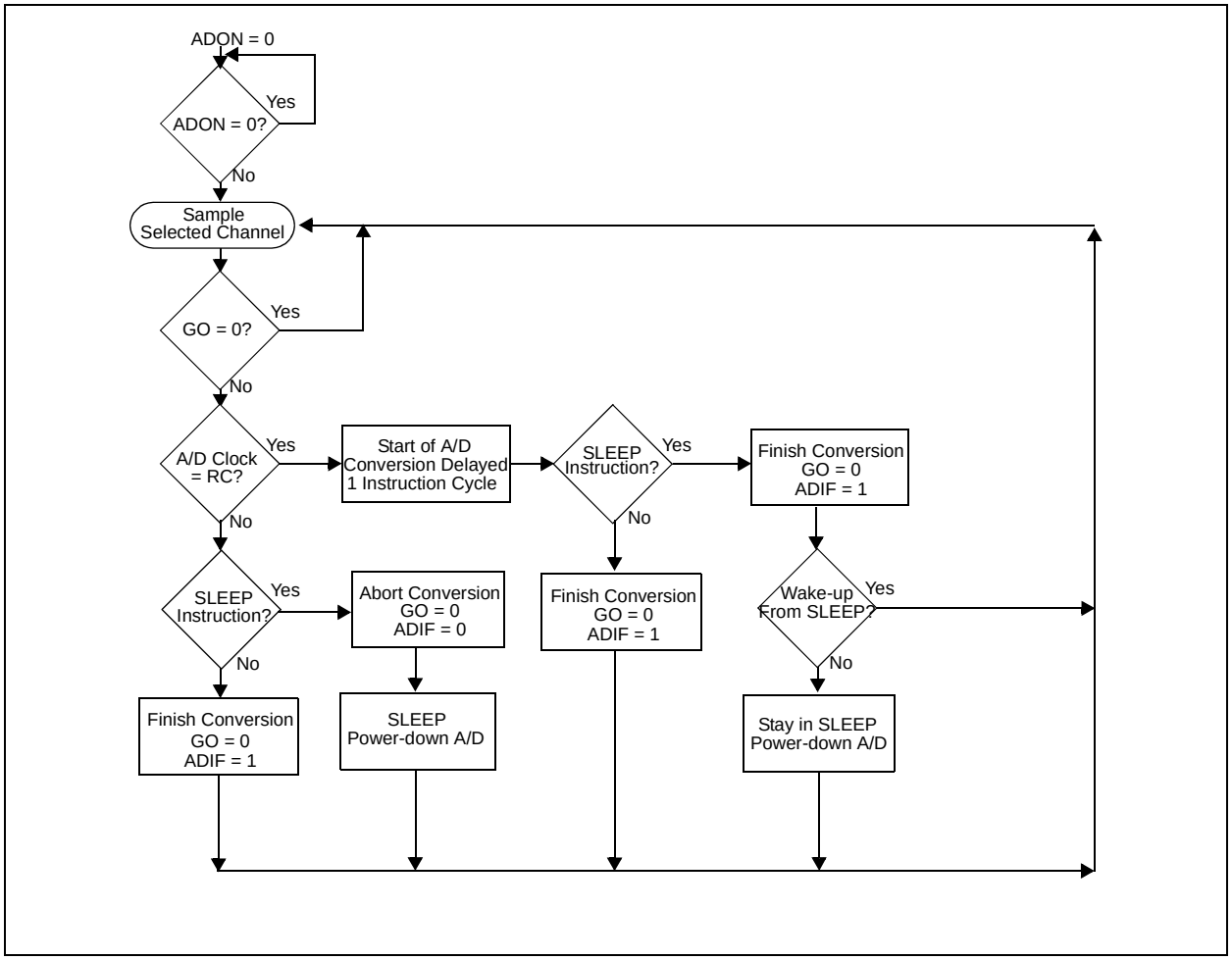


TABLE 13-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb	LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	**f, d**	Add W and f	1	00 0111 dfff ffff		C,DC,Z	1,2
ANDWF	**f, d**	AND W with f	1	00 0101 dfff ffff		Z	1,2
CLRF	**f**	Clear f	1	00 0001 lfff ffff		Z	2
CLRW	**-**	Clear W	1	00 0001 0000 0011		Z	
COMF	**f, d**	Complement f	1	00 1001 dfff ffff		Z	1,2
DECF	**f, d**	Decrement f	1	00 0011 dfff ffff		Z	1,2
DECFSZ	**f, d**	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff			1,2,3
INCF	**f, d**	Increment f	1	00 1010 dfff ffff		Z	1,2
INCFSZ	**f, d**	Increment f, Skip if 0	1(2)	00 1111 dfff ffff			1,2,3
IORWF	**f, d**	Inclusive OR W with f	1	00 0100 dfff ffff		Z	1,2
MOVF	**f, d**	Move f	1	00 1000 dfff ffff		Z	1,2
MOVWF	**f**	Move W to f	1	00 0000 lfff ffff			
NOP	**-**	No Operation	1	00 0000 0xx0 0000			
RLF	**f, d**	Rotate Left f through Carry	1	00 1101 dfff ffff		C	1,2
RRF	**f, d**	Rotate Right f through Carry	1	00 1100 dfff ffff		C	1,2
SUBWF	**f, d**	Subtract W from f	1	00 0010 dfff ffff		C,DC,Z	1,2
SWAPF	**f, d**	Swap nybbles in f	1	00 1110 dfff ffff			1,2
XORWF	**f, d**	Exclusive OR W with f	1	00 0110 dfff ffff		Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	**f, b**	Bit Clear f	1	01 00bb bfff ffff			1,2
BSF	**f, b**	Bit Set f	1	01 01bb bfff ffff			1,2
BTFSC	**f, b**	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff			3
BTFSS	**f, b**	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff			3
LITERAL AND CONTROL OPERATIONS							
ADDLW	**k**	Add literal and W	1	11 111x kkkk kkkk		C,DC,Z	
ANDLW	**k**	AND literal with W	1	11 1001 kkkk kkkk		Z	
CALL	**k**	Call subroutine	2	10 0kkk kkkk kkkk			
CLRWDT	**-**	Clear Watchdog Timer	1	00 0000 0110 0100		$\overline{TO}$,$\overline{PD}$	
GOTO	**k**	Go to address	2	10 1kkk kkkk kkkk			
IORLW	**k**	Inclusive OR literal with W	1	11 1000 kkkk kkkk		Z	
MOVLW	**k**	Move literal to W	1	11 00xx kkkk kkkk			
RETFIE	**-**	Return from interrupt	2	00 0000 0000 1001			
RETLW	**k**	Return with literal in W	2	11 01xx kkkk kkkk			
RETURN	**-**	Return from Subroutine	2	00 0000 0000 1000			
SLEEP	**-**	Go into Standby mode	1	00 0000 0110 0011		$\overline{TO}$,$\overline{PD}$	
SUBLW	**k**	Subtract W from literal	1	11 110x kkkk kkkk		C,DC,Z	
XORLW	**k**	Exclusive OR literal with W	1	11 1010 kkkk kkkk		Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

14.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

14.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

14.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

NOTES:

FIGURE 15-6: EXTERNAL CLOCK TIMING

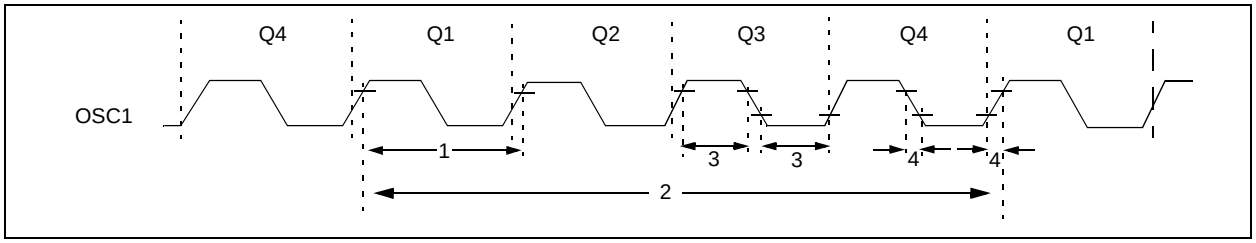


TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency **(Note 1)**	DC	—	4	MHz	XT mode
			DC	—	20	MHz	EC mode
			DC	—	20	MHz	HS mode
			DC	—	200	kHz	LP mode
		Oscillator Frequency **(Note 1)**	0.1*	—	4	MHz	XT mode
			4*	—	20	MHz	HS mode
			5*	—	200	kHz	LP mode
1	TOSC	External CLKIN Period **(Note 1)**	250	—	—	ns	XT mode
			50	—	—	ns	EC mode
			50	—	—	ns	HS mode
			5	—	—	µs	LP mode
		Oscillator Period **(Note 1)**	250	—	10,000*	ns	XT mode
			50	—	250*	ns	HS mode
			5	—	—	µs	LP mode
2	TCY	Instruction Cycle Time **(Note 1)**	200	TCY	DC	ns	TCY = 4/FOSC
3*	TosL, TosH	External Clock in (OSC1) High or Low Time	100	—	—	ns	XT mode
			2.5	—	—	µs	LP mode
			15	—	—	ns	HS mode
							EC mode
4*	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT mode
			—	—	50	ns	LP mode
			—	—	15	ns	HS mode
							EC mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Max. Frequency" values with a square wave applied to the OSC1/CLKIN pin.

When an external clock input is used, the "Min." frequency (or Max. TCY) limit is "DC" (no clock) for all devices.

TABLE 15-6: ENHANCED CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

Param. No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**717/770/771	10	—	—	ns	
				PIC16**LC**717/770/771	20	—	—	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**717/770/771	10	—	—	ns	
				PIC16**LC**717/770/771	20	—	—	ns	
52*	TccP	CCP1 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)
53*	TccR	CCP1 output fall time		PIC16**C**717/770/771	—	10	25	ns	
				PIC16**LC**717/770/771	—	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16**C**717/770/771	—	10	25	ns	
				PIC16**LC**717/770/771	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 15-12: PIC16C770/771 AND PIC16LC770/771 A/D CONVERSION REQUIREMENTS (NORMAL MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	1.6	—	—	µs	Tosc based, VREF ≥ 2.5V
			3.0	—	—	µs	Tosc based, VREF full range
							ADCS<1:0> = 11 (A/D RC mode)
			3.0	6.0	9.0	µs	At VDD = 2.5V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	13TAD	—	TAD	
132*	TACQ	Acquisition Time	**Note 2**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2	—	—	

* These parameters are characterized but not tested.

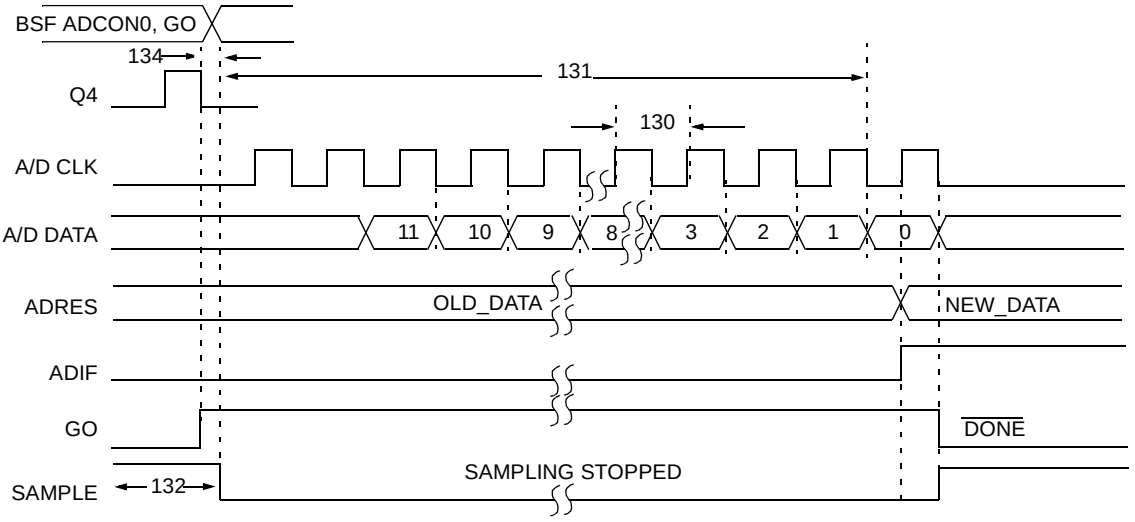
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

FIGURE 15-15: PIC16C770/771 AND PIC16LC770/771 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-13: PIC16C770/771 AND PIC16LC770/771 A/D CONVERSION REQUIREMENT (SLEEP MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D Internal RC oscillator period	3.0	6.0	9.0	µs	ADCS<1:0> = 11 (RC mode) At VDD= 3.0V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	13TAD	—	—	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2 + TCY	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

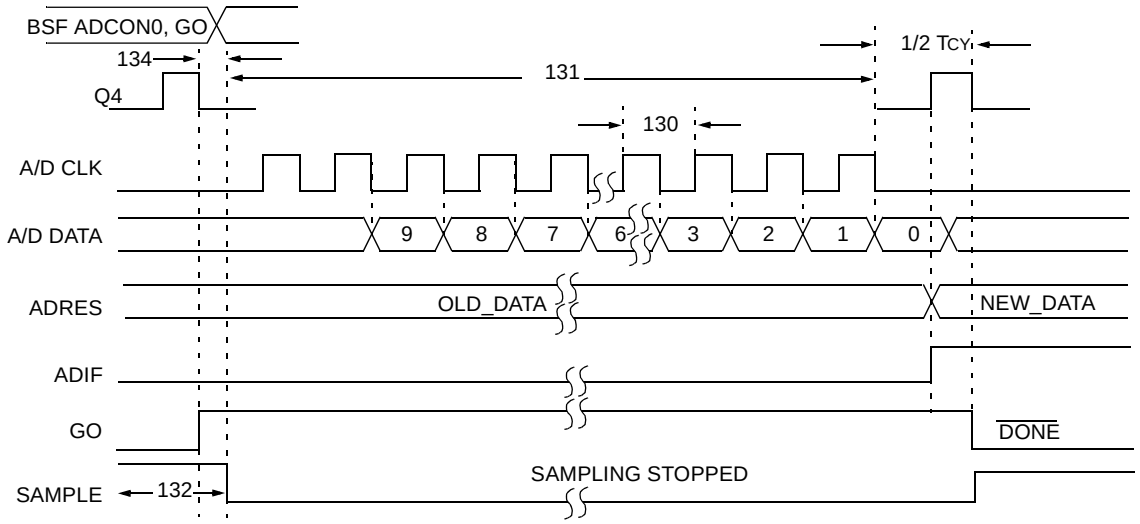
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

FIGURE 15-16: PIC16C717 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-15: PIC16C717 AND PIC16LC717 A/D CONVERSION REQUIREMENT (NORMAL MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	1.6	—	—	µs	Tosc based, VREF ≥ 2.5V
			3.0	—	—	µs	Tosc based, VREF full range
							ADCS<1:0> = 11 (A/D RC mode)
			3.0	6.0	9.0	µs	At VDD = 2.5V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	11TAD	—	TAD	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2	—	—	

* These parameters are characterized but not tested.

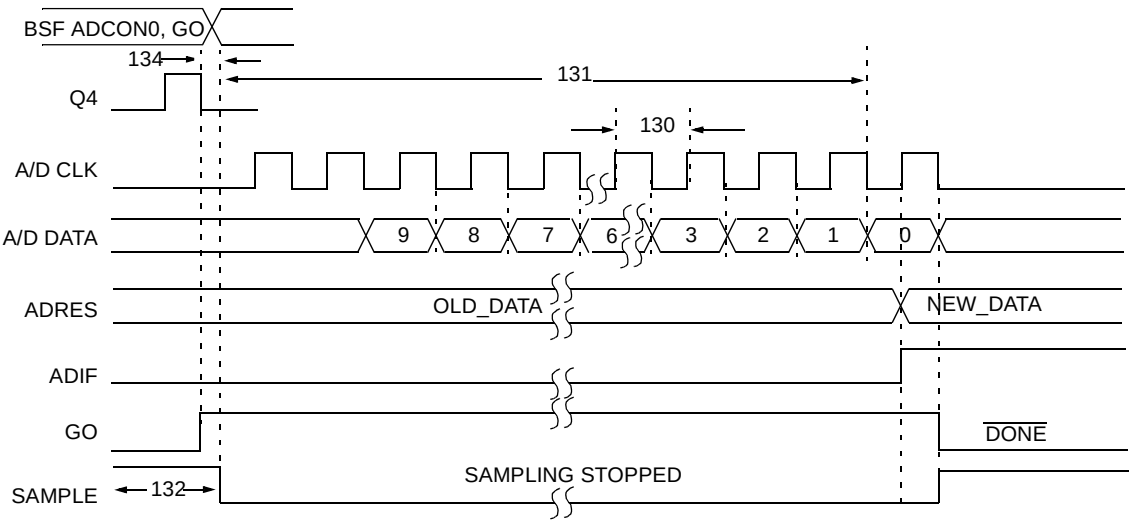
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

FIGURE 15-17: PIC16C717 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-16: PIC16C717 AND PIC16LC717 A/D CONVERSION REQUIREMENT (SLEEP MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	3.0	6.0	9.0	µs	ADCS<1:0> = 11 (A/D RC mode) At VDD = 3.0V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	11TAD	—	—	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2 + TCY	—	—	If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

FIGURE 16-10: TYPICAL IDD VS. FOSC OVER VDD (ER MODE)

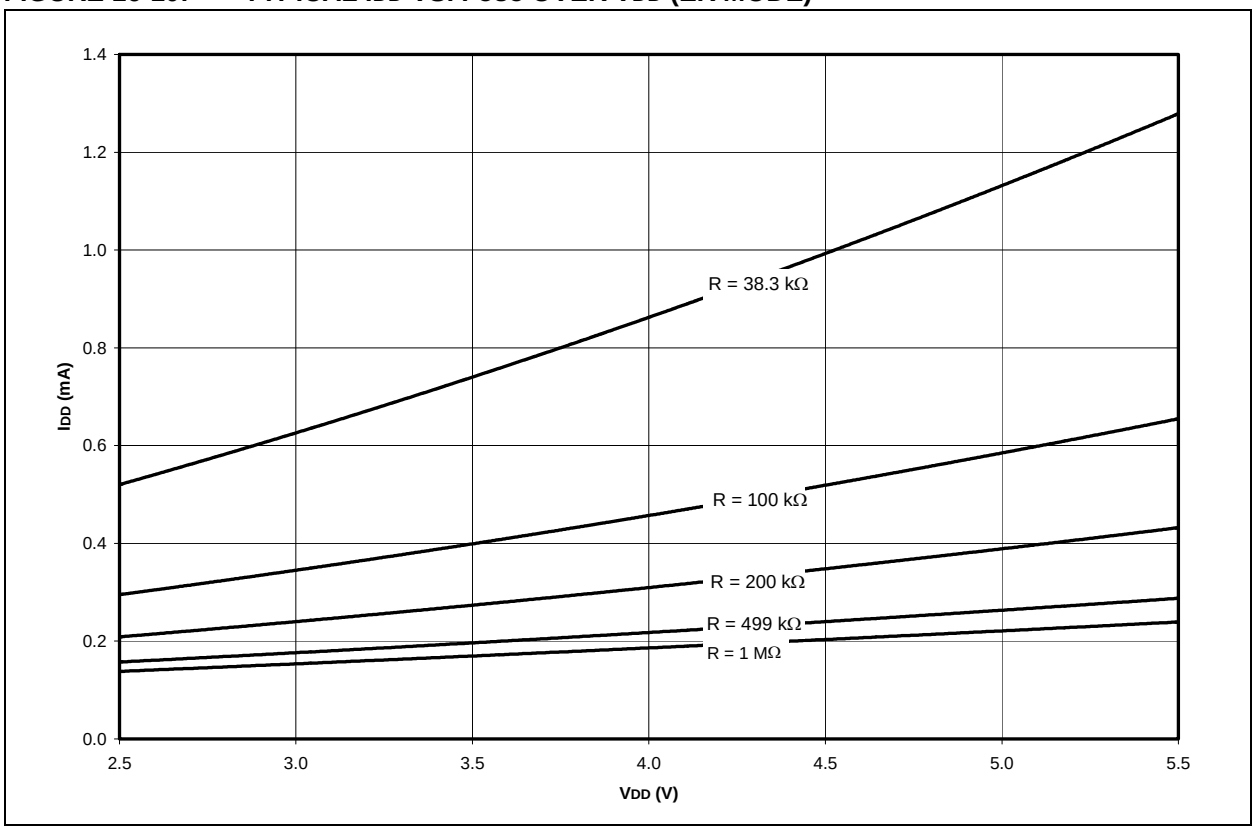


FIGURE 16-11: TYPICAL FOSC VS. VDD (ER MODE)

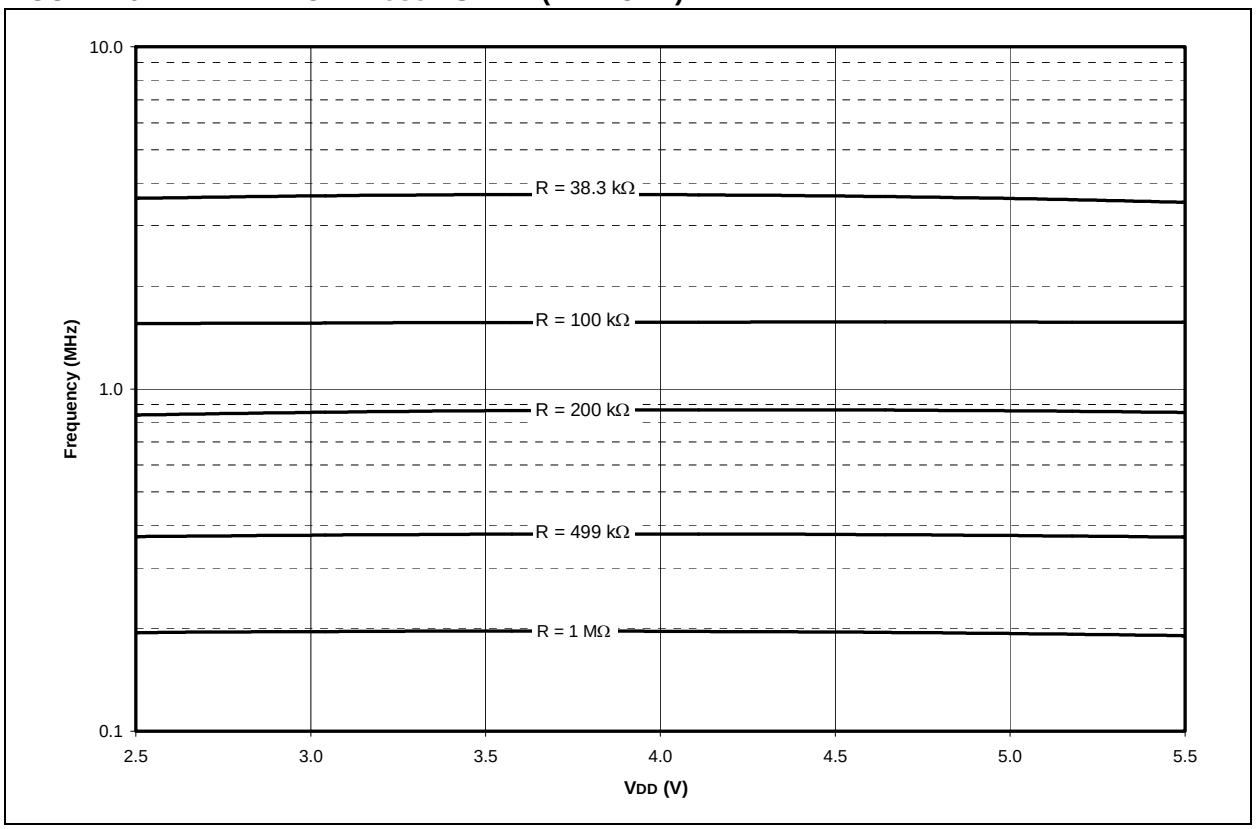
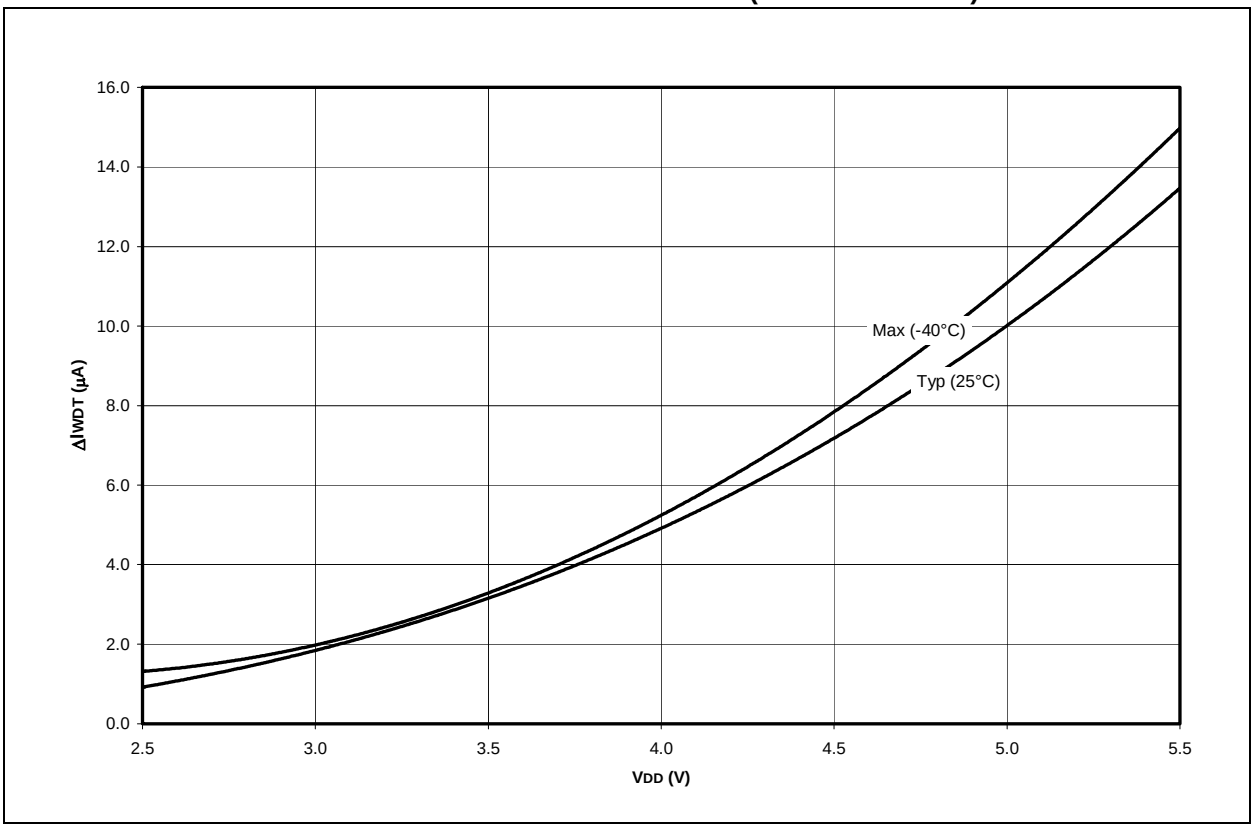
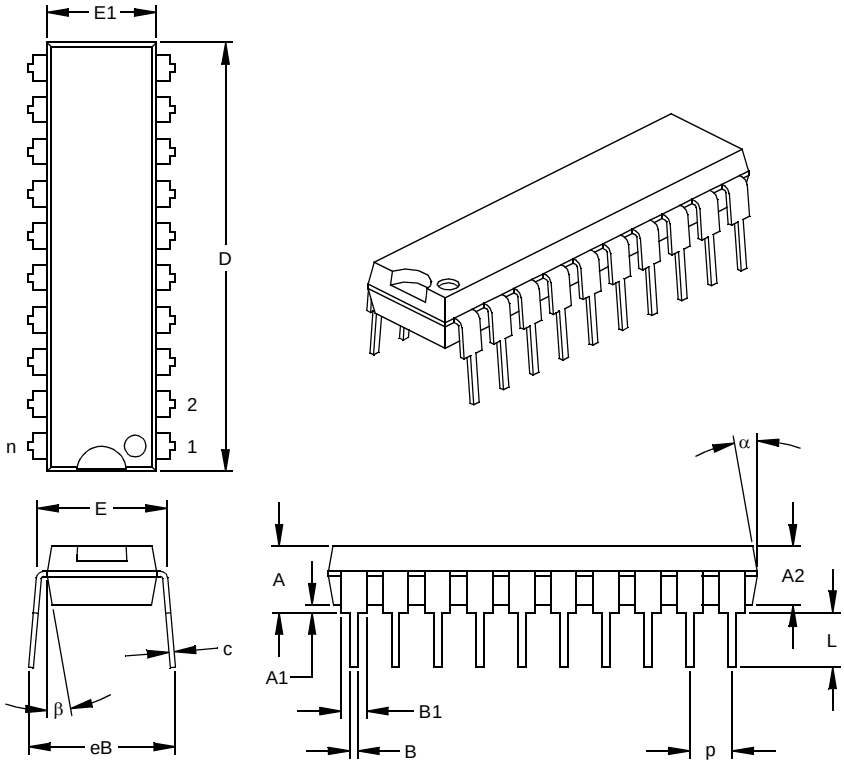


FIGURE 16-19: TYPICAL AND MAXIMUM ΔIWDT VS. VDD (-40°C TO +125°C)



17.5 20-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-019