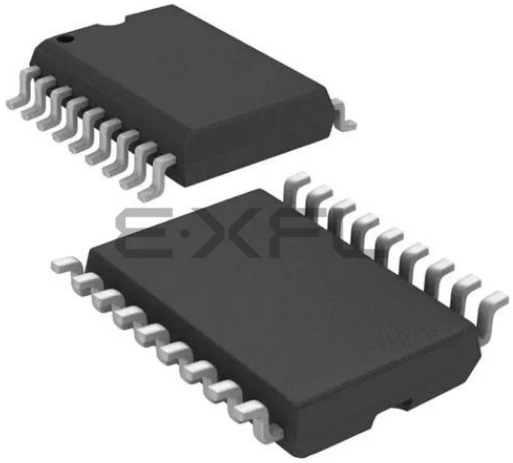

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc717-i-so

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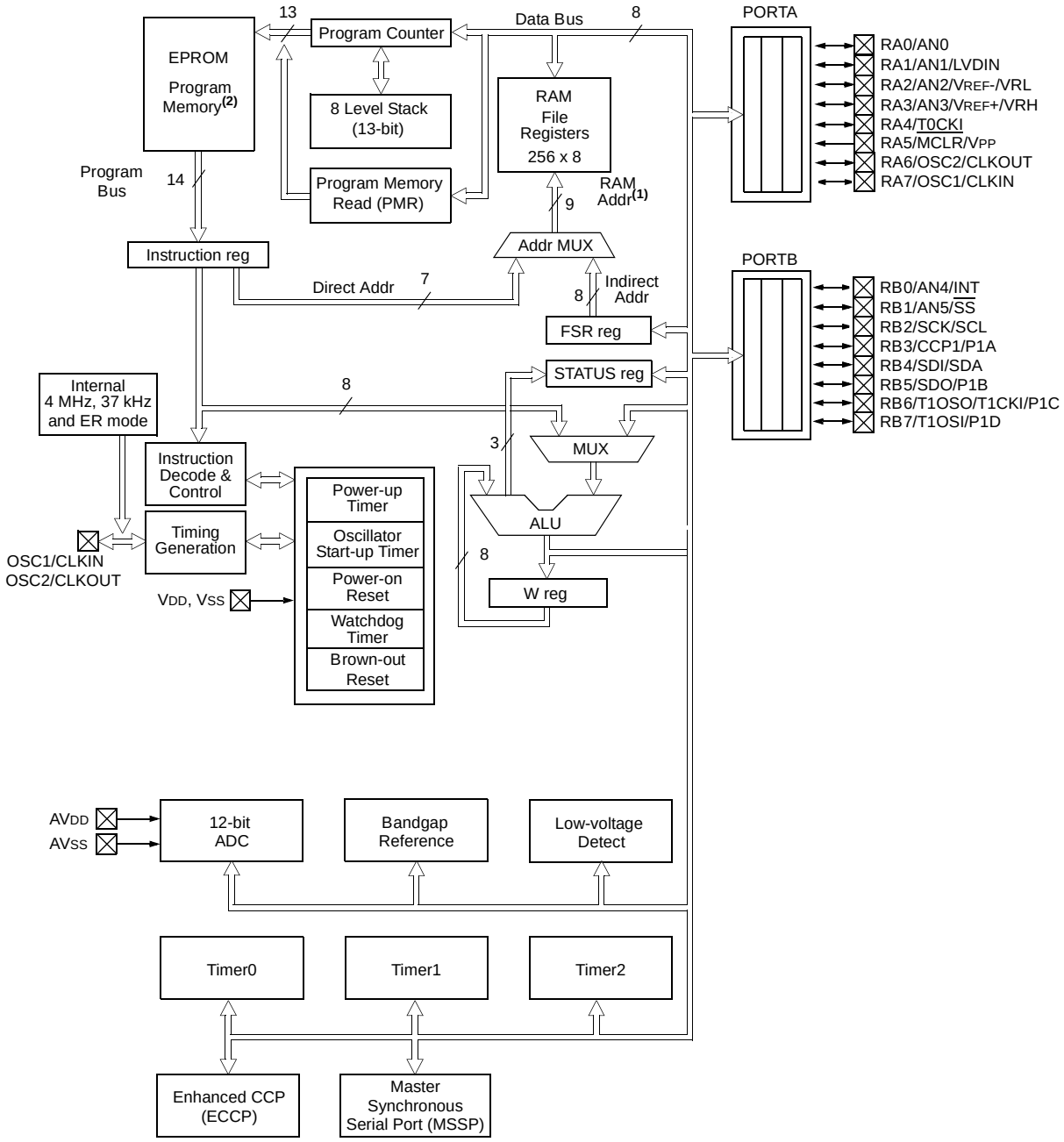
FIGURE 1-2: PIC16C770/771 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.
2: Program memory for PIC16C770 is 2K x 14. Program memory for PIC16C771 is 4K x 14.

TABLE 1-1: PIC16C717/770/771 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0	RA0	ST	CMOS	Bi-directional I/O
	AN0	AN		A/D input
RA1/AN1/LVDIN	RA1	ST	CMOS	Bi-directional I/O
	AN1	AN		A/D input
	LVDIN	AN		LVD input reference
RA2/AN2/VREF-/VRL	RA2	ST	CMOS	Bi-directional I/O
	AN2	AN		A/D input
	VREF-	AN		Negative analog reference input
	VRL		AN	Internal voltage reference low output
RA3/AN3/VREF+/VRH	RA3	ST	CMOS	Bi-directional I/O
	AN3	AN		A/D input
	VREF+	AN		Positive analog reference input
	VRH		AN	Internal voltage reference high output
RA4/T0CKI	RA4	ST	OD	Bi-directional I/O
	T0CKI	ST		TMR0 clock input
RA5/$\overline{MCLR}$/VPP	RA5	ST		Input port
	$\overline{MCLR}$	ST		Master clear
	VPP	Power		Programming voltage
RA6/OSC2/CLKOUT	RA6	ST	CMOS	Bi-directional I/O
	OSC2		XTAL	Crystal/resonator
	CLKOUT		CMOS	FOSC/4 output
RA7/OSC1/CLKIN	RA7	ST	CMOS	Bi-directional I/O
	OSC1	XTAL		Crystal/resonator
	CLKIN	ST		External clock input/ER resistor connection
RB0/AN4/INT	RB0	TTL	CMOS	Bi-directional I/O**(1)**
	AN4	AN		A/D input
	INT	ST		Interrupt input
RB1/AN5/$\overline{SS}$	RB1	TTL	CMOS	Bi-directional I/O**(1)**
	AN5	AN		A/D input
	$\overline{SS}$	ST		SSP slave select input
RB2/SCK/SCL	RB2	TTL	CMOS	Bi-directional I/O**(1)**
	SCK	ST	CMOS	Serial clock I/O for SPI
	SCL	ST	OD	Serial clock I/O for I^2C
RB3/CCP1/P1A	RB3	TTL	CMOS	Bi-directional I/O**(1)**
	CCP1	ST	CMOS	Capture 1 input/Compare 1 output
	P1A		CMOS	PWM P1A output
RB4/SDI/SDA	RB4	TTL	CMOS	Bi-directional I/O**(1)**
	SDI	ST		Serial data in for SPI
	SDA	ST	OD	Serial data I/O for I^2C
RB5/SDO/P1B	RB5	TTL	CMOS	Bi-directional I/O**(1)**
	SDO		CMOS	Serial data out for SPI
	P1B		CMOS	PWM P1B output

Note 1: Bit programmable pull-ups.

2: Only in PIC16C770/771 devices.

TABLE 1-1: PIC16C717/770/771 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB6/T1OSO/T1CKI/P1C	RB6	TTL	CMOS	Bi-directional I/O(1)
	T1OSO		XTAL	Crystal/Resonator
	T1CKI	CMOS		TMR1 clock input
	P1C		CMOS	PWM P1C output
RB7/T1OSI/P1D	RB7	TTL	CMOS	Bi-directional I/O(1)
	T1OSI	XTAL		TMR1 crystal/resonator
	P1D		CMOS	PWM P1D output
VSS	VSS	Power		Ground reference for logic and I/O pins
VDD	VDD	Power		Positive supply for logic and I/O pins
AVSS(2)	AVSS	Power		Ground reference for analog
AVDD(2)	AVDD	Power		Positive supply for analog

Note 1: Bit programmable pull-ups.

2: Only in PIC16C770/771 devices.

2.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note:	Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTERRUPT CONTROL REGISTER (INTCON: 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit**(1)**
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit**(1)**
1 = At least one of the RB<7:0> pins changed state (must be cleared in software)
0 = None of the RB<7:0> pins have changed state

Note 1: Individual RB pin interrupt-on-change can be enabled/disabled from the Interrupt-on-Change PORTB register (IOCB).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.6 PIE2 REGISTER

This register contains the individual enable bits for the SSP bus collision and low voltage detect interrupts.

REGISTER 2-6: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (PIE2: 8Dh)

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
LVDIE	—	—	—	BCLIE	—	—	—
bit 7							bit 0

bit 7 **LVDIE:** Low Voltage Detect Interrupt Enable bit
1 = LVD Interrupt is enabled
0 = LVD Interrupt is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **BCLIE:** Bus Collision Interrupt Enable bit
1 = Bus Collision interrupt is enabled
0 = Bus Collision interrupt is disabled

bit 2-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

2.2.2.8 PCON REGISTER

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external MCLR Reset or WDT Reset. Those devices with brown-out detection circuitry contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

The PCON register also contains the frequency select bit of the INTRC or ER oscillator.

Note:	$\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

REGISTER 2-8: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	U-0	R/W-1	U-0	R/W-q	R/W-q
—	—	—	—	OSCF	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OSCF:** Oscillator Speed bit

INTRC Mode
1 = 4 MHz nominal
0 = 37 kHz nominal
ER Mode
1 = Oscillator frequency depends on the external resistor value on the OSC1 pin.
0 = 37 kHz nominal
All other modes
x = Ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit (See Section 2.2.2.8 Note)

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Legend:		q = Value depends on conditions	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-2: WEAK PULL-UP PORTB REGISTER (WPUB: 95h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit 7							bit 0

bit 7-0 **WPUB<7:0>:** PORTB Weak Pull-Up Control bits

1 = Weak pull-up enabled
0 = Weak pull-up disabled

Note 1: For the WPUB register setting to take effect, the $\overline{\text{RBPU}}$ bit in the OPTION_REG register must be cleared.

2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRIS = 0).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-3: INTERRUPT-ON-CHANGE PORTB REGISTER (IOCB: 96h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
bit 7							bit 0

bit 7-0 **IOCB<7:0>:** Interrupt-on-Change PORTB Control bits

1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note: The interrupt enable bits GIE and RBIE in the INTCON Register must be set for individual interrupts to be recognized.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.0 PROGRAM MEMORY READ (PMR)

Program memory is readable during normal operation (full VDD range). It is indirectly addressed through the Special Function Registers:

- PMCON1
- PMDATH
- PMDATL
- PMADRH
- PMADRL

When interfacing the program memory block, the PMDATH & PMDATL registers form a 2-byte word, which holds the 14-bit data. The PMADRH & PMADRL registers form a 2-byte word, which holds the 12-bit address of the program memory location being accessed. Mid-range devices have up to 8K words of program EPROM with an address range from 0h to 3FFFh. When the device contains less memory than the full address range of the PMADRH:PMARDL registers, the Most Significant bits of the PMADRH register are ignored.

4.1 PMCON1 REGISTER

PMCON1 is the control register for program memory accesses.

Control bit RD initiates a read operation. This bit cannot be cleared, only set, in software. It is cleared in hardware at completion of the read operation.

REGISTER 4-1: PROGRAM MEMORY READ CONTROL REGISTER 1 (PMCON1: 18Ch)

R-1	U-0	U-0	U-0	U-0	U-0	U-0	R/S-0
Reserved	—	—	—	—	—	—	RD
bit 7							bit 0

bit 7 **Reserved:** Read as ‘1’

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **RD**: Read Control bit

1 = Initiates a Program memory read (read takes 2 cycles). RD is cleared in hardware.
0 = Reserved

Legend:		S = Settable (cleared in hardware)	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

4.2 PMDATH AND PMDATL REGISTERS

The PMDATH:PMDATL registers are loaded with the contents of program memory addressed by the PMADRH and PMADRL registers upon completion of a Program Memory Read command.

TABLE 4-1: PROGRAM MEMORY READ REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--xx xxxx	--uu uuuu
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	xxxx xxxx	uuuu uuuu
10Fh	PMADRH	—	—	—	—	PMA11	PMA10	PMA9	PMA8	---- xxxx	---- uuuu
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Program Memory Read.

6.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
  (Two 8-bit registers; TMR1H and TMR1L)
- Readable and writable (Both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- RESET from ECCP module trigger

Timer1 has a control register, shown in Register 6-1. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Figure 6-2 is a simplified block diagram of the Timer1 module.

Additional information on timer modules is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

6.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

The Operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

REGISTER 6-1: TIMER1 CONTROL REGISTER (T1CON: 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off **(1)**

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from pin RB6/T1OSO/T1CKI /P1C (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: The oscillator inverter and feedback resistor are turned off to eliminate power drain.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 9-5: SPI SLAVE MODE WAVEFORM (CKE = 0)

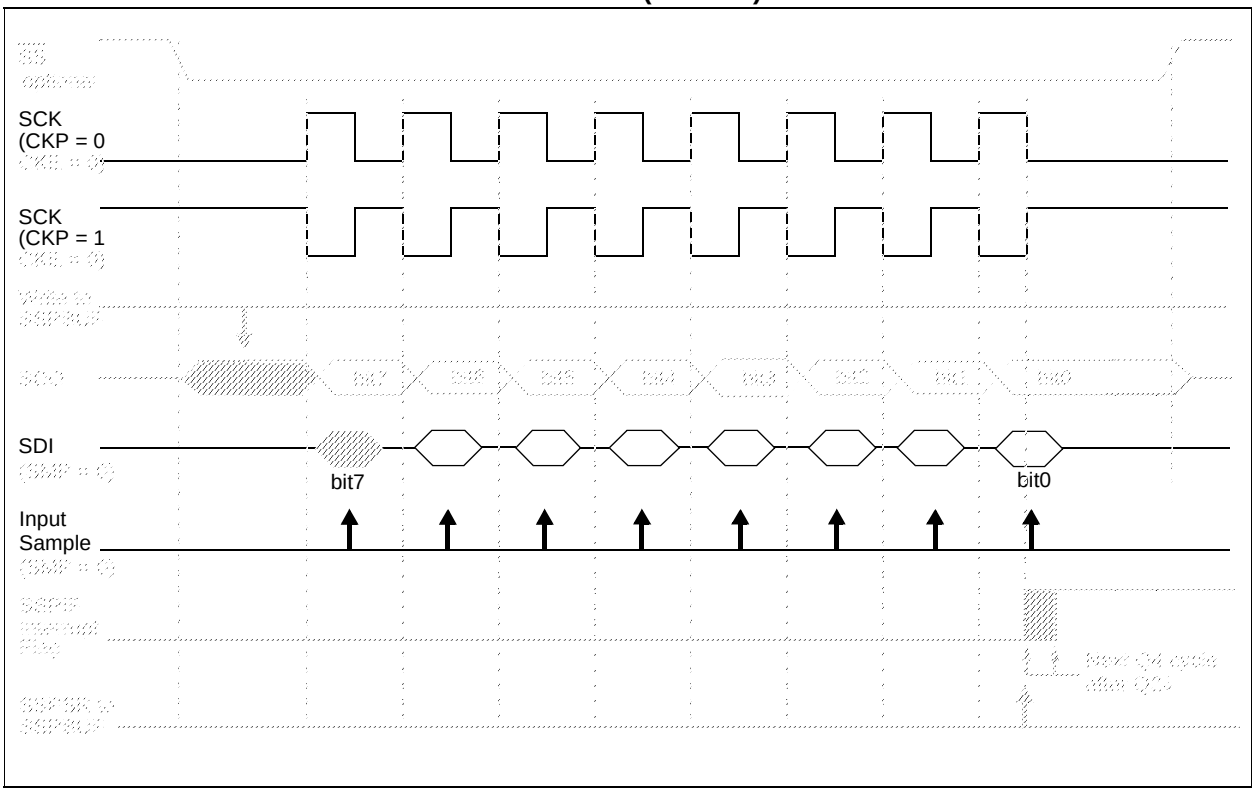
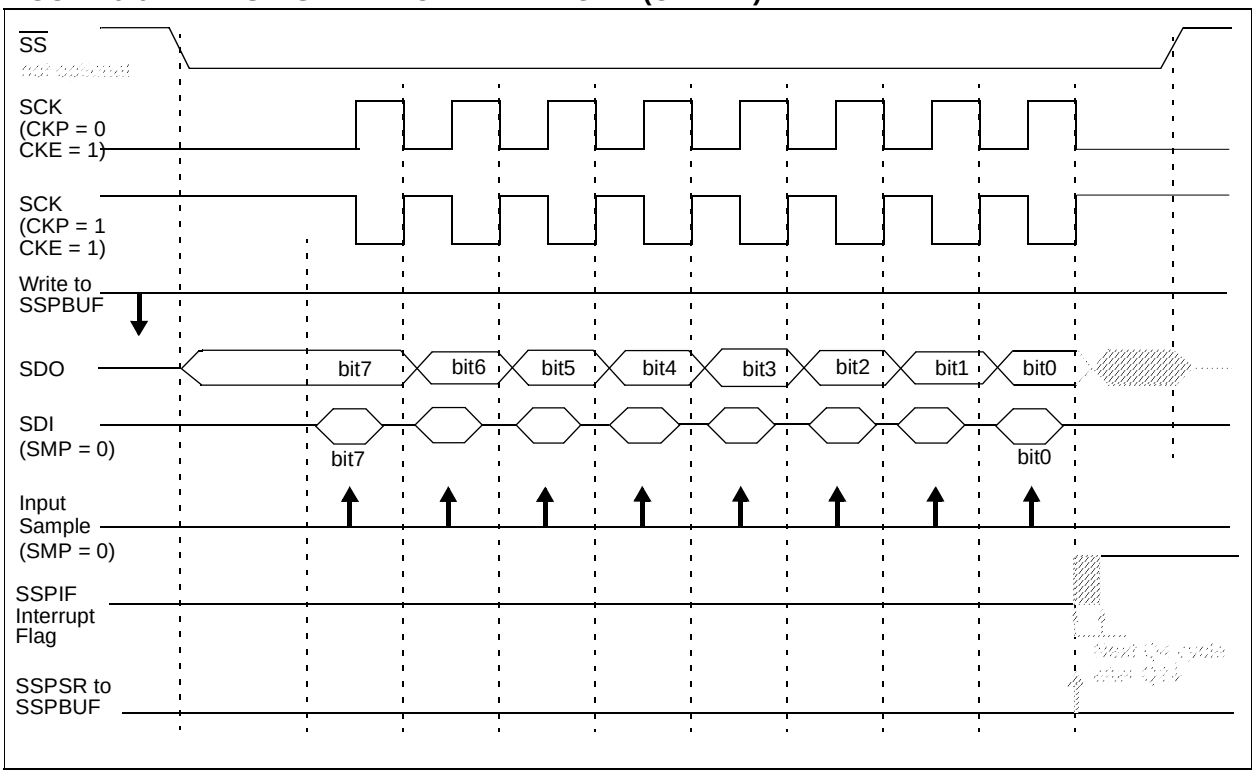


FIGURE 9-6: SPI SLAVE MODE WAVEFORM (CKE = 1)



9.2.7 MULTI-MASTER OPERATION

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET or when the MSSP module is disabled. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware, with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A START Condition
- A Repeated START Condition
- An Acknowledge Condition

Refer to Application Note AN578, *"Use of the SSP Module in the I^2C™ Multi-Master Environment."*

9.2.8 I^2C MASTER OPERATION

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON and by setting the SSPEN bit. Once Master mode is enabled, the user has six options.

1. Assert a START condition on SDA and SCL.
2. Assert a Repeated START condition on SDA and SCL.
3. Write to the SSPBUF register initiating transmission of data/address.
4. Generate a STOP condition on SDA and SCL.
5. Configure the I^2C port to receive data.
6. Generate an Acknowledge condition at the end of a received byte of data.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the I^2C bus will not be released.

Note:	The MSSP Module, when configured in I^2C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a START condition and immediately write the SSPBUF register to initiate transmission before the START condition is complete. In this case, the SSPBUF will not be written to, and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

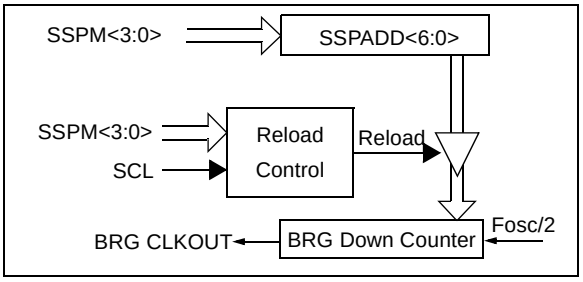
9.2.9 BAUD RATE GENERATOR

The baud rate generator used for SPI mode operation is used in the I^2C Master mode to set the SCL clock frequency. Standard SCL clock frequencies are 100 kHz, 400 kHz, and 1 MHz. One of these frequencies can be achieved by setting the SSPADD register to the appropriate number for the selected Fosc frequency. One half of the SCL period is equal to [(SSPADD+1) •2]/Fosc.

The baud rate generator reload value is contained in the lower seven bits of the SSPADD register (Figure 9-14). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload occurs. The BRG count is decremented twice per instruction cycle (TCY) on the Q2 and Q4 clock.

In I^2C Master mode, the BRG is reloaded automatically provided that the SCL line is sampled high. For example, if Clock Arbitration is taking place, the BRG reload will be suppressed until the SCL line is released by the slave allowing the pin to float high (Figure 9-15).

FIGURE 9-14: BAUD RATE GENERATOR BLOCK DIAGRAM



9.2.17.1 BUS COLLISION DURING A START CONDITION

During a START condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the START condition (Figure 9-24).

b) SCL is sampled low before SDA is asserted low. (Figure 9-25).

During a START condition both the SDA and the SCL pins are monitored.

If:

the SDA pin is already low
or the SCL pin is already low,

then:

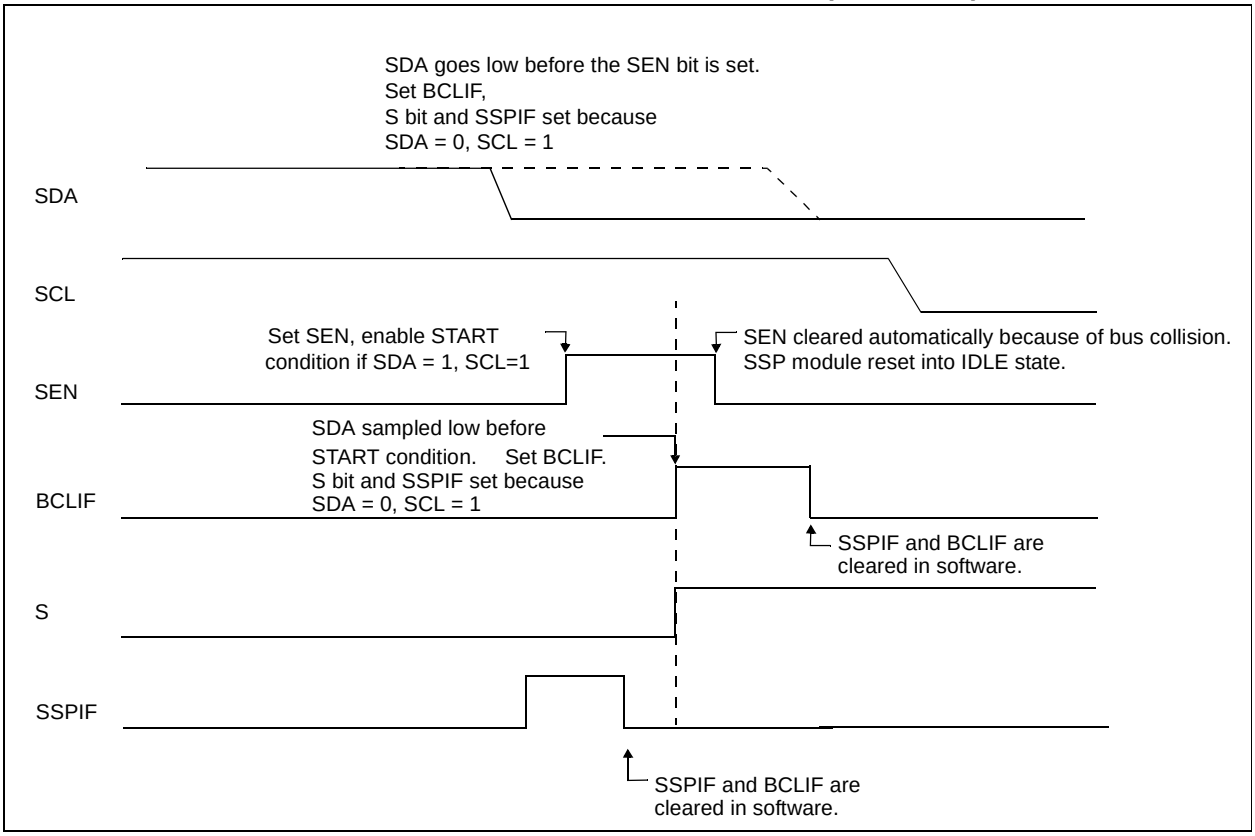
the START condition is aborted,
and the BCLIF flag is set,
and the SSP module is reset to its IDLE state (Figure 9-24).

The START condition begins with the SDA and SCL pins de-asserted. When the SDA pin is sampled high, the baud rate generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs, because it is assumed that another master is attempting to drive a data '1' during the START condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 9-26). If however a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The baud rate generator is then reloaded and counts down to 0, and during this time, if the SCL pin is sampled as '0', a bus collision does not occur. At the end of the BRG count the SCL pin is asserted low.

Note:	The reason that bus collision is not a factor during a START condition is that no two bus masters can assert a START condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision, because the two masters must be allowed to arbitrate the first address following the START condition. If the address is the same, arbitration must be allowed to continue into the data portion, REPEATED START or STOP conditions.

FIGURE 9-24: BUS COLLISION DURING START CONDITION (SDA ONLY)



11.4 A/D Conversions

Example 11-1 shows an example that performs an A/D conversion. The port pins are configured as analog inputs. The analog reference V_{REF+} is the device AV_{DD} and the analog reference V_{REF-} is the device AV_{SS}. The A/D interrupt is enabled and the A/D conversion clock is T_{RC}. The conversion is performed on the AN0 channel.

EXAMPLE 11-1: PERFORMING AN A/D CONVERSION

```
    BSF     STATUS, RP0    ;Select Bank 1
    CLRF    ADCON1         ;Configure A/D Voltage Reference
    MOVLW   0x01
    MOVWF   ANSEL          ;disable AN0 digital input buffer
    MOVWF   TRISA          ;RA0 is input mode
    BSF     PIE1, ADIE     ;Enable A/D interrupt
    BCF     STATUS, RP0    ;Select Bank 0
    MOVLW   0xC1           ;RC clock, A/D is on,
                           ;Ch 0 is selected
    MOVWF   ADCON0         ;
    BCF     PIR1, ADIF     ;Clear A/D Int Flag
    BSF     INTCON, PEIE   ;Enable Peripheral
    BSF     INTCON, GIE    ;Enable All Interrupts
;
; Ensure that the required sampling time for the
; selected input channel has lapsed. Then the
; conversion may be started.
    BSF     ADCON0, GO     ;Start A/D Conversion
            :              ;The ADIF bit will be
                           ;set and the GO/DONE bit
            :              ;cleared upon completion-
                           ;of the A/D conversion.
; Wait for A/D completion and read ADRESH:ADRESL for result.
```

TABLE 12-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

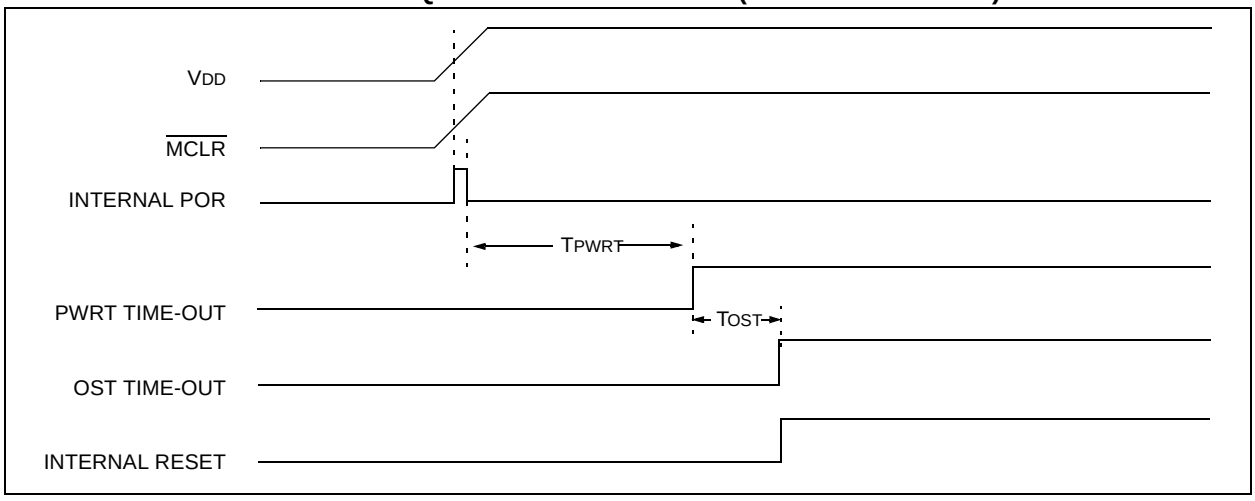
Register	Power-on Reset or Brown-out Reset	$\overline{\text{MCLR}}$ Reset or WDT Reset	Wake-up via WDT or Interrupt
P1DEL	0000 0000	0000 0000	uuuu uuuu
REFCON	0000 ----	0000 ----	uuuu ----
LVDCON	--00 0101	--00 0101	--uu uuuu
ANSEL	--11 1111	--11 1111	--uu uuuu
ADRESL	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	0000 0000	0000 0000	uuuu uuuu
PMDATL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMADRL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMDATH	--xx xxxx	--uu uuuu	--uu uuuu
PMADRH	---- xxxx	---- uuuu	---- uuuu
PMCON1	1--- ---0	1--- ---0	1--- ---0

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

2: See Table 12-5 for RESET value for specific condition.

FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})



RETFIE **Return from Interrupt**

Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

RETLW **Return with Literal in W**

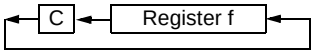
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RETURN **Return from Subroutine**

Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

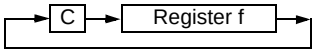
RLF **Rotate Left f through Carry**

Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



RRF **Rotate Right f through Carry**

Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



SLEEP

Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 12.8 for more details.

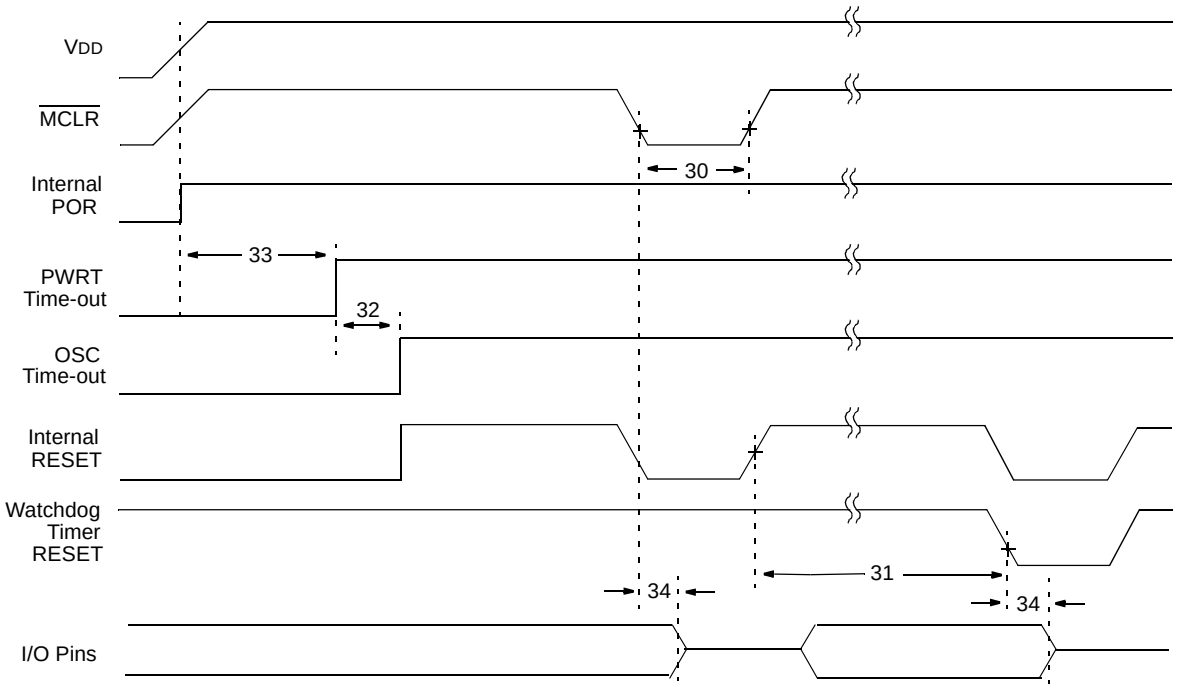
TABLE 15-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC16C717/770/771 AND PIC16LC717/770/771

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating Voltage VDD range is described in Section and Section					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)***	**Max**	**Units**	**Conditions**
	FIRC	Internal Calibrated RC Frequency	3.65	4.00	4.28	MHz	VDD = 5.0V
		Internal RC Frequency*	3.55	4.00	4.31	MHz	VDD = 2.5V

* These parameters are characterized but not tested.

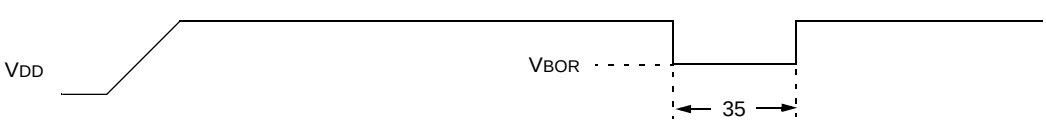
Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



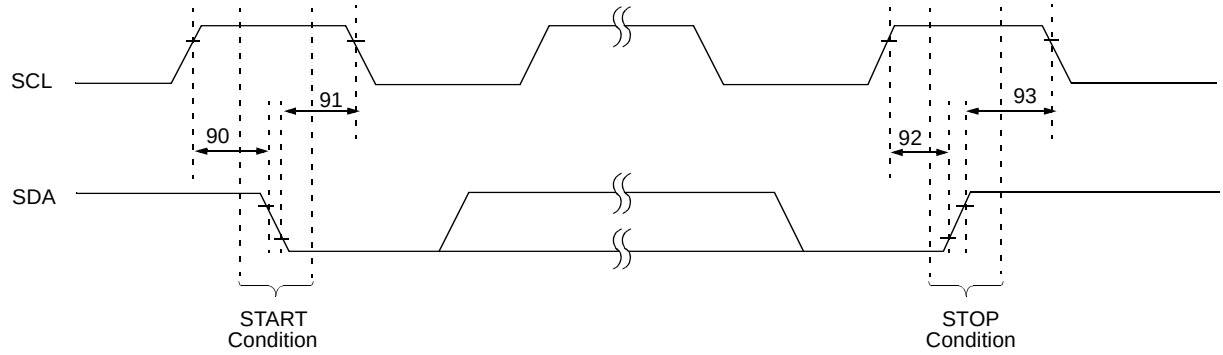
Note: Refer to Figure 15-4 for load conditions.

FIGURE 15-8: BROWN-OUT RESET TIMING



15.6 Master SSP I²C Mode Timing Waveforms and Requirements

FIGURE 15-22: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS



Note: Refer to Figure 15-4 for load conditions.

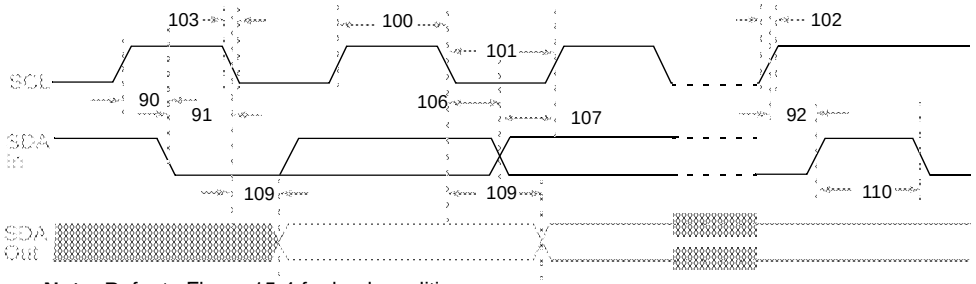
TABLE 15-21: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	Only relevant for a Repeated START condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
93*	THD:STO	STOP condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		

* These parameters are characterized but not tested. For the value required by the I²C specification, please refer to the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

Maximum pin capacitance = 10 pF for all I²C pins.

FIGURE 15-23: MASTER SSP I²C BUS DATA TIMING



Note: Refer to Figure 15-4 for load conditions.

NOTES: