Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

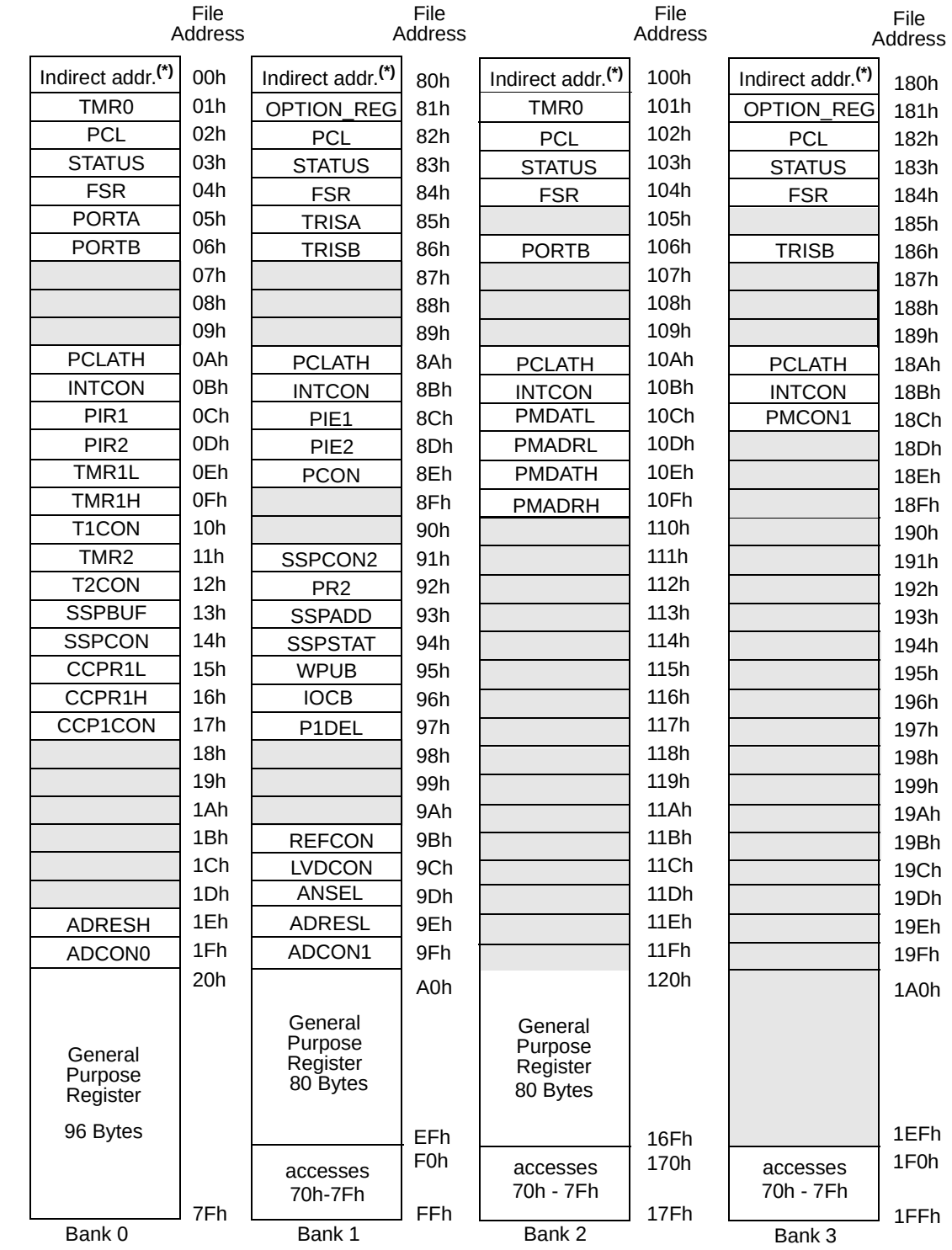
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc717-i-ss

NOTES:

© 1999-2013 Microchip Technology Inc.

FIGURE 2-3: REGISTER FILE MAP



© 1999-2013 Microchip Technology Inc.

2.2.2.8 PCON REGISTER

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external MCLR Reset or WDT Reset. Those devices with brown-out detection circuitry contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

The PCON register also contains the frequency select bit of the INTRC or ER oscillator.

Note:	$\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

REGISTER 2-8: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	U-0	R/W-1	U-0	R/W-q	R/W-q
—	—	—	—	OSCF	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OSCF:** Oscillator Speed bit

INTRC Mode
1 = 4 MHz nominal
0 = 37 kHz nominal
ER Mode
1 = Oscillator frequency depends on the external resistor value on the OSC1 pin.
0 = 37 kHz nominal
All other modes
x = Ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit (See Section 2.2.2.8 Note)

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

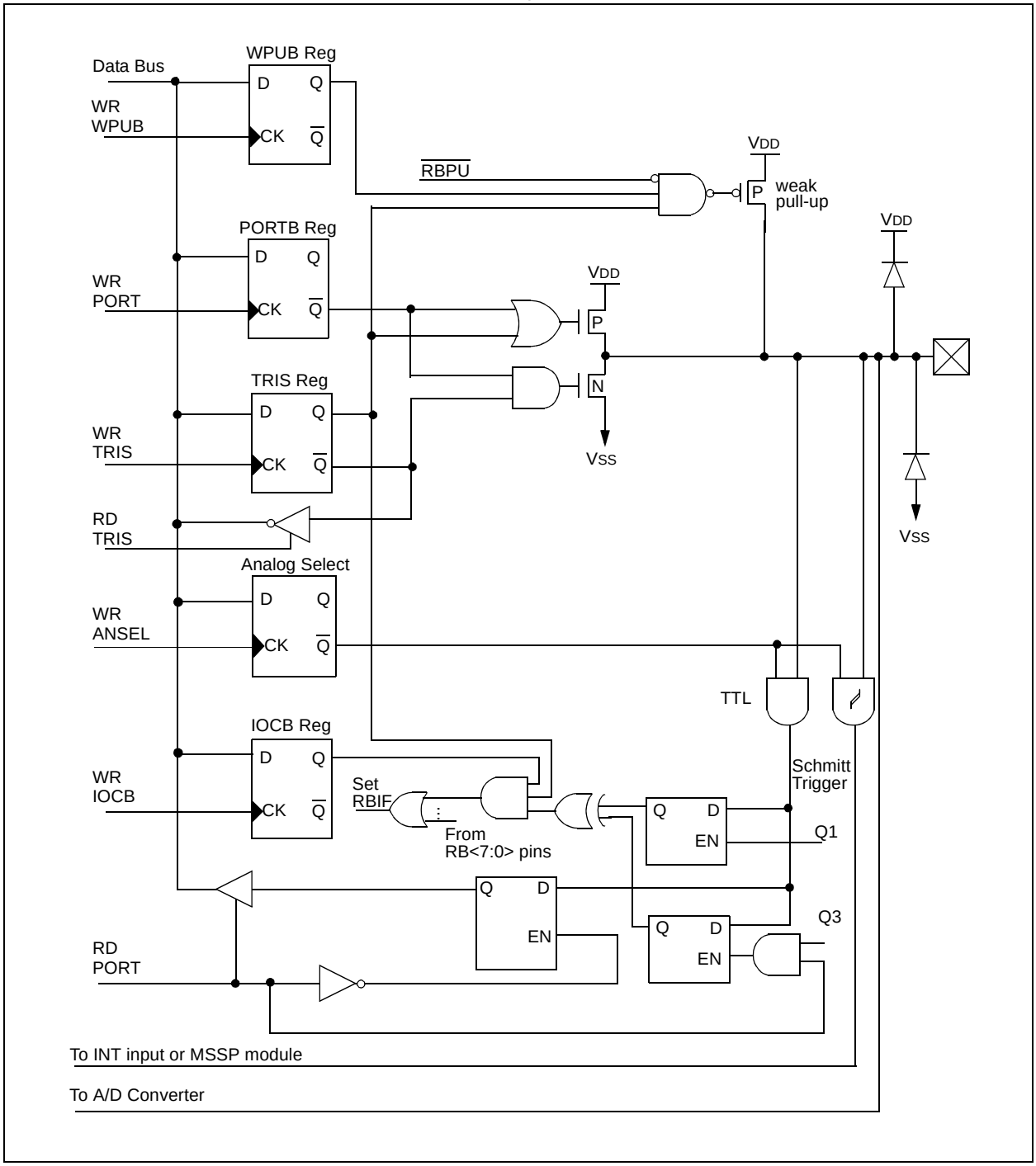
Legend:		q = Value depends on conditions	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The RB0 pin is multiplexed with the A/D converter analog input 4 and the external interrupt input (RB0/AN4/INT). When the pin is used as analog input, the ANSEL register must have the proper value to select the RB0 pin as Analog mode.

The RB1 pin is multiplexed with the A/D converter analog input 5 and the MSSP module slave select input (RB1/AN5/$\overline{SS}$). When the pin is used as analog input, the ANSEL register must have the proper value to select the RB1 pin as Analog mode.

Note:	Upon RESET, the ANSEL register configures the RB1 and RB0 pins as analog inputs. Both RB1 and RB0 pins will read as '1'.

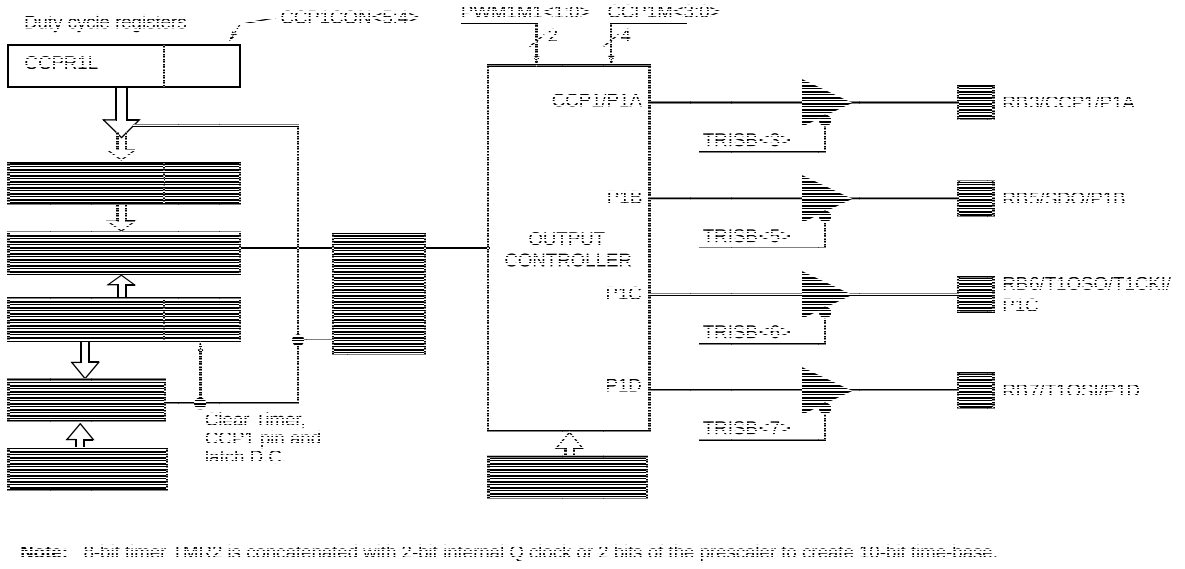
FIGURE 3-7: BLOCK DIAGRAM OF RB0/AN4/INT, RB1/AN5/$\overline{SS}$ PIN



8.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the ECCP module produces up to a 10-bit resolution PWM output. Figure 8-3 shows the simplified PWM block diagram.

FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM PERIOD} = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (\text{TMR2 PRESCALE VALUE})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 7.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

© 1999-2013 Microchip Technology Inc.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

PWM duty cycle = (CCPR1L:CCP1CON<5:4>) • TOSC • (TMR2 prescale value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)} \text{bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

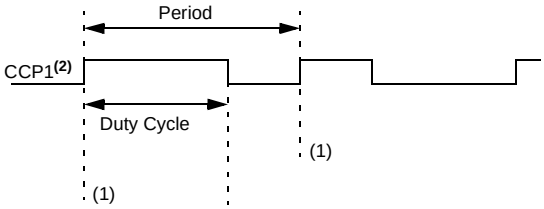
8.3.3 PWM OUTPUT CONFIGURATIONS

The PWM1M1 bits in the CCP1CON register allows one of the following configurations:

- Single output
- Half-Bridge output
- Full-Bridge output, Forward mode
- Full-Bridge output, Reverse mode

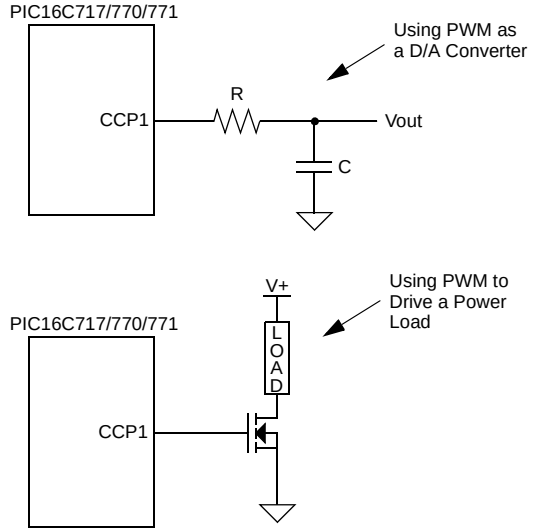
In the Single Output mode, the RB3/CCP1/P1A pin is used as the PWM output. Since the CCP1 output is multiplexed with the PORTB<3> data latch, the TRISB<3> bit must be cleared to make the CCP1 pin an output.

FIGURE 8-4: SINGLE PWM OUTPUT



Note 1: At this time, the TMR2 register is equal to the PR2 register.
2: Output signal is shown as asserted high.

FIGURE 8-5: EXAMPLE OF SINGLE OUTPUT APPLICATION



In the Half-Bridge Output mode, two pins are used as outputs. The RB3/CCP1/P1A pin has the PWM output signal, while the RB5/SDO/P1B pin has the complementary PWM output signal. This mode can be used for half-bridge applications, as shown on Figure 8-7, or for full-bridge applications, where four power switches are being modulated with two PWM signal.

Since the P1A and P1B outputs are multiplexed with the PORTB<3> and PORTB<5> data latches, the TRISB<3> and TRISB<5> bits must be cleared to configure P1A and P1B as outputs.

In Half-Bridge Output mode, the programmable deadband delay can be used to prevent shoot-through current in bridge power devices. See Section 8.3.5 for more details of the deadband delay operations.

REGISTER 9-1: SYNC SERIAL PORT STATUS REGISTER (SSPSTAT: 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

bit 7 **SMP:** Sample bit
SPI Master Mode
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave Mode
SMP must be cleared when SPI is used in Slave mode
In I^2C Master or Slave mode:
1= Slew rate control disabled for Standard Speed mode (100 kHz and 1 MHz)
0= Slew rate control enabled for High Speed mode (400 kHz)

bit 6 **CKE:** SPI Clock Edge Select (Figure 9-3, Figure 9-5, and Figure 9-6)
CKP = 0
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK
CKP = 1
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** STOP bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared)
1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)
0 = STOP bit was not detected last

bit 3 **S:** START bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared)
1 = Indicates that a START bit has been detected last (this bit is '0' on RESET)
0 = START bit was not detected last

bit 2 **R/$\overline{W}$:** Read/$\overline{\text{Write}}$ bit information (I^2C mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit, or $\overline{\text{NACK}}$ bit.
In I^2C Slave mode:
1 = Read
0 = Write
In I^2C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress.
ORing this bit with SEN, RSEN, PEN, RCEN, or AKEN will indicate if the MSSP is in IDLE mode

bit 1 **UA:** Update Address (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0 **BF:** Buffer Full Status bit
Receive (SPI and I^2C modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty
Transmit (I^2C mode only)
1 = Data Transmit in progress (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is full
0 = Data Transmit complete (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is empty

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

© 1999-2013 Microchip Technology Inc.

9.2.11 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated START condition occurs when the RSEN bit (SSPCON2<1>) is set high while the I²C module is in the idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the baud rate generator is loaded with the contents of SSPADD<6:0> and begins counting. The SDA pin is released (brought high) for one baud rate generator count (TBRG). When the baud rate generator times out, if SDA is sampled high, the SCL pin will be de-asserted (brought high). When SCL is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG period. This action is then followed by assertion of the SDA pin (SDA is low) for one TBRG period while SCL is high. As soon as a START condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. Following this, the baud rate generator is reloaded with the contents of SSPAD<6:0> and begins counting. When the BRG times out a third time, the RSEN bit in the SSPCON2 register is automatically cleared and SCL is pulled low. The SSPIF flag is set, which indicates the Restart sequence is complete.

Note 1: If RSEN is set while another event is in progress, it will not take effect. Queuing of events is not allowed.

2: A bus collision during the Repeated START condition occurs if either of the following is true:

a) SDA is sampled low when SCL goes from low to high.

b) SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data “1”.

Immediately following the SSPIF bit transition to true, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then perform one of the following:

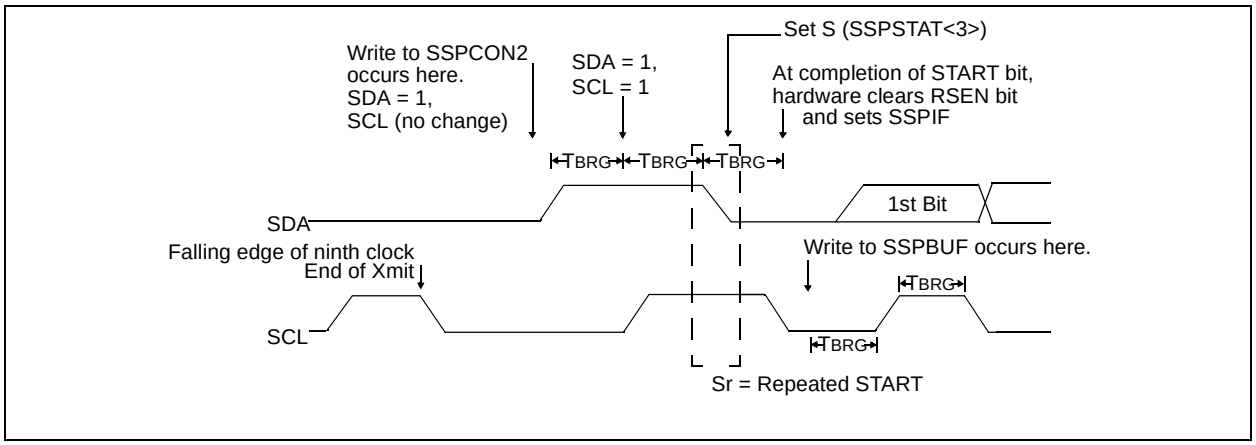
- Transmit an additional eight bits of address (if the user transmitted the first half of a 10-bit address with R/$\overline{W}$ = 0),
- Transmit eight bits of data (if the user transmitted a 7-bit address with R/$\overline{W}$ = 0), or
- Receive eight bits of data (if the user transmitted either the first half of a 10-bit address or a 7-bit address with R/$\overline{W}$ = 1).

9.2.11.1 WCOL STATUS FLAG

If the user writes the SSPBUF when a Repeated START sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn’t occur).

Note: Because queueing of events is not allowed, writing of the lower five bits of SSPCON2 is disabled until the Repeated START condition is complete.

FIGURE 9-17: REPEAT START CONDITION WAVEFORM



 © 1999-2013 Microchip Technology Inc.

9.2.16 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or repeated START/STOP condition, de-asserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 9-22).

FIGURE 9-22: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE

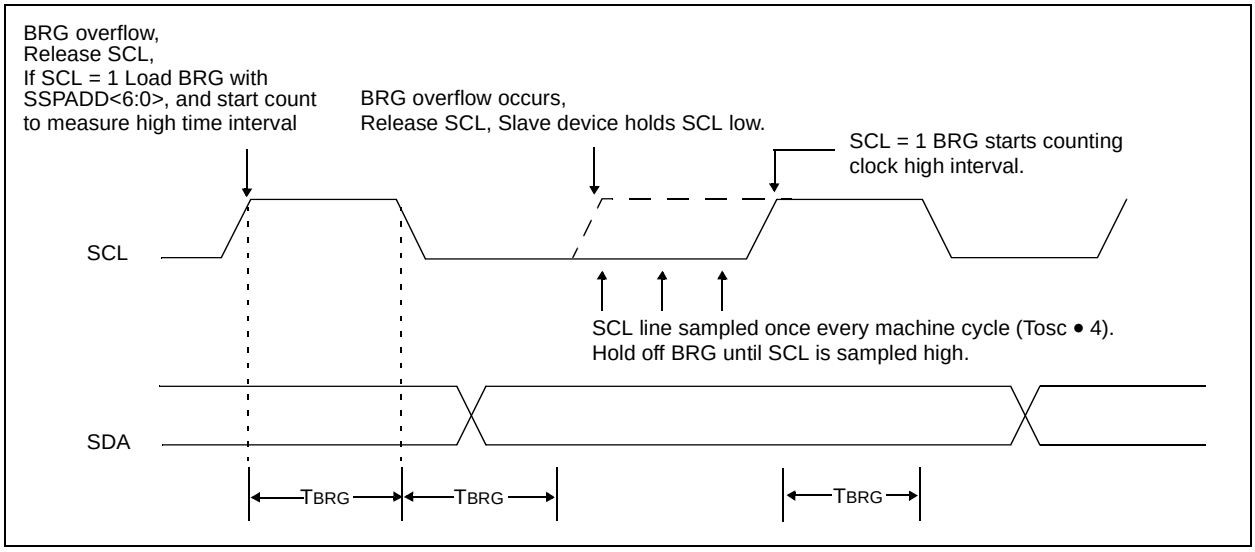
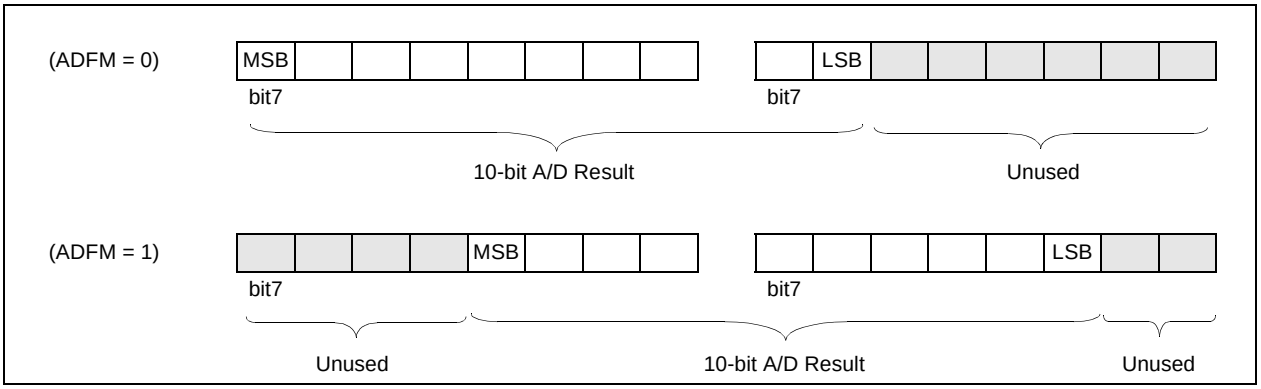


FIGURE 11-2: PIC16C717 10-BIT A/D RESULT FORMAT



After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS and ANSEL bits selected as an input. To determine acquisition time, see Section 11.6. After this acquisition time has elapsed, the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

11.2 Configuring the A/D Module

11.2.1 CONFIGURING ANALOG PORT PINS

The ANSEL and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted. The proper ANSEL bits must be set (analog input) to disable the digital input buffer.

The A/D operation is independent of the state of the TRIS bits and the ANSEL bits.

Note 1:	When reading the PORTA register, all pins configured as analog input channels will read as '0'.
2:	When reading the PORTB register, all pins configured as analog pins on PORTB will be read as '1'.
3:	Analog levels on any pin that is defined as a digital input, including the ANx pins, may cause the input buffer to consume current that is out of the devices specification.

11.2.2 CONFIGURING THE REFERENCE VOLTAGES

The VCFG bits in the ADCON1 register configure the A/D module reference inputs. The reference high input can come from an internal reference (VRH) or (VRL), an external reference (V_{REF+}), or AV_{DD}. The low reference input can come from an internal reference (VRL), an external reference (V_{REF-}), or AV_{SS}. If an external reference is chosen for the reference high or reference low inputs, the port pin that multiplexes the incoming external references is configured as an analog input, regardless of the values contained in the A/D port configuration bits (PCFG<3:0>).

© 1999-2013 Microchip Technology Inc.

RETFIE **Return from Interrupt**

Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

RETLW **Return with Literal in W**

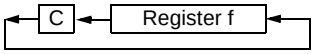
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RETURN **Return from Subroutine**

Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

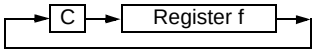
RLF **Rotate Left f through Carry**

Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



RRF **Rotate Right f through Carry**

Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



SLEEP

Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 12.8 for more details.

14.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ® Demonstration Board

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or ‘C’)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

14.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

14.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI ‘C’ compilers for Microchip’s PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

© 1999-2013 Microchip Technology Inc.

15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16C717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IDD	**Supply Current(2)**					
D010D		**PIC16LC7XX**		1.0	2.0	mA	FOSC = 10 MHz, VDD = 3V, -40°C to 85°C
D010E					3.0		FOSC = 10 MHz, VDD = 3V, -40°C to 125°C
D010G				0.36	1.0	mA	FOSC = 4 MHz, VDD = 2.5V, -40°C to 125°C
D010K				11	45	µA	FOSC = 32 kHz, VDD = 2.5V, -40°C to 125°C
	IDD	**Supply Current(2)**					
D010		**PIC16C7XX**		4.0	7.5	mA	FOSC = 20 MHz, VDD = 5.5V, -40°C to 85°C
D010A					12.0		FOSC = 20 MHz, VDD = 5.5V, -40°C to 125°C
D010B				2.5	5.0	mA	FOSC = 20 MHz, VDD = 4V, -40°C to 85°C
D010C					6.0		FOSC = 20 MHz, VDD = 4V, -40°C to 125°C
D010F				0.55	1.5	mA	FOSC = 4 MHz, VDD = 4V, -40°C to 125°C
D010H				30	80	µA	FOSC = 32 kHz, VDD = 4V, -40°C to 85°C
D010J					95		FOSC = 32 kHz, VDD = 4V, -40°C to 125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active Operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

15.4.2 LOW VOLTAGE DETECT MODULE (LVD)

FIGURE 15-13: LOW VOLTAGE DETECT CHARACTERISTICS

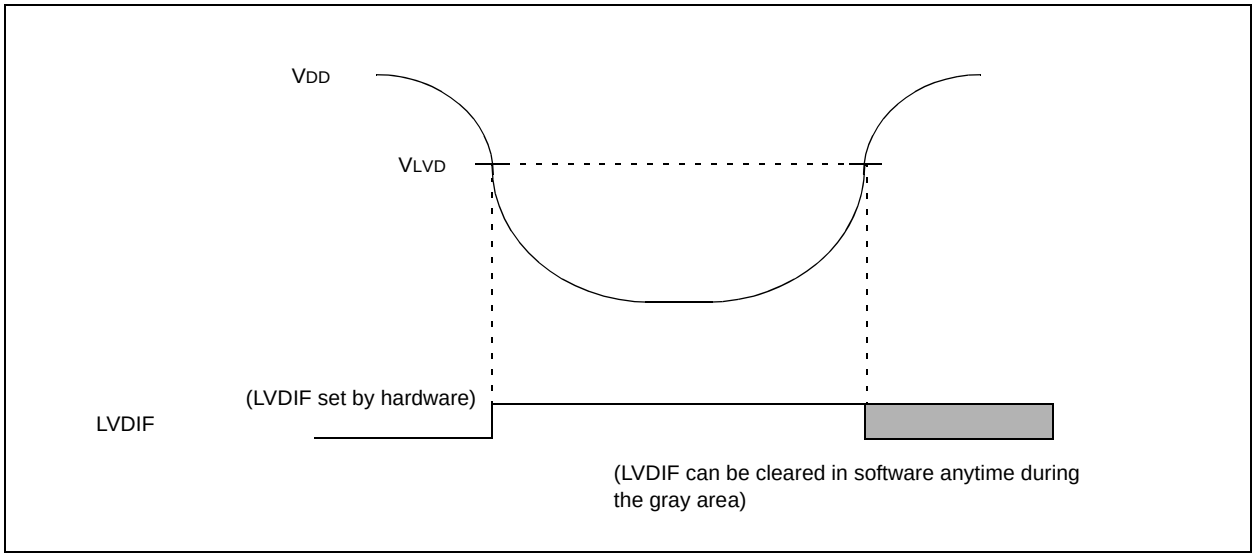


TABLE 15-8: ELECTRICAL CHARACTERISTICS: LVD

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC Characteristics Section 15.1.					
Param. No.	**Characteristic**		**Symbol**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420*	LVD Voltage	LVV = 0100	VLVD	2.5	2.58	2.66	V	
		LVV = 0101		2.7	2.78	2.86	V	
		LVV = 0110		2.8	2.89	2.98	V	
		LVV = 0111		3.0	3.1	3.2	V	
		LVV = 1000		3.3	3.41	3.52	V	
		LVV = 1001		3.5	3.61	3.72	V	
		LVV = 1010		3.6	3.72	3.84	V	
		LVV = 1011		3.8	3.92	4.04	V	
		LVV = 1100		4.0	4.13	4.26	V	
		LVV = 1101		4.2	4.33	4.46	V	
		LVV = 1110		4.5	4.64	4.78	V	

* These parameters are characterized but not tested.

Note 1: Production tested at Tamb = 25°C. Specifications over temperature limits ensured by characterization.

© 1999-2013 Microchip Technology Inc.

TABLE 15-14: PIC16C717 AND PIC16LC717 A/D CONVERTER CHARACTERISTICS:

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	Min. resolution for A/D is 4.1 mV, VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A03	EIL	Integral error	—	—	±1	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A04	EDL	Differential error	—	—	±1	LSb	No missing codes to 10 bits VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A06	EOFF	Offset error	—	—	±2	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A07	EGN	Gain Error	—	—	±1	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A10	—	Monotonicity	—	Note 3	—	—	AVSS ≤ VAIN ≤ VREF+
A20*	VREF	Reference voltage (VREF+ - VREF-)	4.096	—	VDD +0.3V	V	Absolute minimum electrical spec to ensure 10-bit accuracy.
A21*	VREF+	Reference V High (AVDD or VREF+)	VREF-	—	AVDD	V	Min. resolution for A/D is 4.1 mV
A22*	VREF-	Reference V Low (AVSS or VREF-)	AVSS	—	VREF+	V	Min. resolution for A/D is 4.1 mV
A25*	VAIN	Analog input voltage	VREFL	—	VREFH	V	
A30*	ZAIN	Recommended impedance of analog voltage source	—	—	2.5	kΩ	
A50*	IREF	VREF input current **(Note 2)**	—	—	10	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 11.0. During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from External VREF+, or VREF-, or AVSS, or AVDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

© 1999-2013 Microchip Technology Inc.

FIGURE 16-10: TYPICAL IDD VS. FOSC OVER VDD (ER MODE)

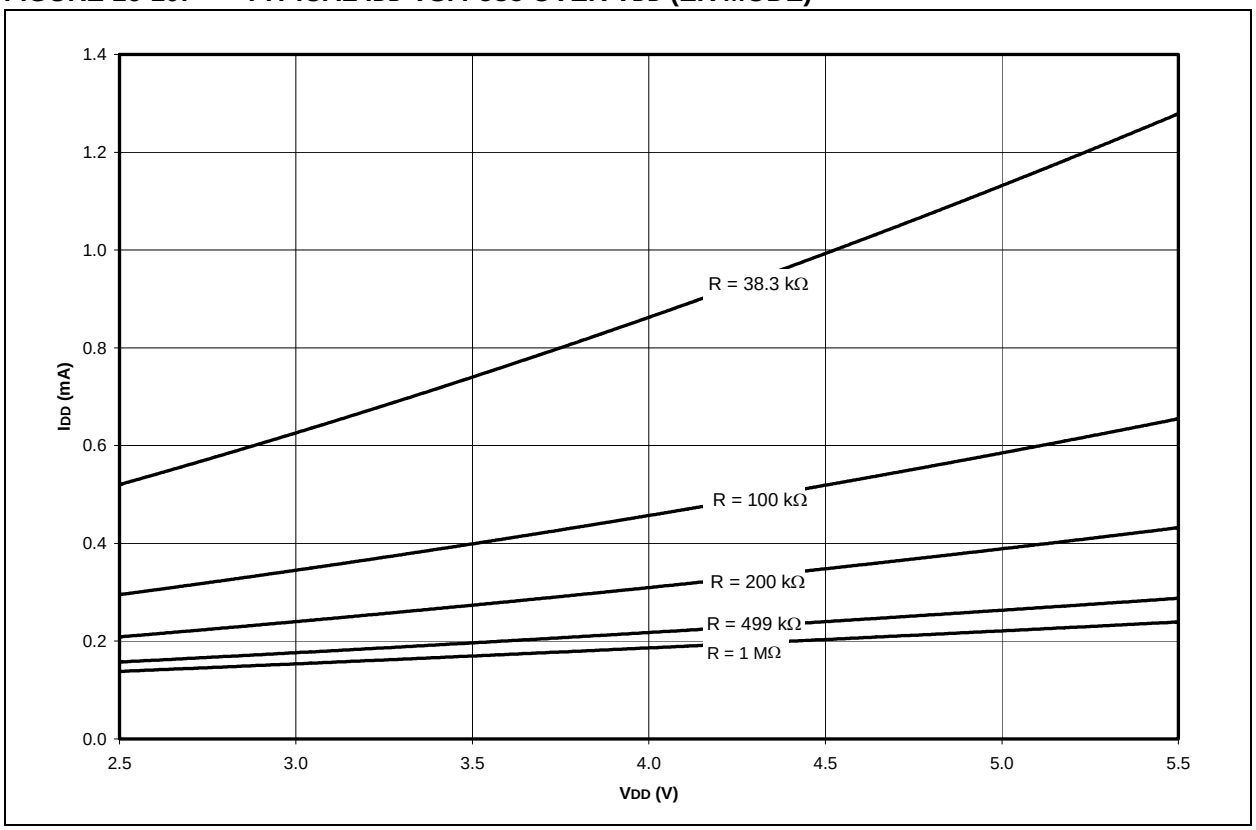
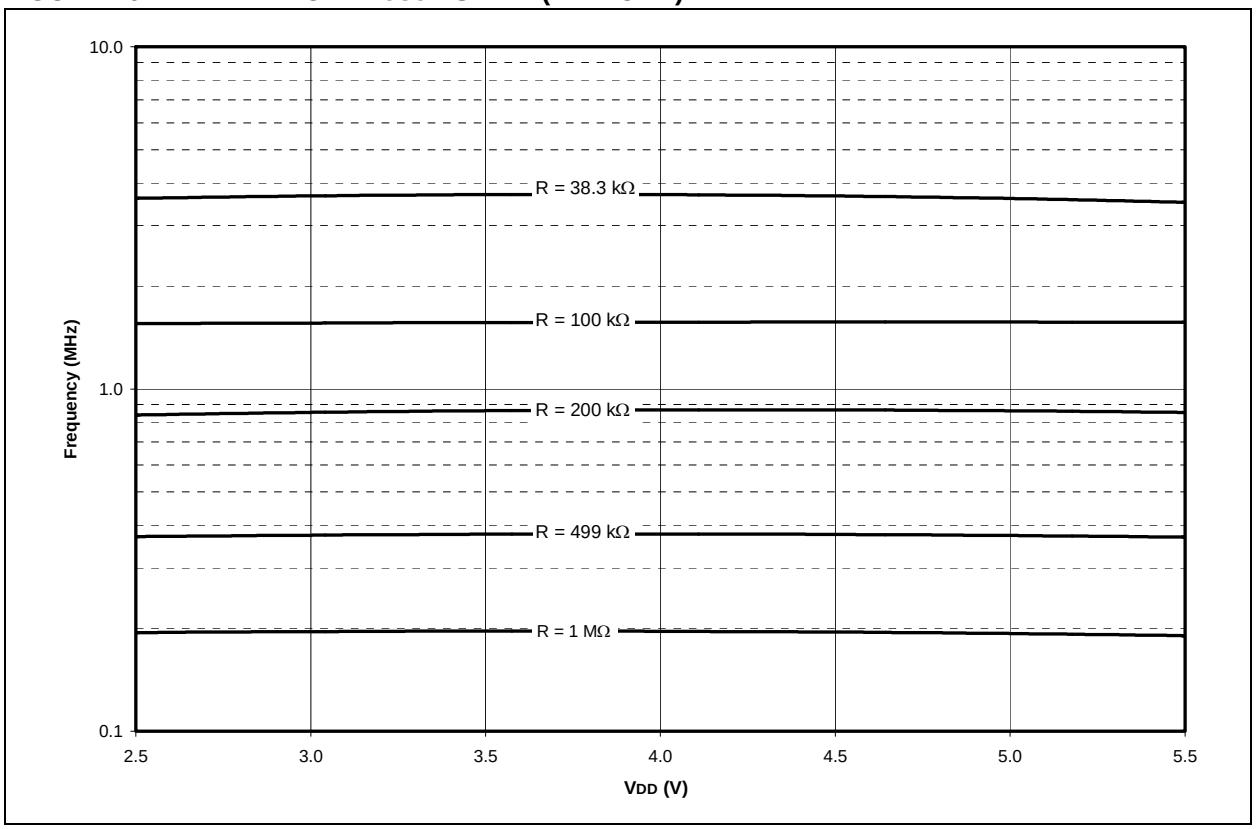


FIGURE 16-11: TYPICAL FOSC VS. VDD (ER MODE)



© 1999-2013 Microchip Technology Inc.

FIGURE 16-26: TYPICAL AND MAXIMUM ΔIBOR VS. VDD (-40°C TO +125°C) (VBOR = 4.5V)

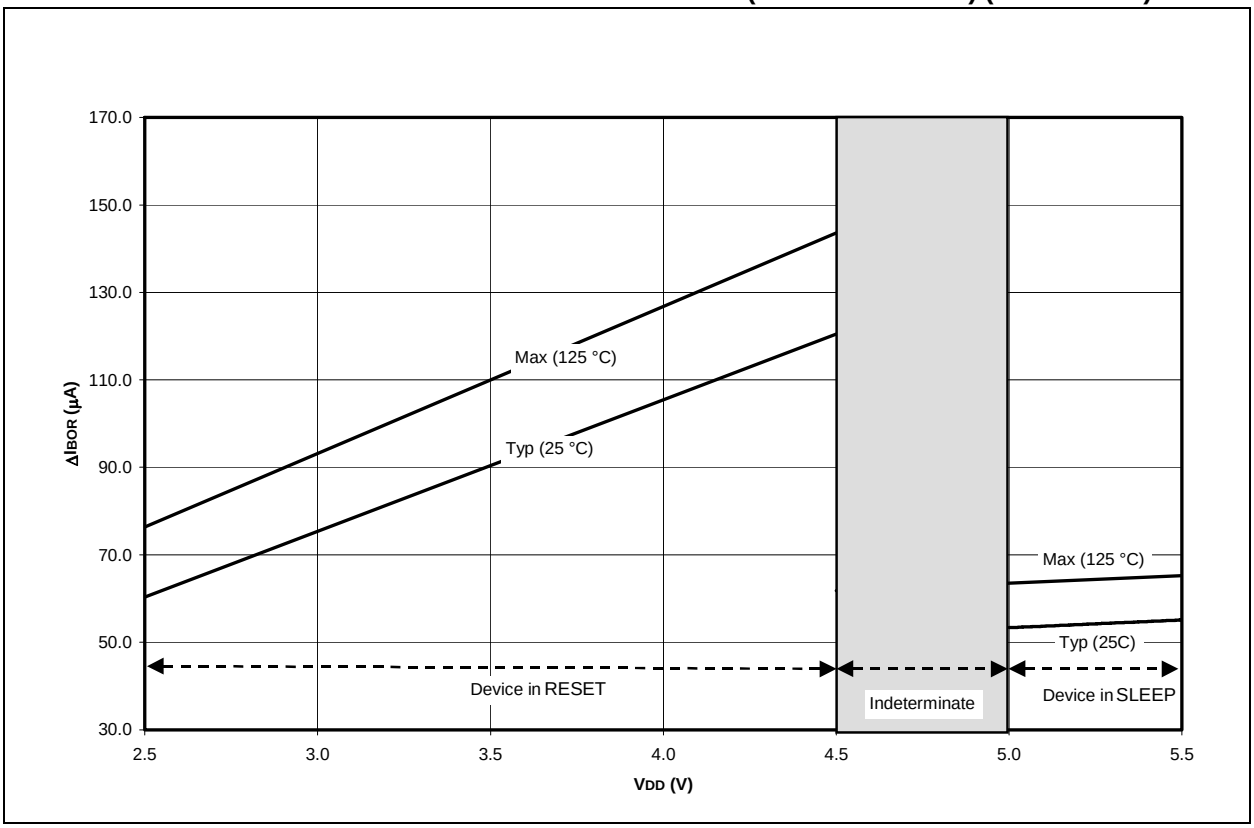


FIGURE 16-27: VOL VS. IOL (-40°C TO +125°C, VDD = 3.0V)

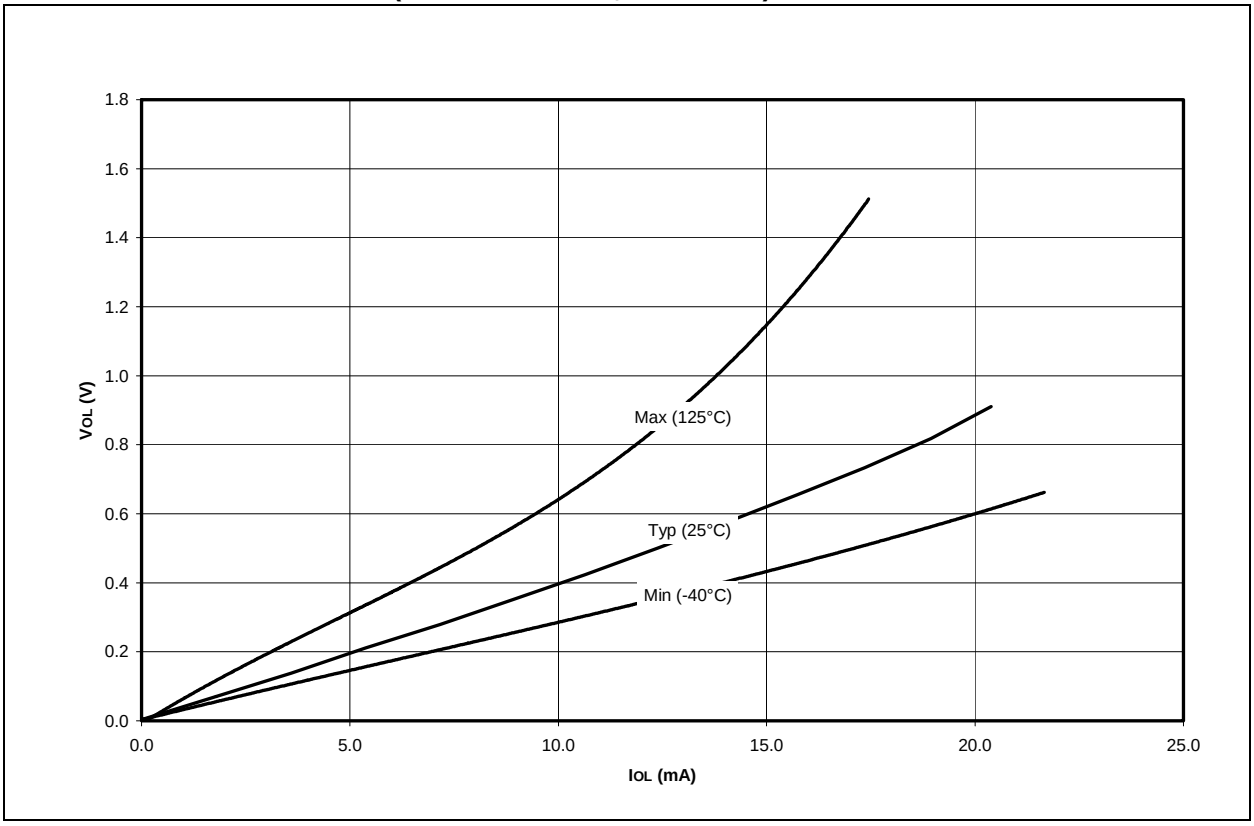


FIGURE 16-30: VOH VS. IOH (-40°C TO +125°C, VDD = 5.0V)

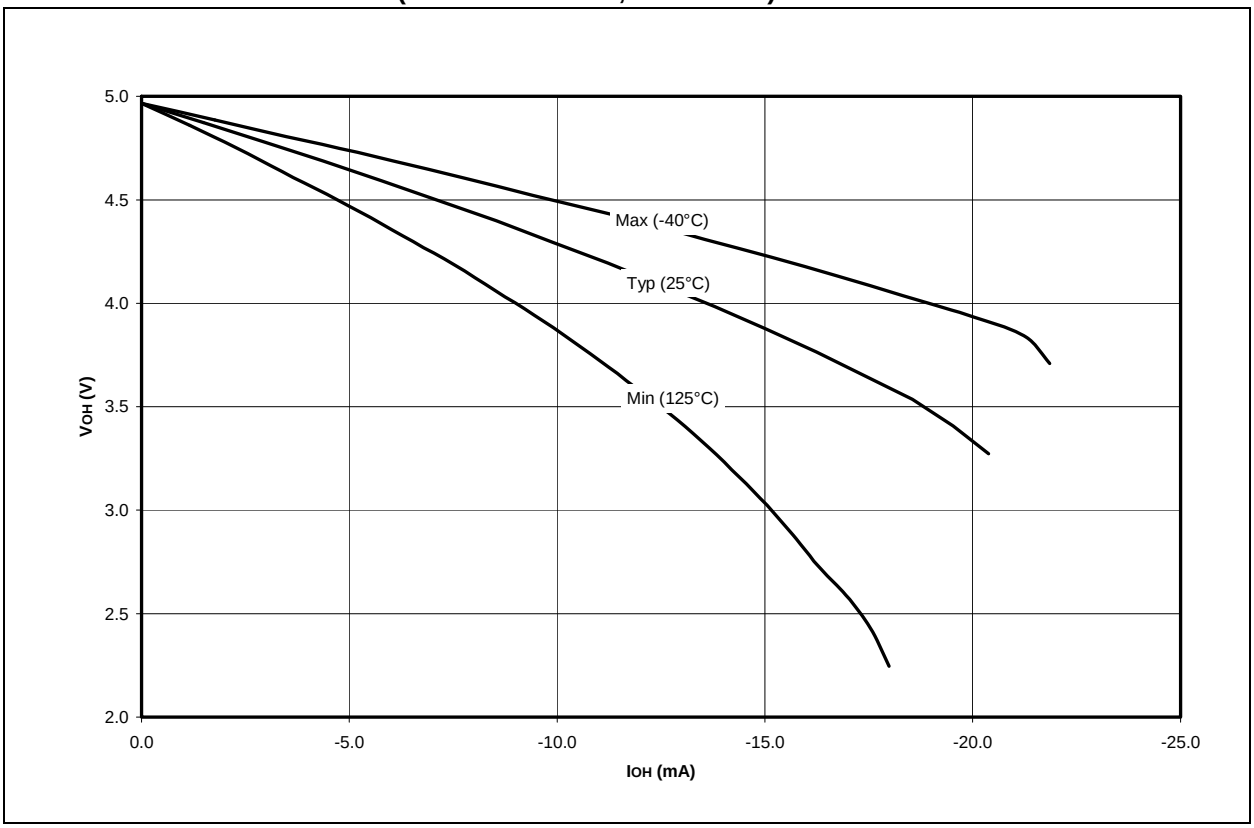
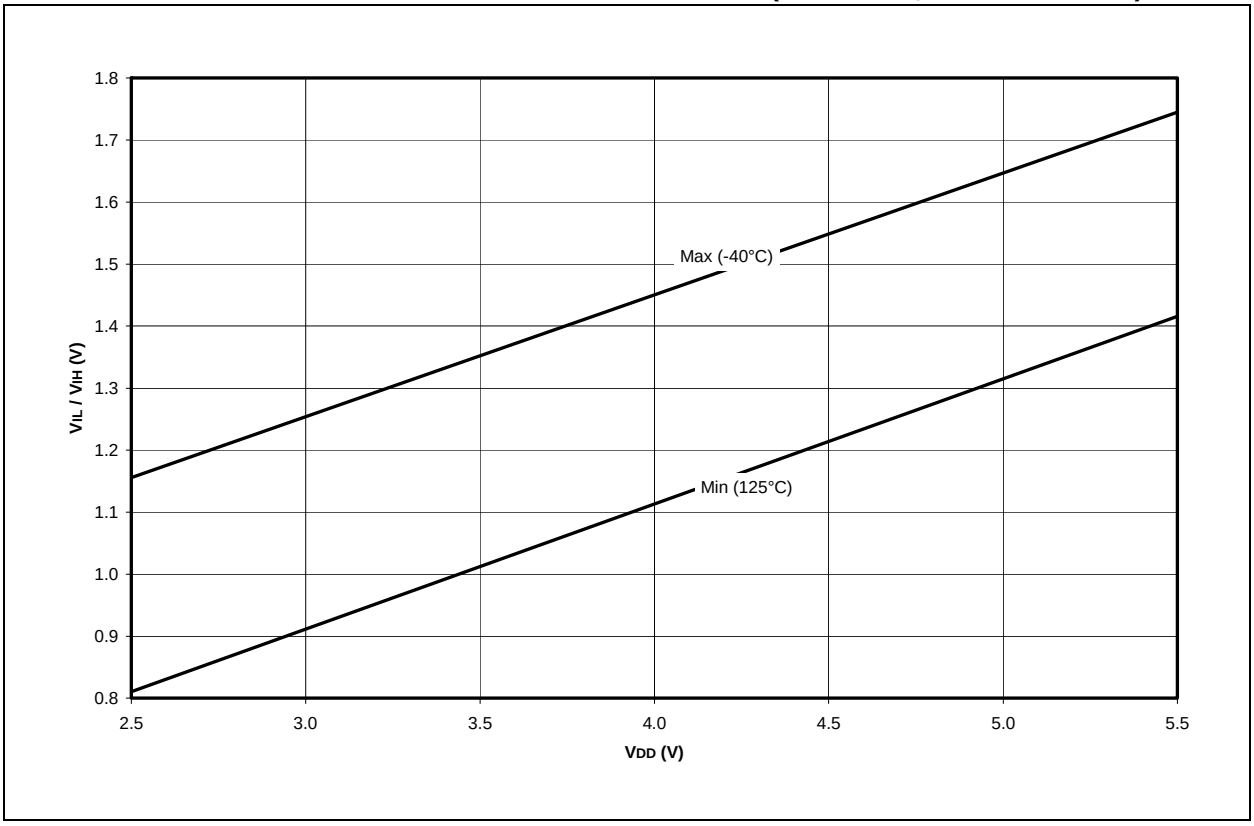
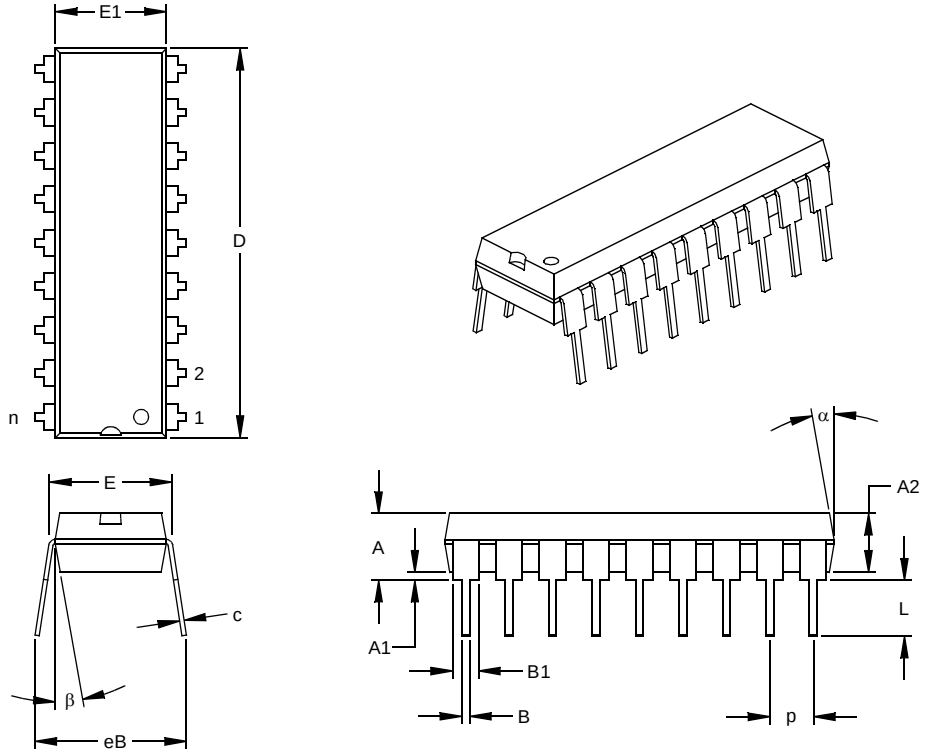


FIGURE 16-31: MINIMUM AND MAXIMUM VIH/VIL VS. VDD (TTL INPUT,-40°C TO +125°C)



17.2 18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

INDEX

© 1999-2013 Microchip Technology Inc.