Microchip Technology - PIC16LC770-E/SO Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc770-e-so

2.2.2.6 PIE2 REGISTER

This register contains the individual enable bits for the SSP bus collision and low voltage detect interrupts.

REGISTER 2-6: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (PIE2: 8Dh)

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
LVDIE	—	—	—	BCLIE	—	—	—
bit 7							bit 0

bit 7 **LVDIE:** Low Voltage Detect Interrupt Enable bit
1 = LVD Interrupt is enabled
0 = LVD Interrupt is disabled

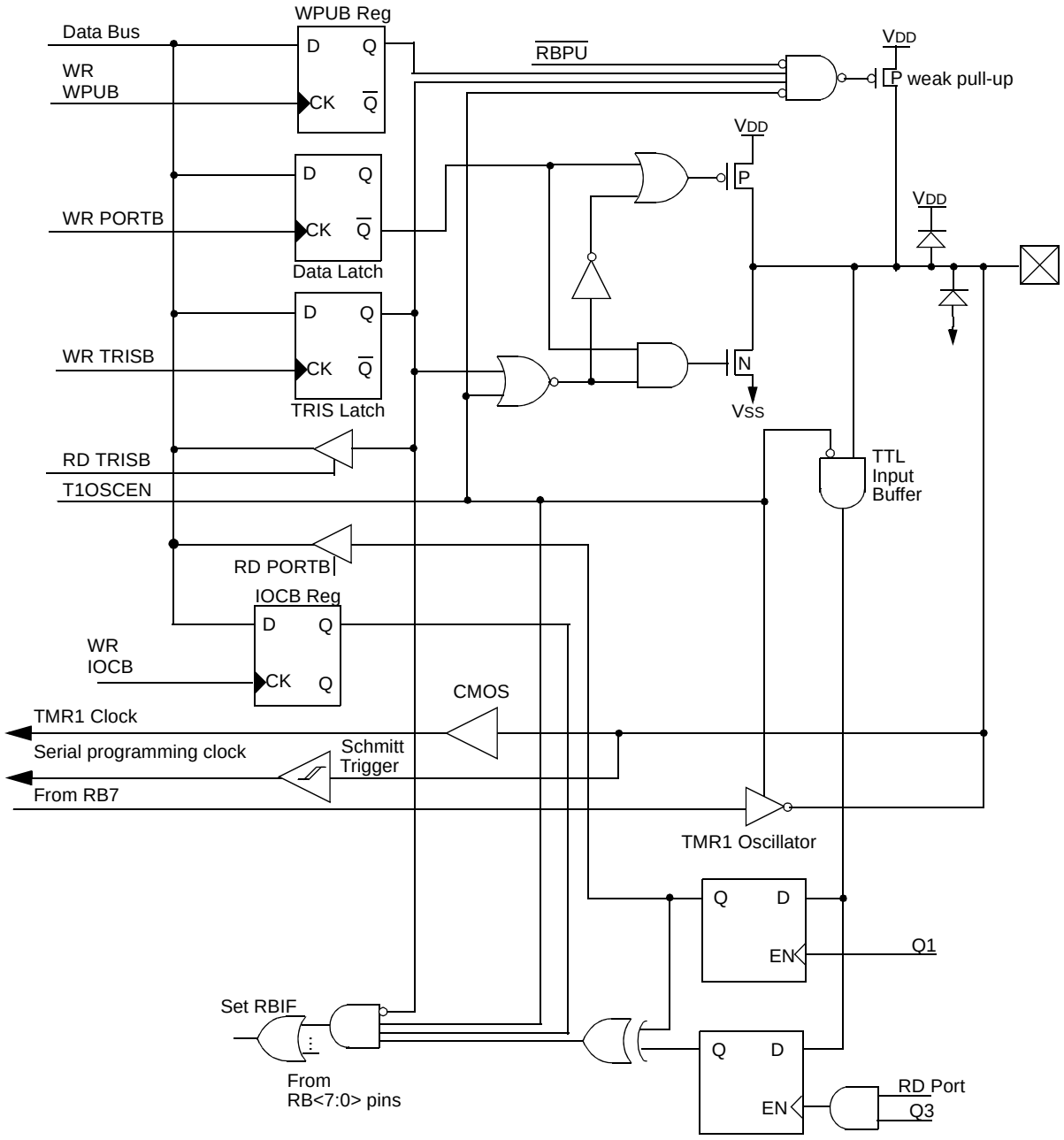
bit 6-4 **Unimplemented:** Read as '0'

bit 3 **BCLIE:** Bus Collision Interrupt Enable bit
1 = Bus Collision interrupt is enabled
0 = Bus Collision interrupt is disabled

bit 2-0 **Unimplemented:** Read as '0'

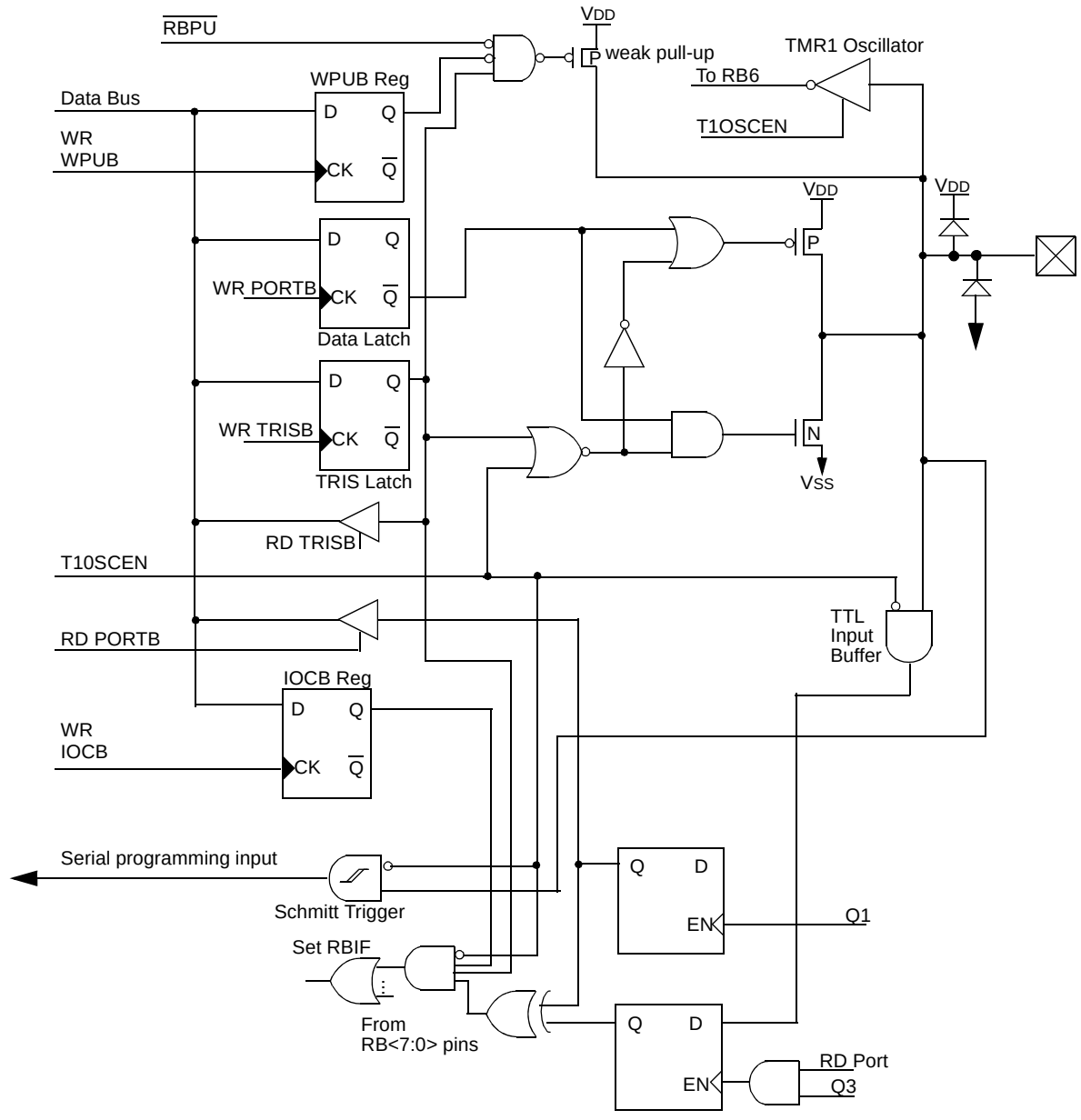
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

FIGURE 3-9: BLOCK DIAGRAM OF RB6/T1OSO/T1CKI/P1C



Note: The TMR1 oscillator enable (T1OSCEN = 1) overrides the RB6 I/O port and P1C functions.

FIGURE 3-10: BLOCK DIAGRAM OF THE RB7/T1OSI/P1D



Note: The TMR1 oscillator enable (T1OSCEN = 1) overrides the RB7 I/O port and P1D functions.

TABLE 4-1: PROGRAM MEMORY READ REGISTER SUMMARY

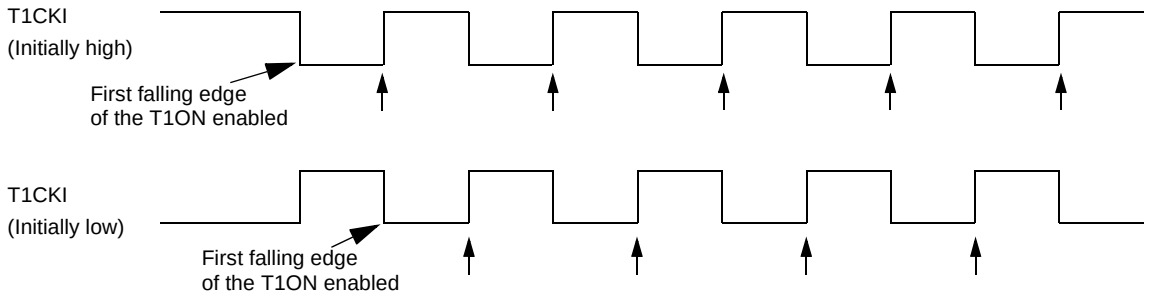
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--xx xxxx	--uu uuuu
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	xxxx xxxx	uuuu uuuu
10Fh	PMADRH	—	—	—	—	PMA11	PMA10	PMA9	PMA8	---- xxxx	---- uuuu
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Program Memory Read.

6.1.1 TIMER1 COUNTER OPERATION

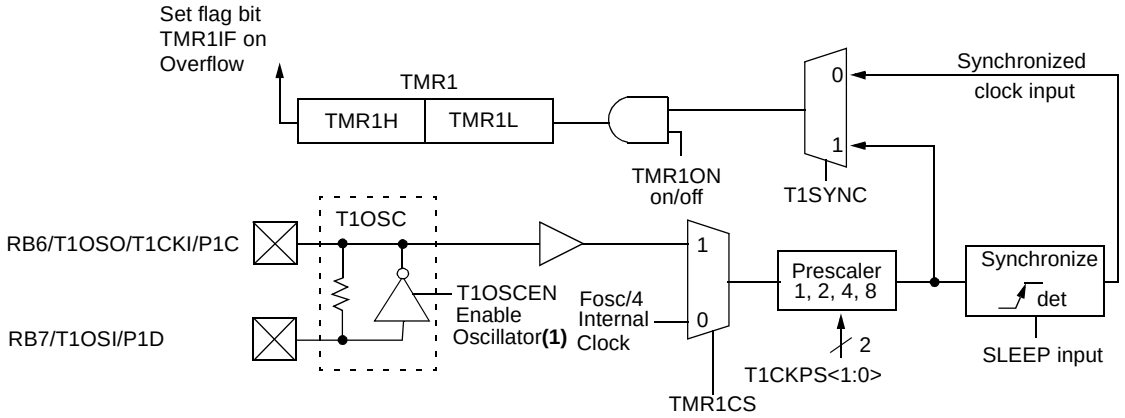
In this mode, Timer1 is being incremented via an external source. Increments occur on a rising edge. After Timer1 is enabled in Counter mode, the module must first have a falling edge before the counter begins to increment.

FIGURE 6-1: TIMER1 INCREMENTING EDGE



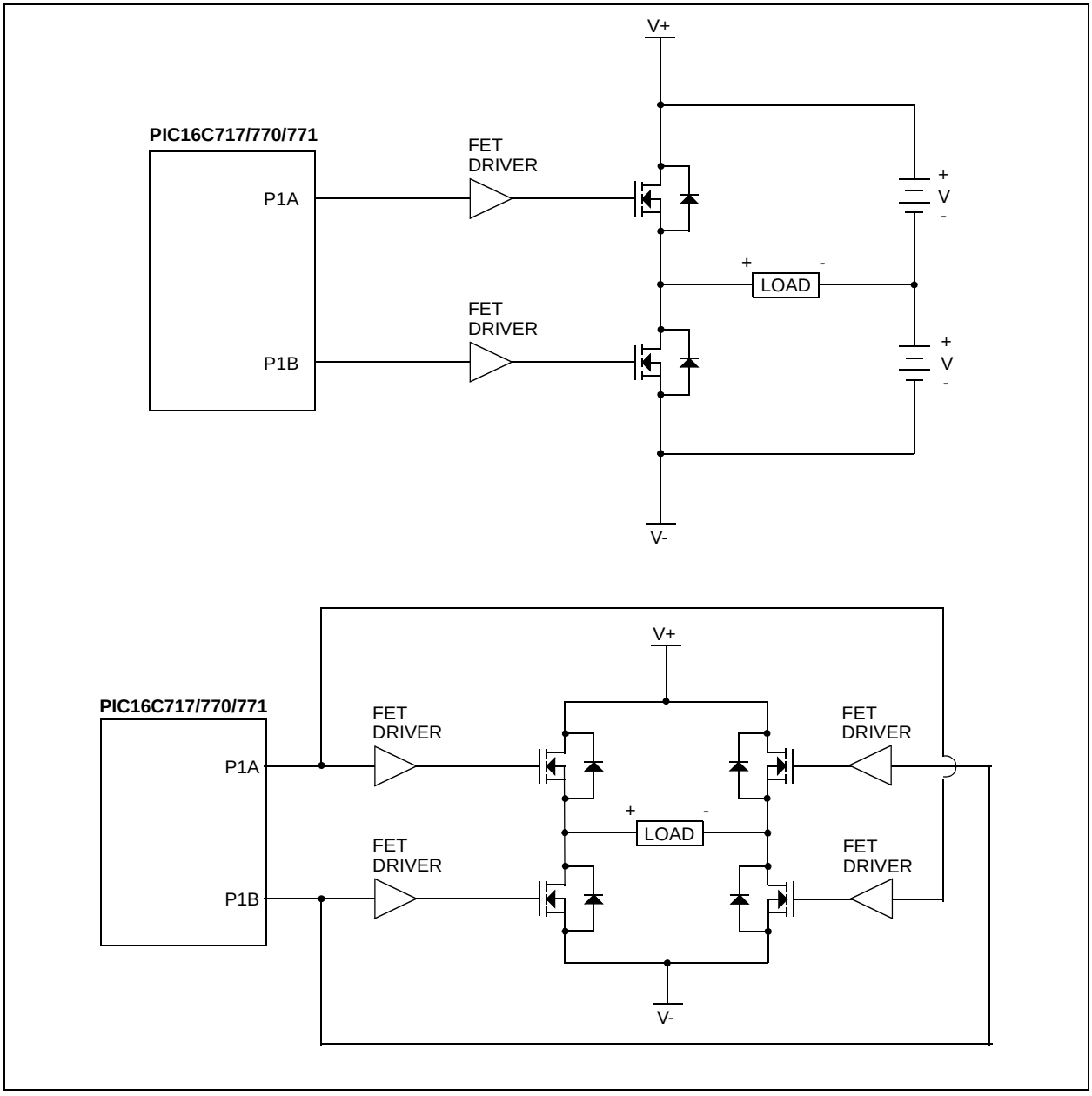
Note: Arrows indicate counter increments.

FIGURE 6-2: TIMER1 BLOCK DIAGRAM



Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

FIGURE 8-7: EXAMPLE OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



9.2.2.4 SLAVE TRANSMISSION

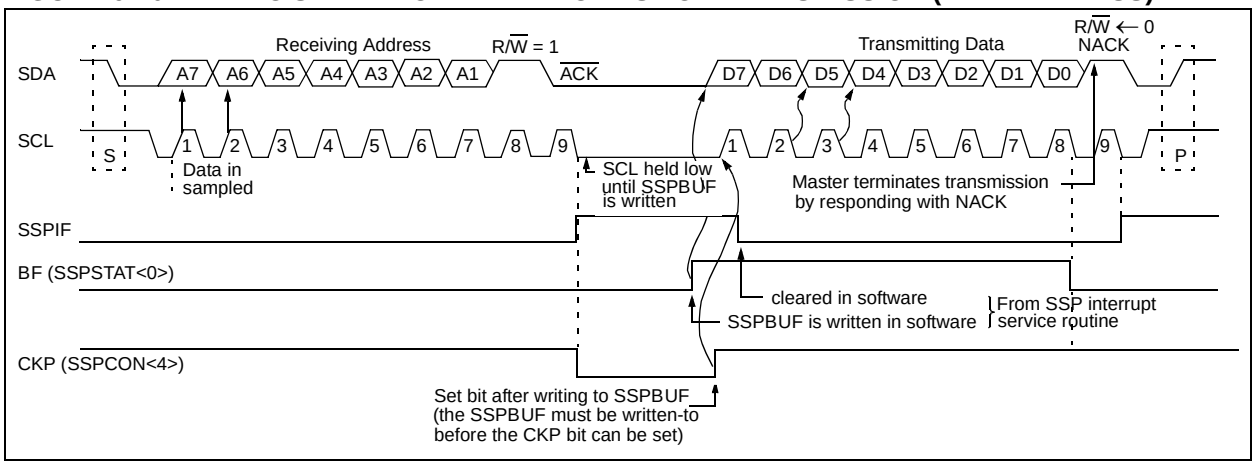
When the R/$\overline{W}$ bit of the incoming address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register on the falling edge of the eighth SCL pulse. The $\overline{ACK}$ pulse will be sent on the ninth bit, and the SCL pin is held low. The slave module automatically stretches the clock by holding the SCL line low so that the master will be unable to assert another clock pulse until the slave is finished preparing the transmit data. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. The CKP bit (SSPCON<4>) must then be set to release the SCL pin from the forced low condition. The eight data bits are shifted out on the falling edges of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 9-10).

The $\overline{ACK}$ or NACK signal from the master-receiver is latched on the rising edge of the ninth SCL input pulse. The master-receiver terminates slave transmission by sending a NACK. If the SDA line is high (NACK), then the data transfer is complete. When the NACK is latched by the slave, the slave logic is RESET which also resets the R/$\overline{W}$ bit to '0'. The slave module then monitors for another occurrence of the START bit. The slave firmware knows not to load another byte into the SSPBUF register by sensing that the buffer is empty (BF = 0) and the R/$\overline{W}$ bit has gone low. If the SDA line is low ($\overline{ACK}$), the R/$\overline{W}$ bit remains high indicating that the next transmit data must be loaded into the SSPBUF register.

An MSSP interrupt (SSPIF flag) is generated for each data transfer byte on the falling edge of the ninth clock pulse. The SSPIF flag bit must be cleared in software. The SSPSTAT register is used to determine the status of the byte transfer.

For more information about the I^{2}C Slave mode, refer to Application Note AN734, "*Using the PIC® SSP for Slave I^{2}C™ Communication*".

FIGURE 9-10: I^{2}C SLAVE MODE WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



REGISTER 11-2: A/D CONTROL REGISTER 1 (ADCON1: 9Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG2	VCFG1	VCFG0	Reserved	Reserved	Reserved	Reserved
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6-4 **VCFG<2:0>:** Voltage Reference Configuration bits

	A/D V_{REF+}	A/D V_{REF-}
000	AV_{DD}(1)	AV_{SS}(2)
001	External V_{REF+}	External V_{REF-}
010	Internal VRH	Internal VRL
011	External V_{REF+}	AV_{SS}(2)
100	Internal VRH	AV_{SS}(2)
101	AV_{DD}(1)	External V_{REF-}
110	AV_{DD}(1)	Internal VRL
111	Internal VRL	AV_{SS}

bit 3-0 **Reserved:** Do not use.

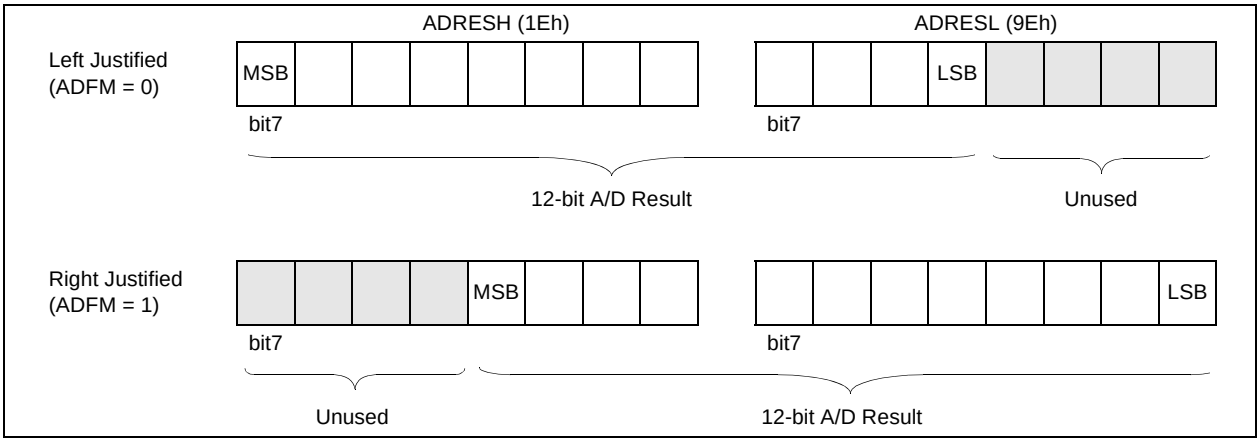
Note 1: This parameter is V_{DD} for the PIC16C717.
2: This parameter is V_{SS} for the PIC16C717.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The value that is in the ADRESH and ADRESL registers are not modified for a Power-on Reset. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

The A/D conversion results can be left justified (ADFM bit cleared), or right justified (ADFM bit set). Figure 11-1 through Figure 11-2 show the A/D result data format of the PIC16C717/770/771.

FIGURE 11-1: PIC16C770/771 12-BIT A/D RESULT FORMATS



13.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 13-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 13-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 13-2 lists the instructions recognized by the MPASM™ assembler.

Figure 13-1 shows the general formats that the instructions can have.

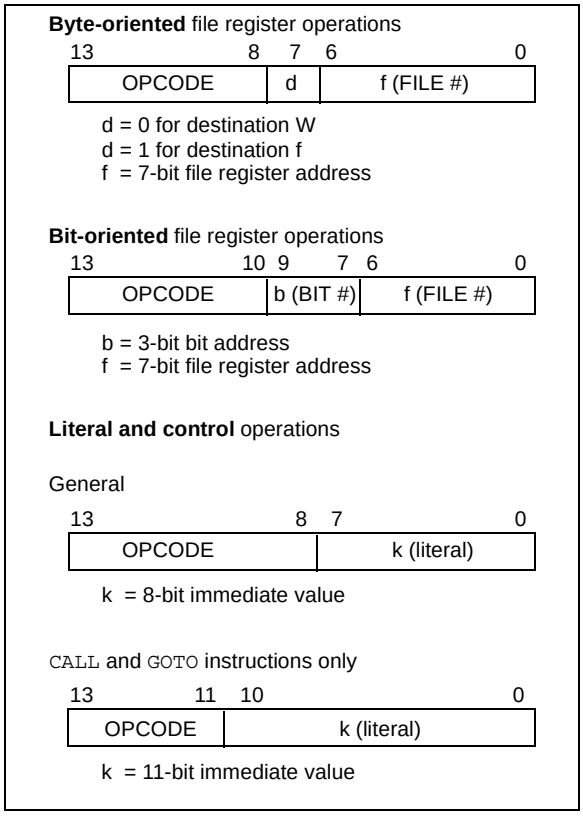
Note: To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\bar{f}) \rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	$k \rightarrow$ PC<10:0> PCLATH<4:3> $\rightarrow$ PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead making it a 2TCY instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead making it a 2TCY instruction.

NOTES:

15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16C717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Base plus Module current					
D021A	IWDT	Watchdog Timer		2	10	µA	VDD = 3V, -40°C to 125°C
D021	IWDT	Watchdog Timer		5	20	µA	VDD = 4V, -40°C to 125°C
D021	IWDT	Watchdog Timer		5	20	µA	VDD = 4V, -40°C to 125°C
D025	IT1OSC	Timer1 Oscillator		3	9	µA	VDD = 3V, -40°C to 125°C
D025	IT1OSC	Timer1 Oscillator		4	12	µA	VDD = 4V, -40°C to 125°C
D025	IT1OSC	Timer1 Oscillator		4	12	µA	VDD = 4V, -40°C to 125°C
D026*	IAD	ADC Converter		300		µA	VDD = 5.5V, A/D on, not converting
D026*	IAD	ADC Converter		300		µA	VDD = 5.5V, A/D on, not converting
D027	IPLVD	Programmable Low Voltage Detect		55	125	µA	VDD = 4V, -40°C to 85°C
D027A					150		VDD = 4V, -40°C to 125°C
D027	IPLVD	Programmable Low Voltage Detect		55	125	µA	VDD = 4V, -40°C to 85°C
D027A					150		VDD = 4V, -40°C to 125°C
D028	IPBOR	Programmable Brown-out Reset		55	125	µA	VDD = 5V, -40°C to 85°C
D028A					150		VDD = 5V, -40°C to 125°C
D028	IPBOR	Programmable Brown-out Reset		55	125	µA	VDD = 5V, -40°C to 85°C
D028A					150		VDD = 5V, -40°C to 125°C
D029	IVRH	Voltage reference High		200	750	µA	VDD = 5V, -40°C to 85°C
D029A					1.0	mA	VDD = 5V, -40°C to 125°C
D029	IVRH	Voltage reference High		200	750	µA	VDD = 5V, -40°C to 85°C
D029A					1.0	mA	VDD = 5V, -40°C to 125°C
D030	IVRL	Voltage reference Low		200	750	µA	VDD = 4V, -40°C to 85°C
D030A					1.0	mA	VDD = 4V, -40°C to 125°C
D030	IVRL	Voltage reference Low		200	750	µA	VDD = 4V, -40°C to 85°C
D030A					1.0	mA	VDD = 4V, -40°C to 125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.2 DC Characteristics: PIC16C717/770/771 & PIC16LC717/770/771 (Commercial, Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in Section 15.1 and Section 15.2.				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range
D030A			VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	For entire VDD range
D032		$\overline{MCLR}$	VSS	—	0.2VDD	V	
D033		OSC1 (in XT, HS, LP and EC)	VSS	—	0.3VDD	V	
		Input High Voltage					
	VIH	I/O ports		—			
		with TTL buffer					
D040			2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25VDD + 0.8V)	—	VDD	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS, LP and EC)	0.7VDD	—	VDD	V	
D070	IPURB	PORTB weak pull-up current per pin	50	250	400	µA	VDD = 5V, VPIN = VSS
		Input Leakage Current (1,2)					
D060	IIL	I/O ports (with digital functions)	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A	IIL	I/O ports (with analog functions)	—	—	±100	nA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		RA5/$\overline{MCLR}$/VPP	—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS, LP and EC osc configuration
		Output Low Voltage					
D080	VOL	I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(2)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D150*	VOD	**Open Drain High Voltage**	—	—	10.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins*					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC	—	—	50	pF	
D102	CB	mode) SCL, SDA in I2C mode	—	—	400	pF	
	CVRH	VRH pin	—	—	200	pF	VRH output enabled
	CVRL	VRL pin	—	—	200	pF	VRL output enabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

TABLE 15-6: ENHANCED CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

Param. No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**717/770/771	10	—	—	ns	
				PIC16**LC**717/770/771	20	—	—	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**717/770/771	10	—	—	ns	
				PIC16**LC**717/770/771	20	—	—	ns	
52*	TccP	CCP1 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)
53*	TccR	CCP1 output fall time		PIC16**C**717/770/771	—	10	25	ns	
				PIC16**LC**717/770/771	—	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16**C**717/770/771	—	10	25	ns	
				PIC16**LC**717/770/771	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.4.3 PROGRAMMABLE BROWN-OUT RESET MODULE (PBOR)

TABLE 15-9: DC CHARACTERISTICS: PBOR

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC Characteristics Section 15.1.					
Param. No.	**Characteristic**		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D005	BOR Voltage	BORV<1:0> = 11	VBOR	2.5	2.58	2.66	V	
		BORV<1:0> = 10		2.7	2.78	2.86		
		BORV<1:0> = 01		4.2	4.33	4.46		
		BORV<1:0> = 00		4.5	4.64	4.78		

15.4.4 VREF MODULE

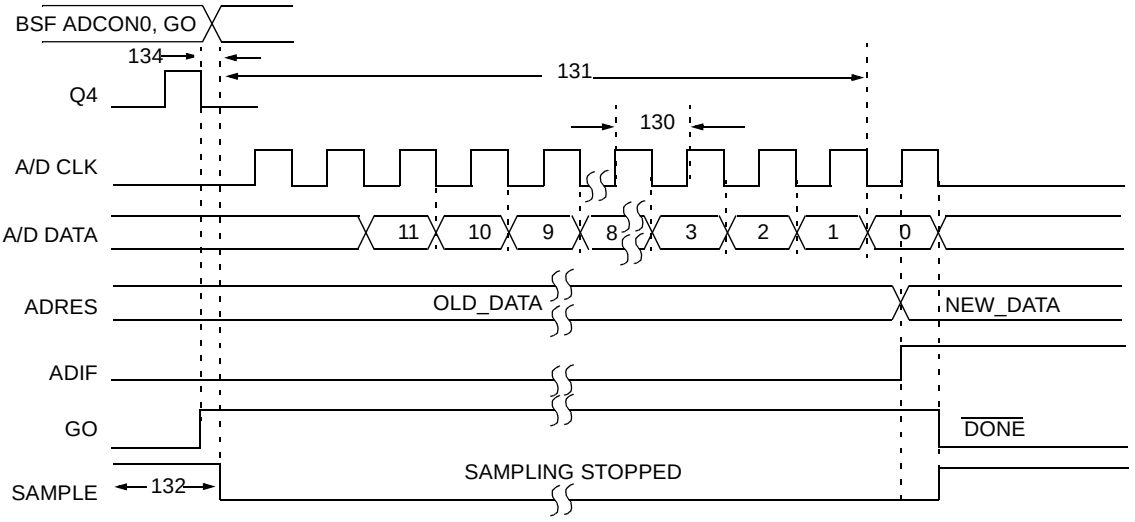
TABLE 15-10: DC CHARACTERISTICS: VREF

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC Characteristics Section 15.1.					
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
D400	VRL	Output Voltage	2.0	2.048	2.1	V	VDD ≥ 2.7V, -40°C ≤ TA ≤ +85°C	
	VRH		4.0	4.096	4.2	V	VDD ≥ 4.5V, -40°C ≤ TA ≤ +85°C	
D400A	VRL	Output Voltage	1.9	2.048	2.2	V	VDD ≥ 2.7V, -40°C ≤ TA ≤ +125°C	
	VRH		4.0	4.096	4.3	V	VDD ≥ 4.5V, -40°C ≤ TA ≤ +125°C	
D404*	IVREFSO	External Load Source	—	—	5	mA		
D405*	IVREFSI	External Load Sink	—	—	-5	mA		
*	CL	External Capacitor Load	—	—	200	pF		
D406*	ΔVout/ ΔIout	VRH Load Regulation	—	0.6	1	mV/mA	VDD ≥ 5V	ISOURCE = 0 mA to 5 mA
			—	1	4			ISINK = 0 mA to 5 mA
		VRL Load Regulation	—	0.6	1		VDD ≥ 3V	ISOURCE = 0 mA to 5 mA
			—	2	4			ISINK = 0 mA to 5 mA

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-15: PIC16C770/771 AND PIC16LC770/771 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-13: PIC16C770/771 AND PIC16LC770/771 A/D CONVERSION REQUIREMENT (SLEEP MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D Internal RC oscillator period	3.0	6.0	9.0	µs	ADCS<1:0> = 11 (RC mode) At VDD= 3.0V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	13TAD	—	—	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2 + TCY	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

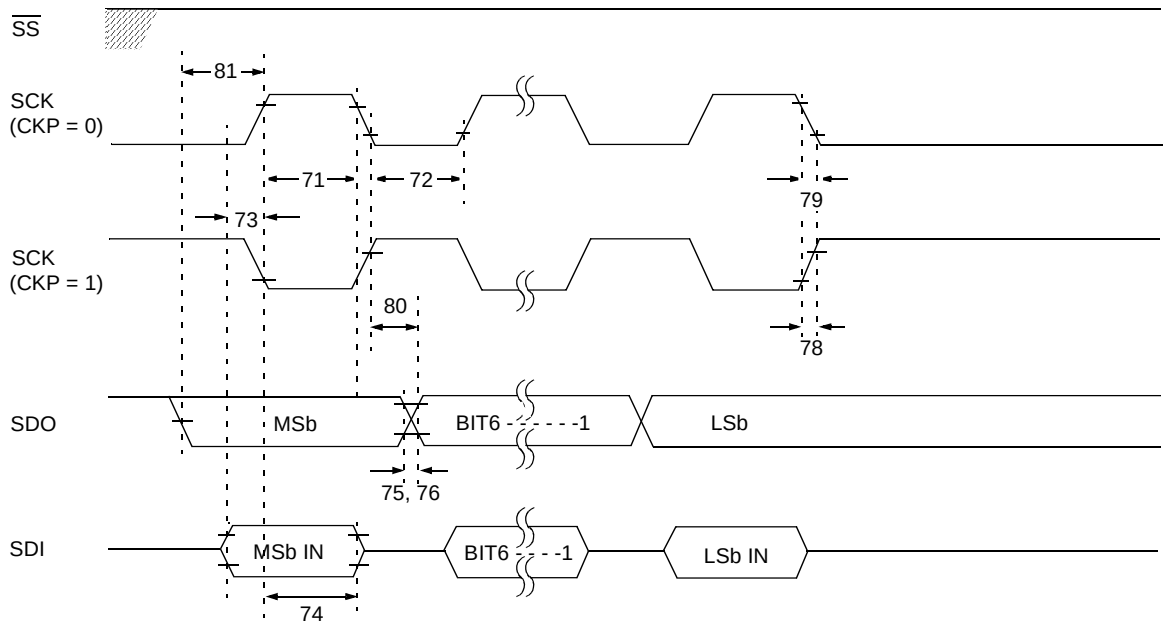
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

FIGURE 15-19: SPI MASTER MODE TIMING (CKE = 1)



Note: Refer to Figure 15-4 for load conditions.

TABLE 15-18: SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
71*	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A*			Single Byte	40	—	—	ns	**Note 1**
72*	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A*			Single Byte	40	—	—	ns	**Note 1**
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A*	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	**Note 1**
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75*	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
76*	TdoF	SDO data output fall time		—	10	25	ns	
78*	TscR	SCK output rise time (Master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX		—	100	ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge		TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

FIGURE 16-4: TYPICAL IDD VS. FOSC OVER VDD (XT MODE)

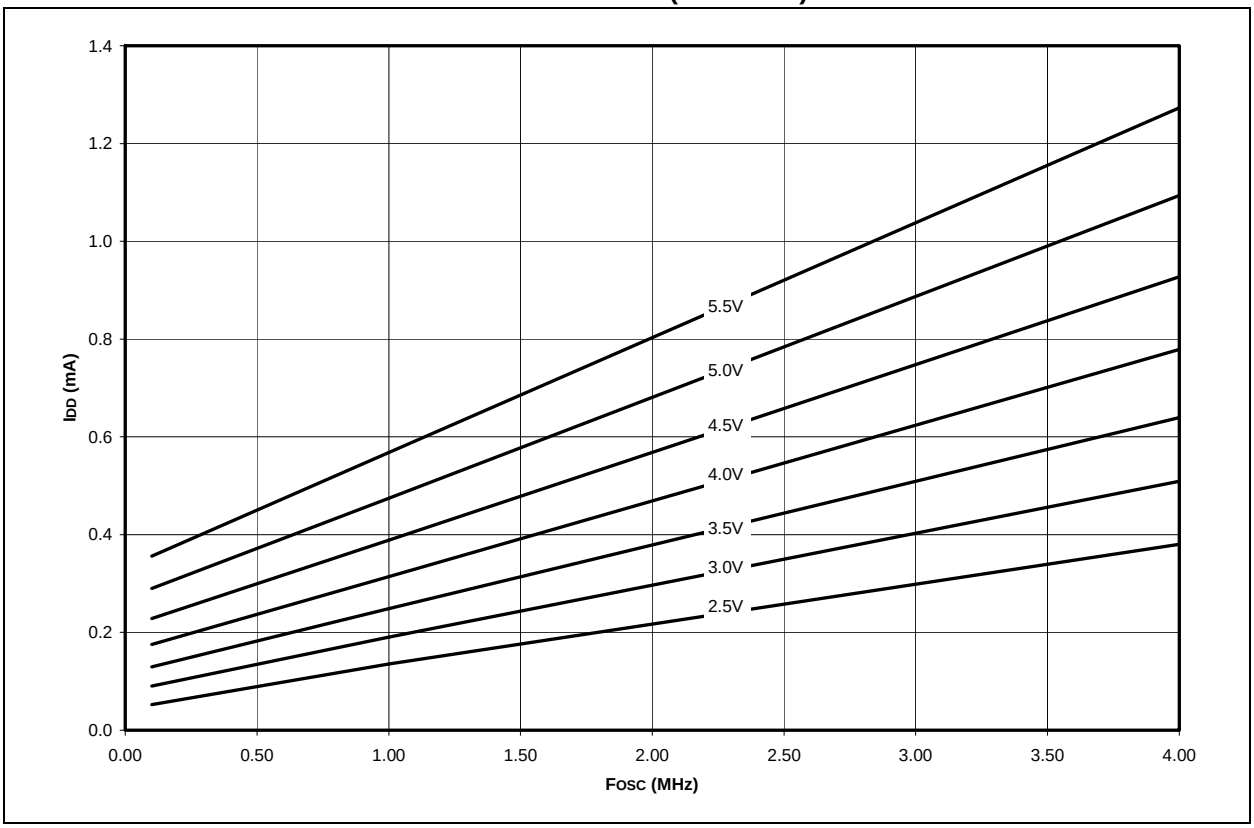


FIGURE 16-5: MAXIMUM IDD VS. FOSC OVER VDD (LP MODE)

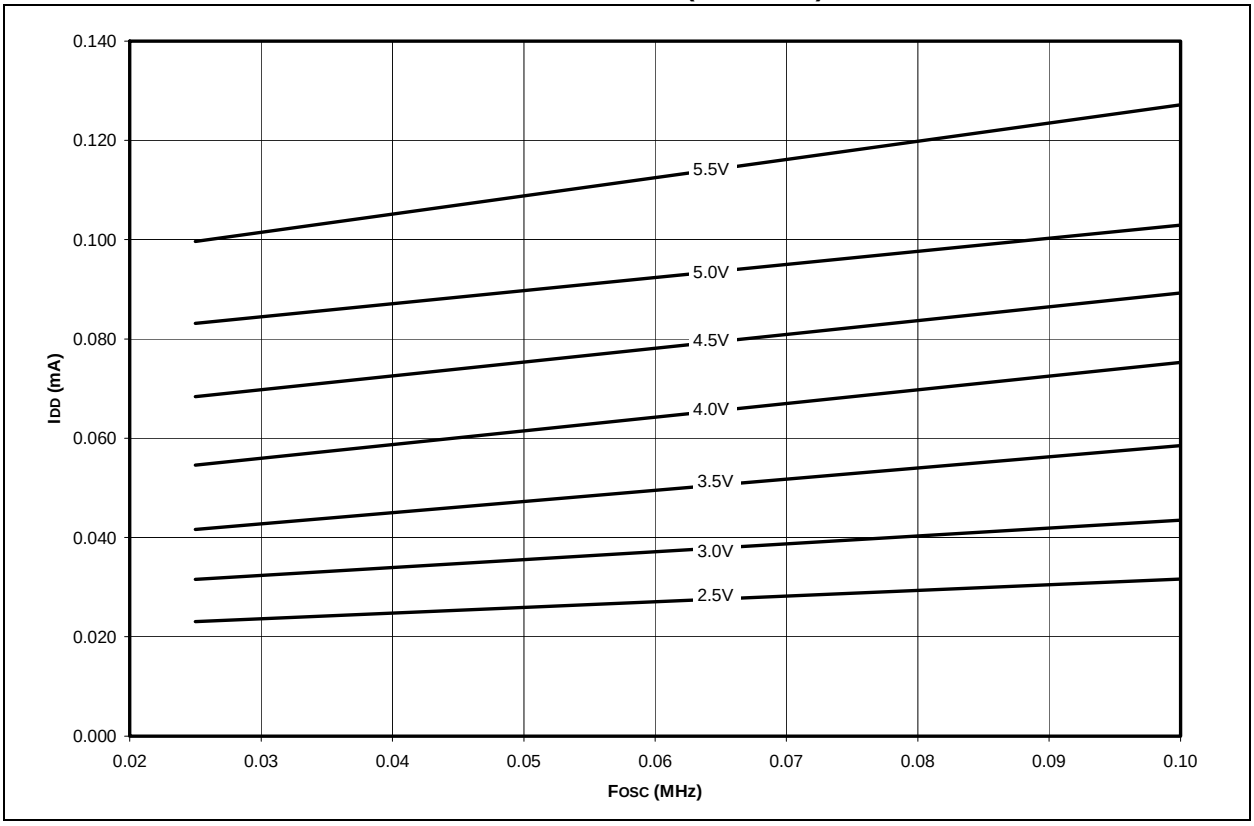


FIGURE 16-32: MINIMUM AND MAXIMUM VIH/VIL VS. VDD (ST INPUT,-40°C TO +125°C)

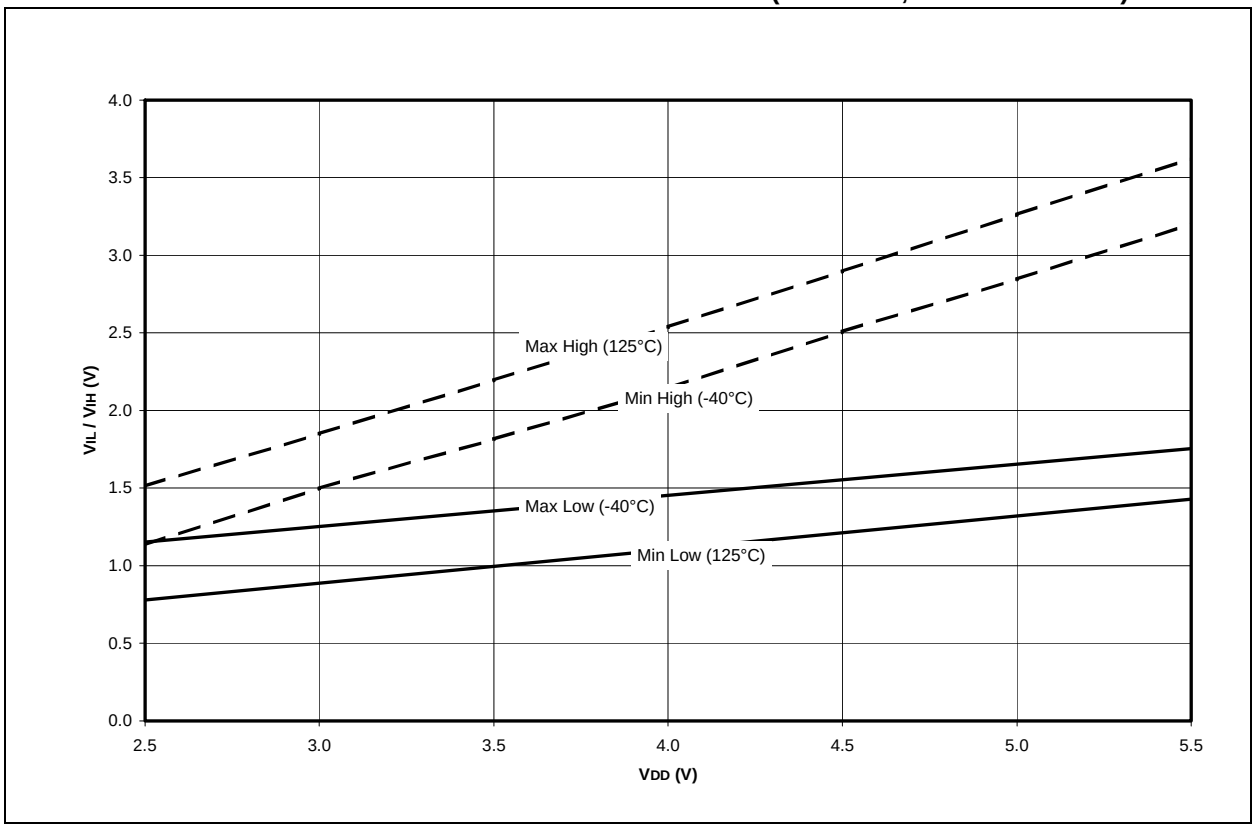
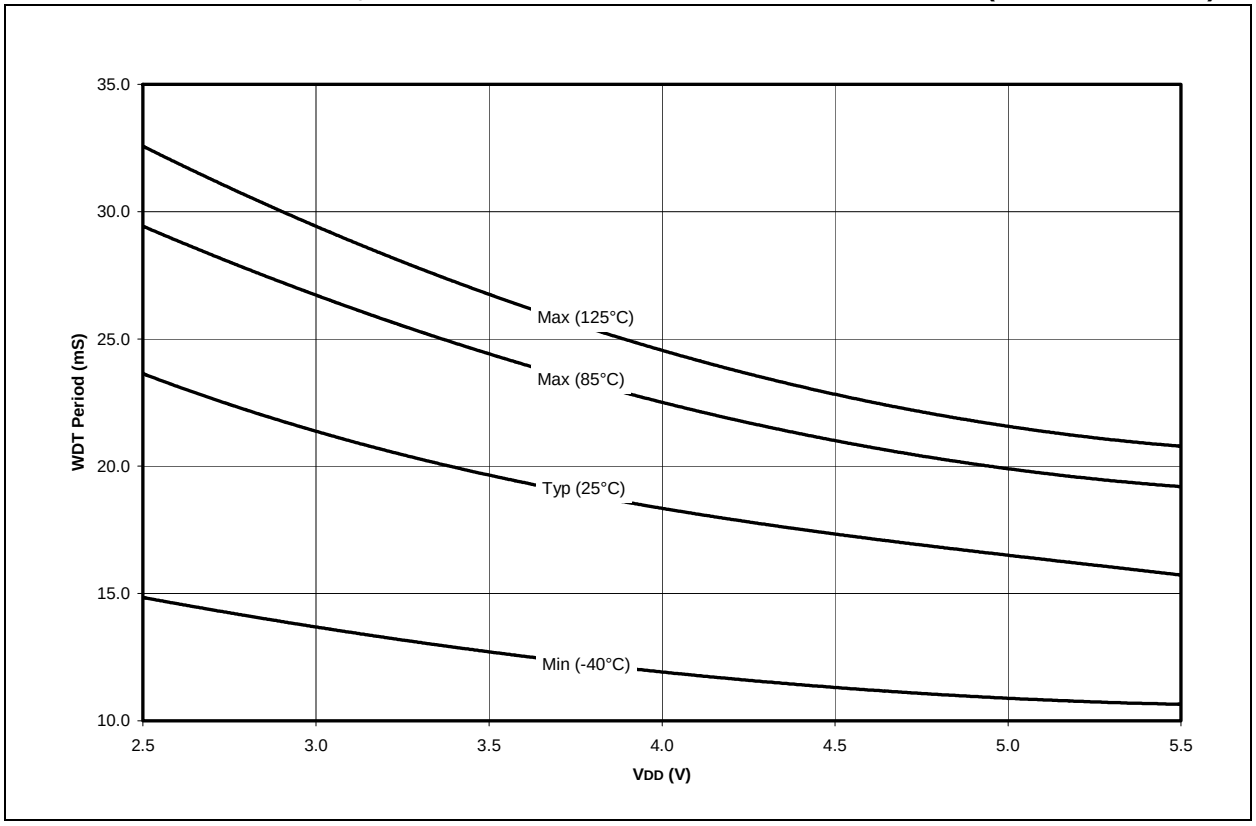


FIGURE 16-33: TYPICAL, MINIMUM AND MAXIMUM WDT PERIOD VS. VDD (-40°C TO +125°C)



APPENDIX B: DEVICE DIFFERENCES

The differences between the devices in this data sheet are listed in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Difference	PIC16C717	PIC16C770	PIC16C771
Program Memory	2K	2K	4K
A/D	6 channels, 10 bits	6 channels, 12 bits	6 channels, 12 bits
Dedicated AV_{DD} and AV_{SS}	Not available	Available	Available
Packages	18-pin PDIP, 18-pin windowed CERDIP, 18-pin SOIC, 20-pin SSOP	20-pin PDIP, 20-pin windowed CERDIP, 20-pin SOIC, 20-pin SSOP	20-pin PDIP, 20-pin windowed CERDIP, 20-pin SOIC, 20-pin SSOP