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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc770-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams



Key Features PICmicro [™] Mid-Range MCU Family Reference Manual, (DS33023)	PIC16C717	PIC16C770	PIC16C771
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR, MCLR, WDT (PWRT, OST)	POR, BOR, MCLR, WDT (PWRT, OST)	POR, BOR, MCLR, WDT (PWRT, OST)
Program Memory (14-bit words)	2K	2K	4K
Data Memory (bytes)	256	256	256
Interrupts	10	10	10
I/O Ports	Ports A,B	Ports A,B	Ports A,B
Timers	3	3	3
Enhanced Capture/Compare/PWM (ECCP) modules	1	1	1
Serial Communications	MSSP	MSSP	MSSP
12-bit Analog-to-Digital Module	-	6 input channels	6 input channels
10-bit Analog-to-Digital Module	6 input channels	-	-
Instruction Set	35 Instructions	35 Instructions	35 Instructions

2.2.2.2 **OPTION_REG REGISTER**

The OPTION_REG register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

OPTION REGISTER (OPTION_REG: 81h, 181h) REGISTER 2-2:

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0
	bit 7				•			bit 0
bit 7	RBPU: PC	ORTB Pull-up	Enable bi	(1)				
	1 = PORT	B weak pull-ı	ups are dis	abled				
	0 = PORT	B weak pull-	ups are ena	abled by the	WPUB register			
bit 6	INTEDG:	nterrupt Edg	e Select bi	t				
	1 = Interru	pt on rising e	edge of RB	0/INT pin				
	0 = Interru	pt on falling	edge of RE	80/INT pin				
bit 5	TOCS: TM	R0 Clock So	urce Selec	t bit				
	1 = Transi	tion on RA4/	T0CKI pin					
	0 = Interna	al instruction	cycle clock	(CLKOUT)				
bit 4	TOSE: TM	R0 Source E	dge Select	t bit				
	1 = Increm	nent on high-	to-low tran	sition on RA	4/T0CKI pin			
	0 = Increm	nent on low-to	o-high tran	sition on RA	4/T0CKI pin			
bit 3	PSA: Pres	caler Assign	ment bit					
	1 = Presca	aler is assign	ed to the V	VDT				
	0 = Presca	aler is assign	ed to the T	ïmer0 modu	le			
bit 2-0	PS<2:0>:	Prescaler Ra	ate Select b	oits				
		Bit Value TI	MR0 Rate	WDT Rate				
		000	1:2	1:1				
		001	1:4	1:2				
		010	1:8	1:4				
		011	1:16	1:8				
		100	1:32	1:10				
		TOT	1:64	1:32				

1:64

1:128

1:64

1:128

1:256

110

111

Note 1: Individual weak pull-up on RB pins can be enabled/disabled from the weak pull-up PORTB Register (WPUB).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented b	oit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.3 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register occur through the PCLATH register.

2.3.1 PROGRAM MEMORY PAGING

PIC16C717/770/771 devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. A return instruction pops a PC address off the stack onto the PC register. Therefore, manipulation of the PCLATH<4:3> bits are not required for the return instructions (which POPs the address from the stack).

2.4 Stack

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

FIGURE 2-4: LOADING OF PC IN DIFFERENT SITUATIONS



Name	Function	Input Type	Output Type	Description
	RB0	TTL	CMOS	Bi-directional I/O ⁽¹⁾
RB0/AN4/INT	AN4	AN		A/D input
	INT	ST		Interrupt input
	RB1	TTL	CMOS	Bi-directional I/O ⁽¹⁾
RB1/AN5/SS	AN5	AN		A/D input
	SS	ST		SSP slave select input
	RB2	TTL	CMOS	Bi-directional I/O ⁽¹⁾
RB2/SCK/SCL	SCK	ST	CMOS	Serial clock I/O for SPI
	SCL	ST	OD	Serial clock I/O for I ² C
	RB3	TTL	CMOS	Bi-directional I/O ⁽¹⁾
RB3/CCP1/P1A	CCP1	ST	CMOS	Capture 1 input/Compare 1 output
	P1A		CMOS	PWM P1A output
	RB4	TTL	CMOS	Bi-directional I/O ⁽¹⁾
RB4/SDI/SDA	SDI	ST		Serial data in for SPI
	SDA	ST	OD	Serial data I/O for I ² C
	RB5	TTL	CMOS	Bi-directional I/O ⁽¹⁾
RB5/SDO/P1B	SDO		CMOS	Serial data out for SPI
	P1B		CMOS	PWM P1B output
	RB6	TTL	CMOS	Bi-directional I/O ⁽¹⁾
	T1OSO		XTAL	Crystal/Resonator
RB6/11050/11CKI/P1C	T1CKI	CMOS		TMR1 clock input
	P1C		CMOS	PWM P1C output
	RB7	TTL	CMOS	Bi-directional I/O ⁽¹⁾
RB7/T1OSI/P1D	T1OSI	XTAL		TMR1 crystal/resonator
	P1D		CMOS	PWM P1D output

TABLE 3-3: PORTB FUNCTIONS

Note 1: Bit programmable pull-ups.

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xx11	uuuu uu11
86h, 186h	TRISB	PORTE	3 Data Dire	ction Reg	gister					1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
95h	WPUB	PORTE	PORTB Weak Pull-up Control							1111 1111	1111 1111
96h	IOCB	PORTE	PORTB Interrupt on Change Control							1111 0000	1111 0000
9Dh	ANSEL	_	_	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	11 1111	11 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 5-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

5.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit TOCS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit TOCS (OPTION_REG<5>). In Counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/TOCKI. The incrementing edge is determined by the Timer0 Source Edge Select bit TOSE (OPTION_REG<4>). Clearing bit TOSE selects the rising edge. Restrictions on the external clock input are discussed in below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization. Additional information on external clock requirements is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

5.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 5-2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS<2:0> bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF 1, MOVWF 1, BSF 1, x...etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.



FIGURE 5-1: TIMER0 BLOCK DIAGRAM

TABLE 8-1: ECCP MODE - TIMER RESOURCE

ECCP Mode	Timer Resource			
Capture	Timer1			
PWM	Timer2			

8.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as:

- · every falling edge
- · every rising edge
- · every 4th rising edge
- every 16th rising edge

An event is selected by control bits CCP1M<3:0> (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

8.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the TRISB<3> bit.

Note:	If the RB3/CCP1/P1A pin is configured as
	an output, a write to the port can cause a
	capture condition.

8.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work.

8.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in Operating mode.

8.1.4 ECCP PRESCALER

There are three prescaler settings, specified by bits CCP1M<3:0>. Whenever the ECCP module is turned off or the ECCP module is not in Capture mode, the prescaler counter is cleared. This means that any RESET will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 8-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 8-1: Changing Between Capture Prescalers

CLRF	CCP1CON	;	Turn ECCP module off
MOVLW	NEW_CAPT_PS	;	Load WREG with the
		;	new prescaler mode
		;	value and ECCP ON
MOVWF	CCP1CON	;	Load CCP1CON with
		;	this value

FIGURE 8-1:

CAPTURE MODE OPERATION BLOCK DIAGRAM



8.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 pin is:

- driven High
- driven Low
- toggle output (High to Low or Low to High)
- remains Unchanged

The action on the pin is based on the value of control bits CCP1M<3:0>. At the same time, interrupt flag bit CCP1IF is set.

Changing the ECCP mode select bits to the clear output on Match mode (CCP1M<3.0> = "1000") presets the CCP1 output latch to the logic 1 level. Changing the ECCP mode select bits to the clear output on Match mode (CCP1M<3:0> = "1001") presets the CCP1 output latch to the logic 0 level.

8.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the appropriate TRISB bit.

Note: Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the port data latch.

8.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the ECCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

9.2.3 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I^2C bus is such that the first byte after the START condition usually determines which device will be the slave addressed by the master. The exception is the general call address, which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I²C protocol. It consists of all 0's with R/W = 0

The general call address is recognized when the General Call Enable bit (GCEN) is set (SSPCON2<7> is set). Following a START bit detect, eight bits are shifted into the SSPSR, and the address is compared against SSPADD. It is also compared to the general call address, fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag is set (eighth bit), and on the falling edge of the ninth bit (ACK bit), the SSPIF flag is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF to determine if the address was device specific or a general call address.

If the general call address is sampled with GCEN set and the slave configured in 10-bit Address mode, the second half of the address is not necessary. The UA bit will not be set and the slave will begin receiving data after the Acknowledge (Figure 9-12).



FIGURE 9-12: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7- OR 10-BIT MODE)

9.2.17 MULTI -MASTER COMMUNICATION, BUS COLLISION, AND BUS ARBITRATION

Multi-master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, bus arbitration is initiated when one master outputs a '1' on SDA (by letting SDA float high) and another master asserts a '0'. If the expected data on SDA is a '1' and the data sampled on the SDA pin = '0', then a bus collision has taken place. The master that expected a '1' will set the Bus Collision Interrupt Flag, BCLIF, and reset the I^2C port to its IDLE state. (Figure 9-23).

A bus collision during transmit results in the following events:

- The transmission is halted.
- · The BF flag is cleared
- The SDA and SCL lines are de-asserted
- The restriction on writing to the SSPBUF during transmission is lifted.

When the user services the bus collision interrupt service routine, and if the I^2C bus is free, the user can resume communication by asserting a START condition.

A bus collision during a START, Repeated START, STOP or Acknowledge condition results in the following events:

- The condition is aborted.
- The SDA and SCL lines are de-asserted.
- The respective control bits in the SSPCON2 register are cleared.

When the user services the bus collision interrupt service routine, and if the l^2C bus is free, the user can resume communication by asserting a START condition.

The Master will continue to monitor the SDA and SCL pins, and if a STOP condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of START and STOP conditions allows the determination of when the bus is free. Control of the l^2C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is idle and the S and P bits are cleared.

FIGURE 9-23: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



9.2.17.1 BUS COLLISION DURING A START CONDITION

During a START condition, a bus collision occurs if:

- a) SDA or SCL are sampled low at the beginning of the START condition (Figure 9-24).
- b) SCL is sampled low before SDA is asserted low. (Figure 9-25).

During a START condition both the SDA and the SCL pins are monitored.

lf:

the SDA pin is already low or the SCL pin is already low,

then:

the START condition is aborted, and the BCLIF flag is set, and the SSP module is reset to its IDLE state (Figure 9-24).

The START condition begins with the SDA and SCL pins de-asserted. When the SDA pin is sampled high, the baud rate generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low

while SDA is high, a bus collision occurs, because it is assumed that another master is attempting to drive a data '1' during the START condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 9-26). If however a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The baud rate generator is then reloaded and counts down to 0, and during this time, if the SCL pin is sampled as '0', a bus collision does not occur. At the end of the BRG count the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a START condition is that no two bus masters can assert a START condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision, because the two masters must be allowed to arbitrate the first address following the START condition. If the address is the same, arbitration must be allowed to continue into the data portion, REPEATED START or STOP conditions.

FIGURE 9-24: BUS COLLISION DURING START CONDITION (SDA ONLY)



9.2.17.3 BUS COLLISION DURING A STOP CONDITION

Bus collision occurs during a STOP condition if:

- After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.
- b) After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The STOP condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the baud rate generator is loaded with SSPADD<6:0> and counts down to '0'. After the BRG times out SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 9-29). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 9-30).

FIGURE 9-29: BUS COLLISION DURING A STOP CONDITION (CASE 1)





10.0 VOLTAGE REFERENCE MODULE AND LOW-VOLTAGE DETECT

The Voltage Reference module provides reference voltages for the Brown-out Reset circuitry, the Low-voltage Detect circuitry and the A/D converter.

b b

b

b

The source for the reference voltages comes from the bandgap reference circuit. The bandgap circuit is energized anytime the reference voltage is required by the other sub-modules, and is powered down when not in use. The control registers for this module are LVDCON and REFCON, as shown in Register 10-1 and Figure 10-2.

REGISTER 10-1: LOW-VOLTAGE DETECT CONTROL REGISTER (LVDCON: 9Ch)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-
—	—	BGST	LVDEN	LV3	LV2	LV1	LV0
bit 7							t
Unimplem	ented: Read	d as '0'					
BGST: Bar	ndgap Stable	Status Flag	g bit				
1 = Indicate	es that the b	andgap volt	age is stable	e, and LVD i	nterrupt is re	eliable	
0 = Indicate	es that the b	andgap volt	age is not st	able, and L\	/D interrupt	should not b	be enab
LVDEN: Lo	w-voltage D	etect Powe	r Enable bit				
1 = Enable	s LVD, powe	ers up band	gap circuit a	nd reference	e generator		
0 = Disable	es LVD, pow	ers down ba	andgap circu	it if unused	by BOR or \	/RH/VRL	
LV<3:0>: L	ow Voltage	Detection Li	imit bits ⁽¹⁾				
1111 = Ext	ternal analoo	a input is us	ed				
1110 = 4.5	V						
1101 = 4.2	V						
1100 = 4.0	V						
1011 = 3.8	V						
1010 = 3.6	SV .						
1001 = 3.5	V V						
1000 = 3.3							
0110 = 2.8	V						
0101 = 2.7	ν. V						
0100 = 2.5	ŠV.						
0011 = Re	served. Do r	not use.					
0010 = Re	served. Do r	not use.					
0001 = Re	served. Do r	not use.					
0000 = Re	served. Do r	not use.					

Note: These are the minimum trip points for the LVD. See Table 15-8 for the trip point tolerances. Selection of reserved setting may result in an inadvertent interrupt.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented I	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

After the A/D module has been configured as desired and the analog input channels have their corresponding TRIS bits selected for port inputs, the selected channel must be acquired before conversion is started. The A/D conversion cycle can be initiated by setting the GO/DONE bit. The A/D conversion begins and lasts for 13TAD. The following steps should be followed for performing an A/D conversion:

- 1. Configure port pins:
 - Configure Analog Input mode (ANSEL)
 - Configure pin as input (TRISA or TRISB)
- 2. Configure the A/D module
 - Configure A/D Result Format / voltage reference (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
- 3. Configure A/D interrupt (if required)
 - Clear ADIF bit
 - Set ADIE bit
 - Set PEIE bit
 - Set GIE bit

FIGURE 11-3: A/D BLOCK DIAGRAM

- 4. Wait the required acquisition time.
- 5. START conversion
 - Set GO/DONE bit (ADCON0)
- 6. Wait 13TAD until A/D conversion is complete, by either:
 - Polling for the GO/DONE bit to be cleared OR
 - Waiting for the A/D interrupt
- 7. Read A/D Result registers (ADRESH and ADRESL), clear ADIF if required.
- 8. For next conversion, go to step 1, step 2 or step 3 as required.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRESH and ADRESL registers will be updated with the partially completed A/D conversion value. That is, the ADRESH and ADRESL registers will contain the value of the current incomplete conversion.

Note: Do not set the ADON bit and the GO/ DONE bit in the same instruction. Doing so will cause the GO/DONE bit to be automatically cleared.



12.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when a VDD rise is detected (in the range of 1.5V - 2.1V). Enable the internal MCLR feature to eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details. For a long rise time, enable external MCLR function and use circuit as shown in Figure 12-5.

Two delay timers, (PWRT on OST), have been provided which hold the device in RESET after a POR (dependent upon device configuration) so that all operational parameters have been met prior to releasing the device to resume/begin normal operation.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions, or if necessary an external POR circuit may be implemented to delay end of RESET for as long as needed.





- Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
 - **2:** R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
 - **3:** $R1 = 100\Omega$ to $1 k\Omega$ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).
 - 4: External MCLR must be enabled (MCLRE = 1).

12.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed TPWRT time-out on power-up type RESETS only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the RESET condition (VDD rises above BOR trip point). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

12.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on a power-up type RESET or a wakeup from SLEEP.

12.7 Programmable Brown-Out Reset (PBOR)

The Programmable Brown-out Reset module is used to generate a RESET when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV<1:0> configuration word bits.

Configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below the specified trip point for longer than TBOR, (parameter #35), the brown-out situation will RESET the chip. A RESET may not occur if VDD falls below the trip point for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer will be invoked at that point and will keep the chip in RESET an additional TPWRT. If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will again begin a TPWRT time delay. Even though the PWRT is always enabled when brown-out is enabled, the PWRT configuration word bit should be cleared (enabled) when brown-out is enabled.

14.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK[™] Object Linker/
 - MPLIB[™] Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD
- Device Programmers
 - PRO MATE® II Universal Device Programmer
 - PICSTART[®] Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
 - PICDEMTM 1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELOQ[®] Demonstration Board

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows[®]-based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

14.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

14.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

PIC16C717/770/771

NOTES:

15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771			$\begin{array}{llllllllllllllllllllllllllllllllllll$							
PIC16C717/770/771			Stand Opera	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions			
		Base plus Module curren	ıt							
D021A	Iwdt	Watchdog Timer		2	10	μA	VDD = 3V, -40°C to 125°C			
D021	Iwdt	Watchdog Timer		5	20	μA	VDD = 4V, -40°C to 125°C			
D021	Iwdt	Watchdog Timer		5	20	μA	$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D025	IT10SC	Timer1 Oscillator		3	9	μΑ	VDD = 3V, -40°C to 125°C			
D025	IT10SC	Timer1 Oscillator		4	12	μA	$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D025	IT10SC	Timer1 Oscillator		4	12	μA	$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D026*	IAD	ADC Converter		300		μΑ	VDD = 5.5V, A/D on, not converting			
D026*	IAD	ADC Converter		300		μA	VDD = 5.5V, A/D on, not converting			
D027	IPLVD	Programmable Low		55	125	μΑ	$VDD = 4V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D027A		Voltage Detect			150		VDD = 4V, -40°C to 125°C			
D027	IPLVD	Programmable Low		55	125	μΑ	VDD = 4V, -40°C to 85°C			
D027A					150		$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D028	IPBOR	Programmable Brown-		55	125	μA	$VDD = 5V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D028A		out Reset			150		VDD = 5V, -40°C to 125°C			
D028	Ipbor	Programmable Brown-		55	125	μA	$VDD = 5V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D028A					150		$VDD = 5V, -40^{\circ}C$ to 125°C			
D029	IVRH	Voltage reference High		200	750 1.0	μA mA	$VDD = 5V, -40^{\circ}C$ to $85^{\circ}C$			
D029A	ly pu	Voltago reference High		200	750		VDD = 5V, -40 C to 125 C			
D029	IVRH	Voltage reference right		200	10	μA mA	$VDD = 5V, -40^{\circ}C$ to $125^{\circ}C$			
D030	IVRI	Voltage reference Low		200	750		$V_{DD} = 4V -40^{\circ}C$ to 85°C			
D030A		tenage reference Low		200	1.0	mA	$V_{DD} = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D030	Ivrl	Voltage reference Low		200	750	μA	$VDD = 4V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D030A					1.0	mA	VDD = 4V, -40°C to 125°C			

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 15-14: PIC16C717 AND PIC16LC717 A/D CONVERTER CHARACTERISTI	CS:
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Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
A01	NR	Resolution		_	10 bits	bit	Min. resolution for A/D is 4.1 mV, VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- \leq VAIN \leq VREF+
A03	EIL	Integral error		_	±1	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, $VREF- \leq VAIN \leq VREF+$
A04	Edl	Differential error	_	_	±1	LSb	No missing codes to 10 bits VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, $VREF- \le VAIN \le VREF+$
A06	EOFF	Offset error	—	_	±2	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A07	Egn	Gain Error	—	_	±1	LSb	VREF+ = AVDD = 4.096V, VREF- = AVSS = 0V, VREF- ≤ VAIN ≤ VREF+
A10	—	Monotonicity		Note 3	—		$AVSS \leq VAIN \leq VREF+$
A20*	Vref	Reference voltage (VREF+ - VREF-)	4.096	_	VDD +0.3V	V	Absolute minimum electrical spec to ensure 10-bit accuracy.
A21*	VREF+	Reference V High (AVDD or VREF+)	VREF-	_	AVdd	V	Min. resolution for A/D is 4.1 mV
A22*	VREF-	Reference V Low (Avss or VREF-)	AVss	_	VREF+	V	Min. resolution for A/D is 4.1 mV
A25*	VAIN	Analog input voltage	Vrefl	_	Vrefh	V	
A30*	ZAIN	Recommended impedance of analog voltage source	_	_	2.5	kΩ	
A50*	IREF	VREF input current (Note 2)	_	_	10	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 11.0. During A/D conversion cycle.

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from External VREF+, or VREF-, or AVSS, or AVDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

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FIGURE 16-17: INTERNAL RC Fosc VS. VDD OVER TEMPERATURE (4 MHz)



18-Lead Plastic Dual In-line (P) – 300 mil (PDIP) 17.2

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eВ	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes: Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-001 Derwing b. C04 007

Drawing No. C04-007

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices in this data sheet are listed in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Difference	PIC16C717	PIC16C770	PIC16C771		
Program Memory	2К	2K	4K		
A/D	6 channels, 10 bits	6 channels, 12 bits	6 channels, 12 bits		
Dedicated AVDD and AVss	Not available	Available	Available		
Packages	18-pin PDIP, 18-pin windowed CERDIP, 18-pin SOIC, 20-pin SSOP	20-pin PDIP, 20-pin windowed CERDIP, 20-pin SOIC, 20-pin SSOP	20-pin PDIP, 20-pin windowed CERDIP, 20-pin SOIC, 20-pin SSOP		