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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc770-i-so

2.0 MEMORY ORGANIZATION

There are two memory blocks in each of these PIC® microcontrollers. Each block (Program Memory and Data Memory) has its own bus, so that concurrent access can occur.

Additional information on device memory may be found in the PICmicro™ Mid-Range MCU Family Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16C717/770/771 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16C717 and the PIC16C770 have 2K x 14 words of program memory. The PIC16C771 has 4K x 14 words of program memory. Accessing a location above the physically implemented address will cause a wrap-around.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK OF THE PIC16C717 AND PIC16C770

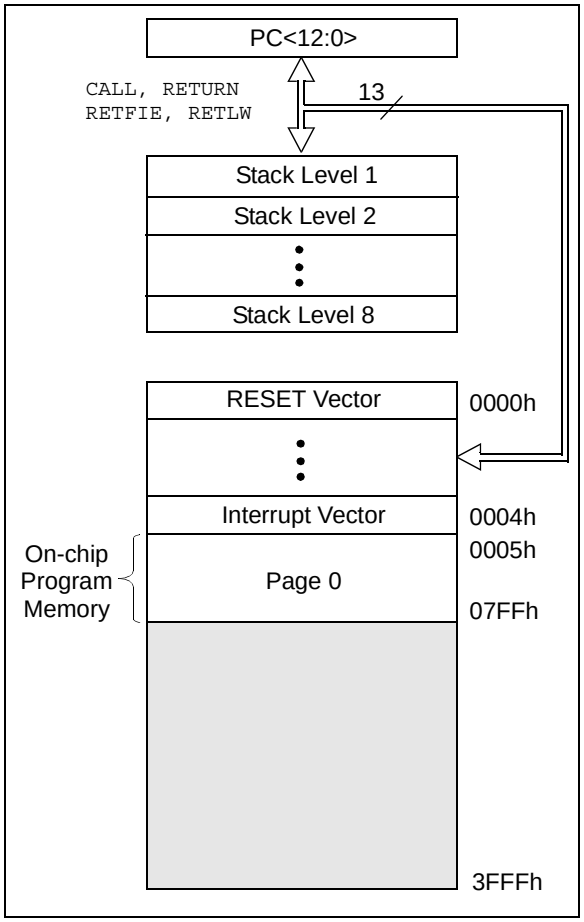
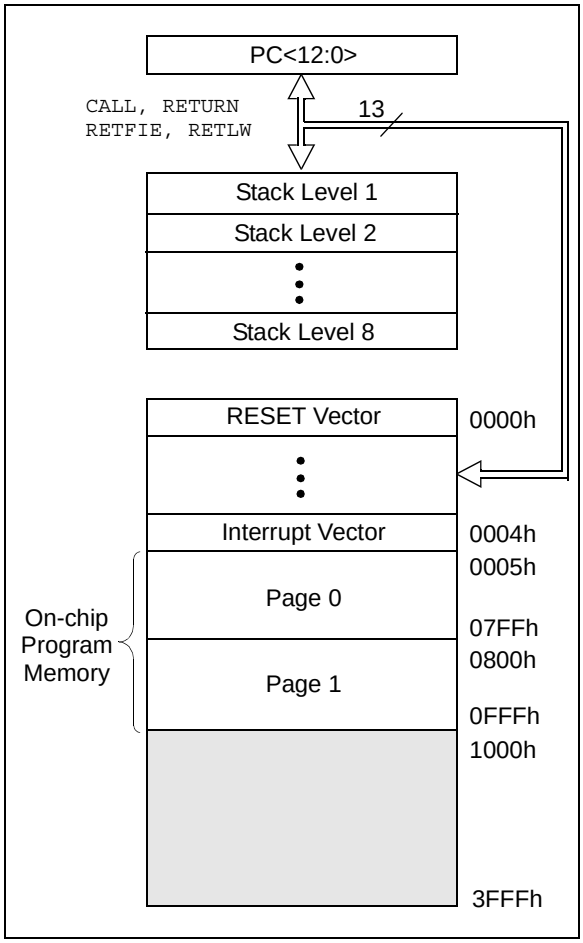


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK OF THE PIC16C771



2.2 Data Memory Organization

The data memory is partitioned into multiple banks, which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1	RP0	(STATUS<6:5>)

= 00 → Bank0
= 01 → Bank1
= 10 → Bank2
= 11 → Bank3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some frequently used special function registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly, through the File Select Register FSR.

2.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note:	Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTERRUPT CONTROL REGISTER (INTCON: 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit**(1)**
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit**(1)**
1 = At least one of the RB<7:0> pins changed state (must be cleared in software)
0 = None of the RB<7:0> pins have changed state

Note 1: Individual RB pin interrupt-on-change can be enabled/disabled from the Interrupt-on-Change PORTB register (IOCB).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.7 PIR2 REGISTER

This register contains the SSP Bus Collision and low-voltage detect interrupt flag bits.

Note:	Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-7: PERIPHERAL INTERRUPT REGISTER 2 (PIR2: 0Dh)

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
LVDIF	—	—	—	BCLIF	—	—	—
bit 7							bit 0

bit 7 **LVDIF:** Low Voltage Detect Interrupt Flag bit
1 = The supply voltage has fallen below the specified LVD voltage (must be cleared in software)
0 = The supply voltage is greater than the specified LVD voltage

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **BCLIF:** Bus Collision Interrupt Flag bit
1 = A bus collision has occurred while the SSP module configured in I^2C Master was transmitting (must be cleared in software)
0 = No bus collision occurred

bit 2-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

2.3 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register occur through the PCLATH register.

2.3.1 PROGRAM MEMORY PAGING

PIC16C717/770/771 devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. A return instruction pops a PC address off the stack onto the PC register. Therefore, manipulation of the PCLATH<4:3> bits are not required for the return instructions (which POPs the address from the stack).

2.4 Stack

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

FIGURE 2-4: LOADING OF PC IN DIFFERENT SITUATIONS

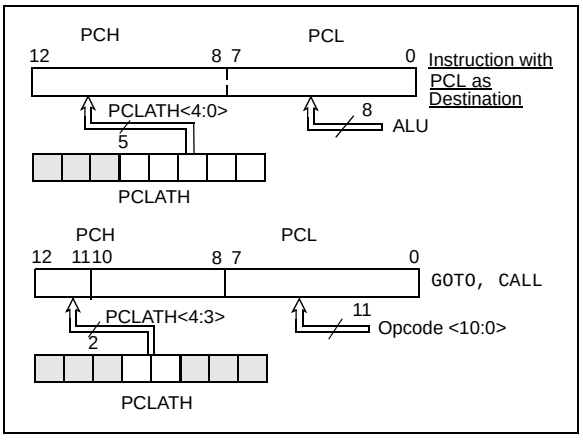


FIGURE 3-3: BLOCK DIAGRAM OF RA4/T0CKI

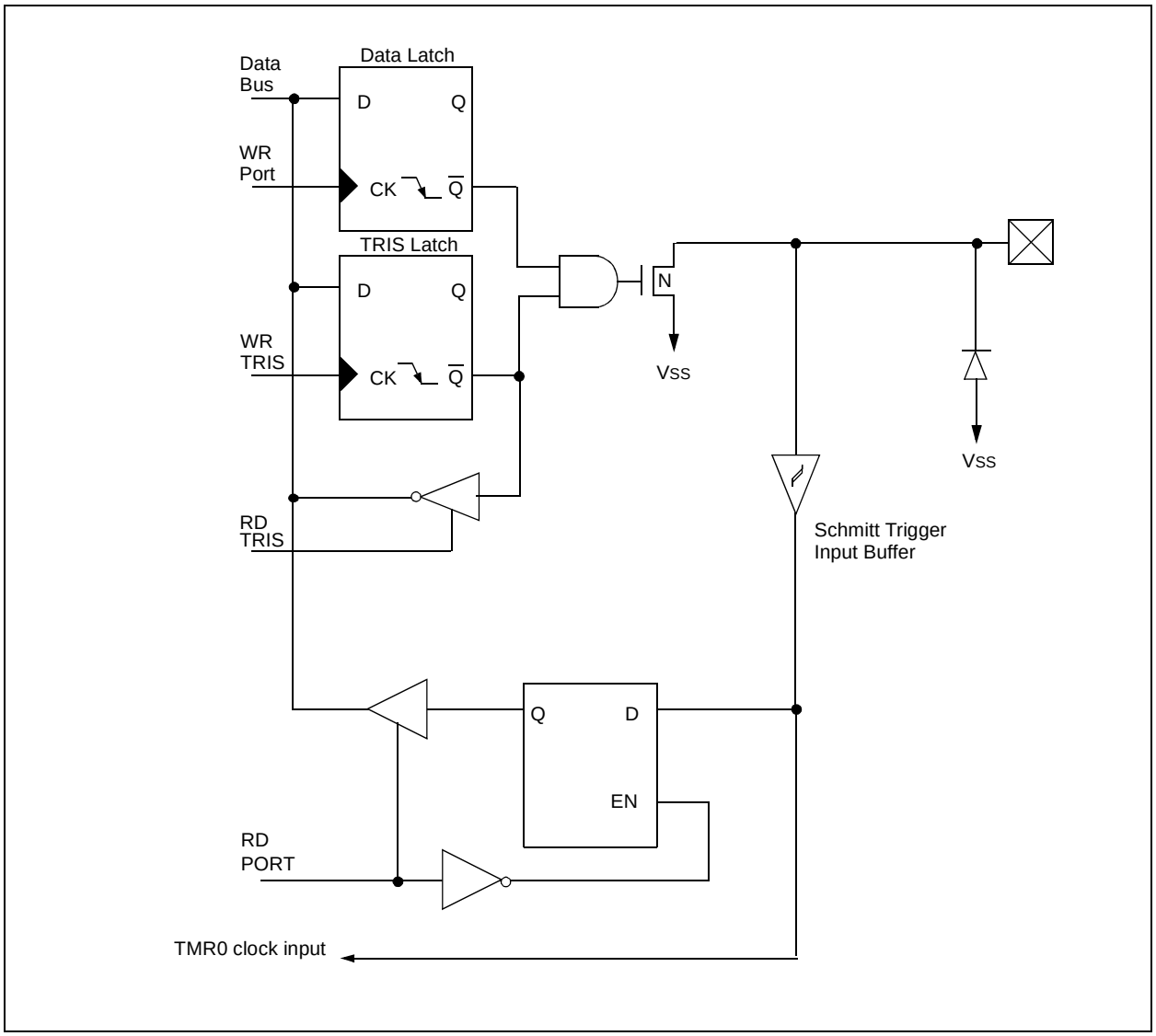
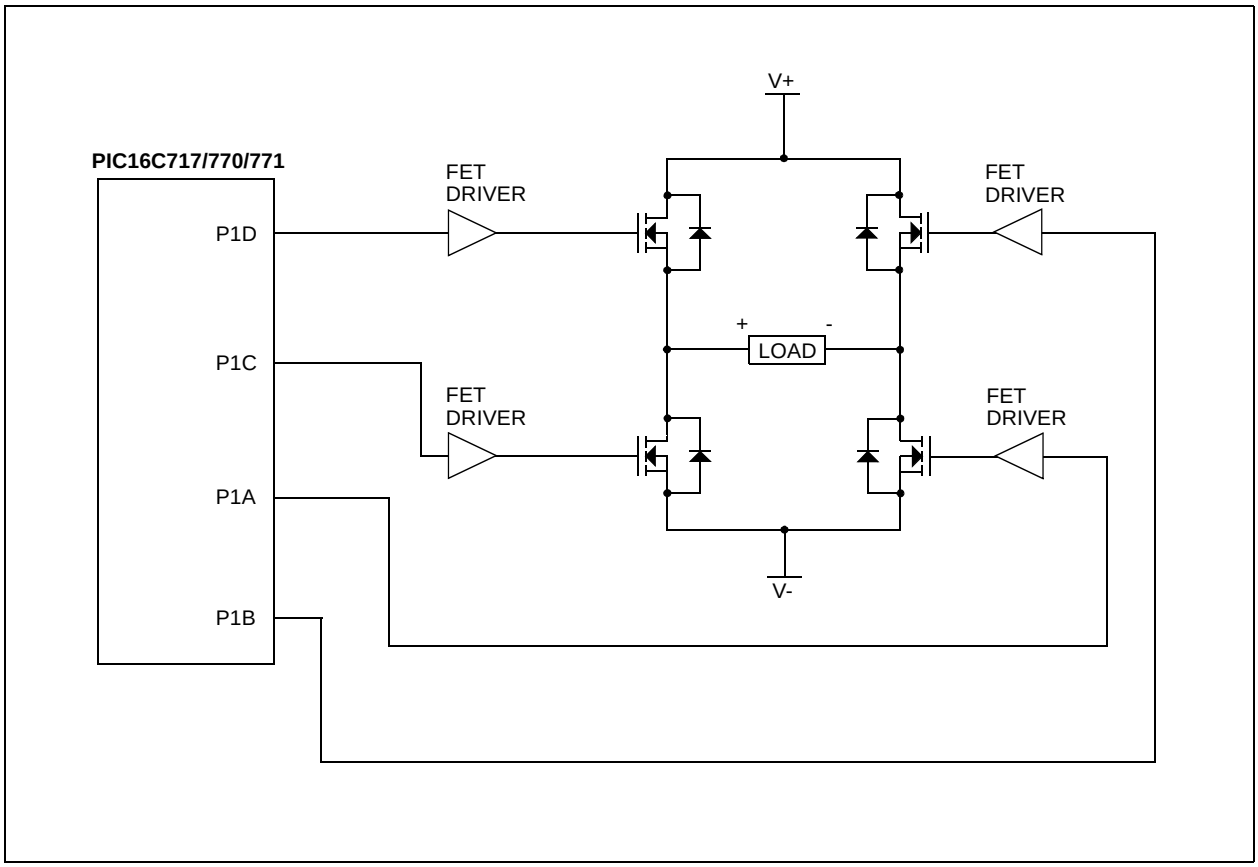


FIGURE 8-9: EXAMPLE OF FULL-BRIDGE APPLICATION



REGISTER 9-2: SYNC SERIAL PORT CONTROL REGISTER (SSPCON: 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

bit 7 **WCOL:** Write Collision Detect bit

Master Mode:

1 = A write to the SSPBUF register was attempted while the I^2C conditions were not valid for a transmission to be started

0 = No collision

Slave Mode:

1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)

0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit

In SPI mode

1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register. (Must be cleared in software).

0 = No overflow

In I^2C mode

1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode. (Must be cleared in software).

0 = No overflow

bit 5 **SSPEN:** Synchronous Serial Port Enable bit

In both modes, when enabled, the I/O pins must be properly configured as input or output.

In SPI mode

1 = Enables serial port and configures SCK, SDO, SDI, and $\overline{SS}$ as the source of the serial port pins

0 = Disables serial port and configures these pins as I/O port pins

In I^2C mode

1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins

0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP:** Clock Polarity Select bit

In SPI mode

1 = IDLE state for clock is a high level

0 = IDLE state for clock is a low level

In I^2C Slave mode SCK release control

1 = Enable clock

0 = Holds clock low (clock stretch) (used to ensure data setup time)

In I^2C Master mode

Unused in this mode

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

9.2.3 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I^2C bus is such that the first byte after the START condition usually determines which device will be the slave addressed by the master. The exception is the general call address, which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I^2C protocol. It consists of all 0's with R/$\overline{W}$ = 0

The general call address is recognized when the General Call Enable bit (GCEN) is set (SSPCON2<7> is set). Following a START bit detect, eight bits are shifted into the SSPSR, and the address is compared against SSPADD. It is also compared to the general call address, fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag is set (eighth bit), and on the falling edge of the ninth bit ($\overline{ACK}$ bit), the SSPIF flag is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF to determine if the address was device specific or a general call address.

If the general call address is sampled with GCEN set and the slave configured in 10-bit Address mode, the second half of the address is not necessary. The UA bit will not be set and the slave will begin receiving data after the Acknowledge (Figure 9-12).

FIGURE 9-12: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7- OR 10-BIT MODE)

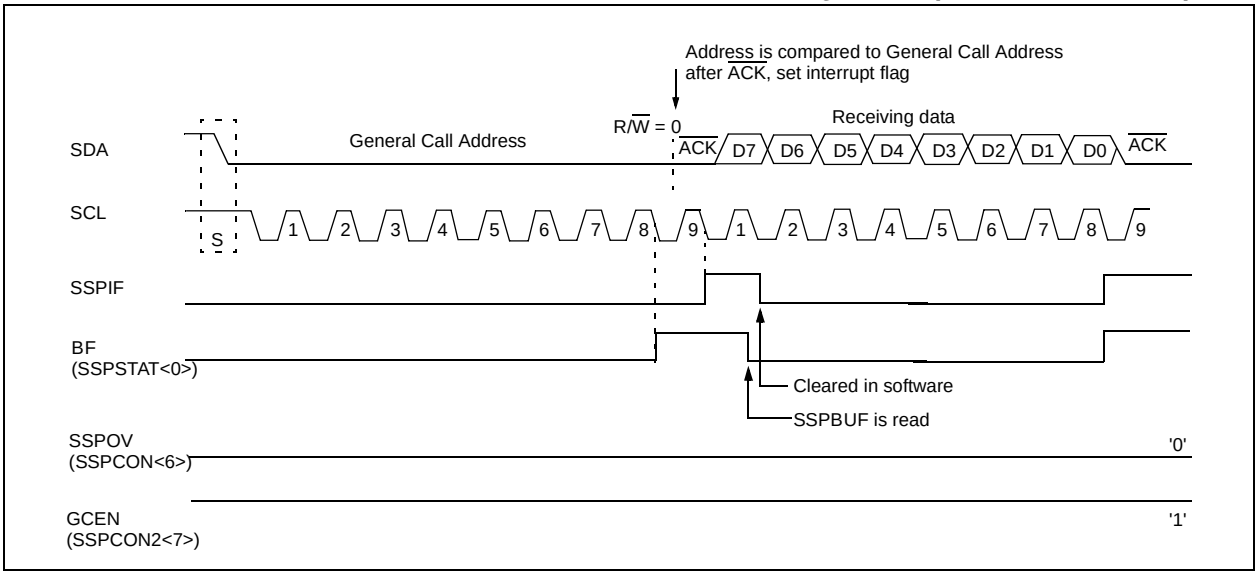
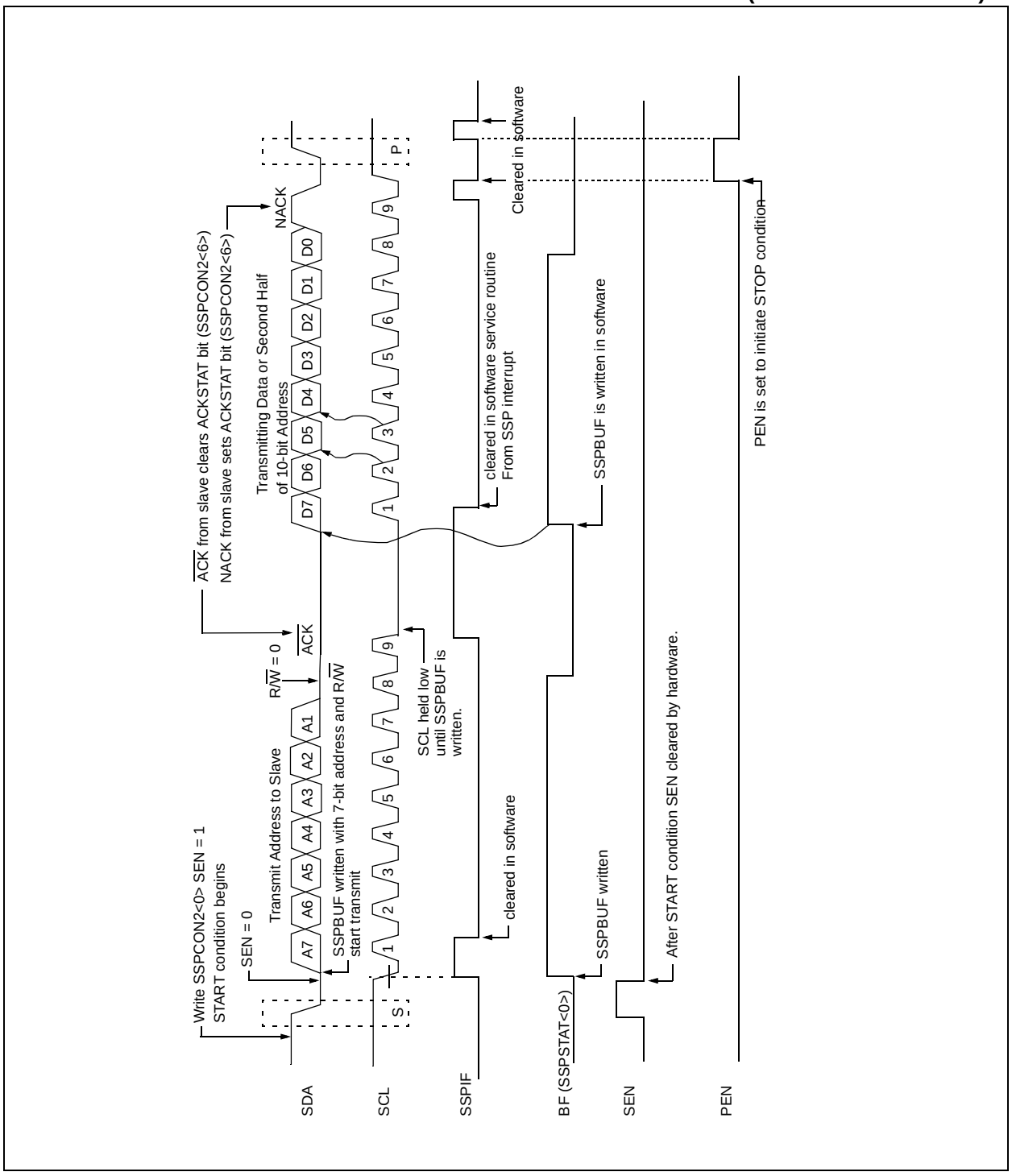


FIGURE 9-18: I²C MASTER MODE WAVEFORMS FOR TRANSMISSION (7 OR 10-BIT ADDRESS)



REGISTER 10-2: VOLTAGE REFERENCE CONTROL REGISTER (REFCON: 9BH)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
VRHEN	VRLEN	VRHOEN	VRLOEN	—	—	—	—
bit 7							bit 0

bit 7 **VRHEN:** Voltage Reference High Enable bit (VRH = 4.096V nominal)
1 = Enabled, powers up reference generator
0 = Disabled, powers down reference generator if unused by LVD, BOR, or VRL

bit 6 **VRLEN:** Voltage Reference Low Enable bit (VRL = 2.048V nominal)
1 = Enabled, powers up reference generator
0 = Disabled, powers down reference generator if unused by LVD, BOR, or VRH

bit 5 **VRHOEN:** High Voltage Reference Output Enable bit**(1)**
1 = Enabled, VRH analog reference is output on RA3 if enabled (VRHEN = 1)
0 = Disabled, analog reference is used internally only**(1)**

bit 4 **VRLOEN:** Low Voltage Reference Output Enable bit
1 = Enabled, VRL analog reference is output on RA2 if enabled (VRLEN = 1)
0 = Disabled, analog reference is used internally only

bit 3-0 **Unimplemented:** Read as '0'

Note 1: RA2 and RA3 must be configured as analog inputs when the VREF output functions are enabled (See ANSEL on page 25).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

11.10 A/D Operation During SLEEP

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be configured for RC (ADCS<1:0> = 11b). With the RC clock source selected, when the GO/DONE bit is set the A/D module waits one instruction cycle before starting the conversion cycle. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise during the sample and conversion. When the conversion cycle is completed the GO/DONE bit is cleared, and the result loaded into the ADRESH and ADRESL registers. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction causes the present conversion to be aborted and the A/D module is turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note:	For the A/D module to operate in SLEEP, the A/D clock source must be configured to RC (ADCS<1:0> = 11).

11.11 Connection Considerations

Since the analog inputs employ ESD protection, they have diodes to VDD and VSS. This requires that the analog input must be between VDD and VSS. If the input voltage exceeds this range by greater than 0.3V (either direction), one of the diodes becomes forward biased and it may damage the device if the input current specification is exceeded.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 2.5 kΩ recommended specification. It is recommended that any external components connected to an analog input pin (capacitor, zener diode, etc.) have very little leakage current.

TABLE 11-2: SUMMARY OF A/D REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
1Eh	ADRESH	A/D High Byte Result Register								xxxx xxxx	uuuu uuuu
9Eh	ADRESL	A/D Low Byte Result Register								xxxx xxxx	uuuu uuuu
9Bh	REFCON	VRHEN	VRLEN	VRHOEN	VRLOEN	—	—	—	—	0000 ----	0000 ----
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	CHS3	ADON	0000 0000	0000 0000
9Fh	ADCON1	ADFM	VCFG2	VCFG1	VCFG0	—	—	—	—	0000 ----	0000 ----
05h	PORTA	PORTA Data Latch when written: PORTA pins when read								000x 0000	000u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xx11	uuuu uu11
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
9Dh	ANSEL	—	—	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
17h	CCP1CON	—	—	—	—					0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

12.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator Selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Low-voltage detection
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming (ICSP)

These devices have a Watchdog Timer, which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up type RESETS only (POR, BOR), designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The INTRC and ER oscillator options save system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

Additional information on special features is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

12.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space.

Some of the core features provided may not be necessary to each application that a device may be used for. The configuration word bits allow these features to be configured/enabled/disabled as necessary. These features include code protection, Brown-out Reset and its trip point, the Power-up Timer, the watchdog timer and the devices Oscillator mode. As can be seen in Register 12-1, some additional configuration word bits have been provided for Brown-out Reset trip point selection.

13.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 13-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 13-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 13-2 lists the instructions recognized by the MPASM™ assembler.

Figure 13-1 shows the general formats that the instructions can have.

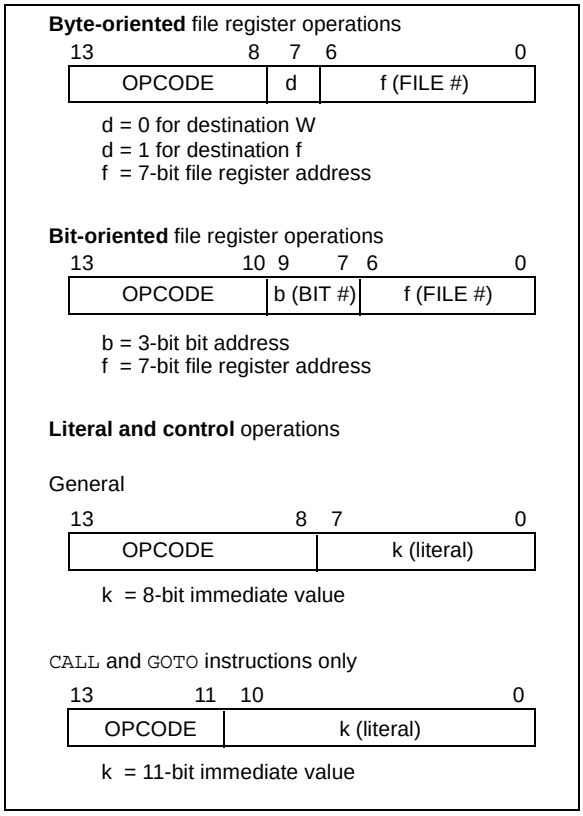
Note: To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16C717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IDD	**Supply Current(2)**					
D010D		**PIC16LC7XX**		1.0	2.0	mA	FOSC = 10 MHz, VDD = 3V, -40°C to 85°C
D010E					3.0		FOSC = 10 MHz, VDD = 3V, -40°C to 125°C
D010G				0.36	1.0	mA	FOSC = 4 MHz, VDD = 2.5V, -40°C to 125°C
D010K				11	45	µA	FOSC = 32 kHz, VDD = 2.5V, -40°C to 125°C
	IDD	**Supply Current(2)**					
D010		**PIC16C7XX**		4.0	7.5	mA	FOSC = 20 MHz, VDD = 5.5V, -40°C to 85°C
D010A					12.0		FOSC = 20 MHz, VDD = 5.5V, -40°C to 125°C
D010B				2.5	5.0	mA	FOSC = 20 MHz, VDD = 4V, -40°C to 85°C
D010C					6.0		FOSC = 20 MHz, VDD = 4V, -40°C to 125°C
D010F				0.55	1.5	mA	FOSC = 4 MHz, VDD = 4V, -40°C to 125°C
D010H				30	80	µA	FOSC = 32 kHz, VDD = 4V, -40°C to 85°C
D010J					95		FOSC = 32 kHz, VDD = 4V, -40°C to 125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active Operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

15.4.3 PROGRAMMABLE BROWN-OUT RESET MODULE (PBOR)

TABLE 15-9: DC CHARACTERISTICS: PBOR

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC Characteristics Section 15.1.					
Param. No.	**Characteristic**		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D005	BOR Voltage	BORV<1:0> = 11	VBOR	2.5	2.58	2.66	V	
		BORV<1:0> = 10		2.7	2.78	2.86		
		BORV<1:0> = 01		4.2	4.33	4.46		
		BORV<1:0> = 00		4.5	4.64	4.78		

15.4.4 VREF MODULE

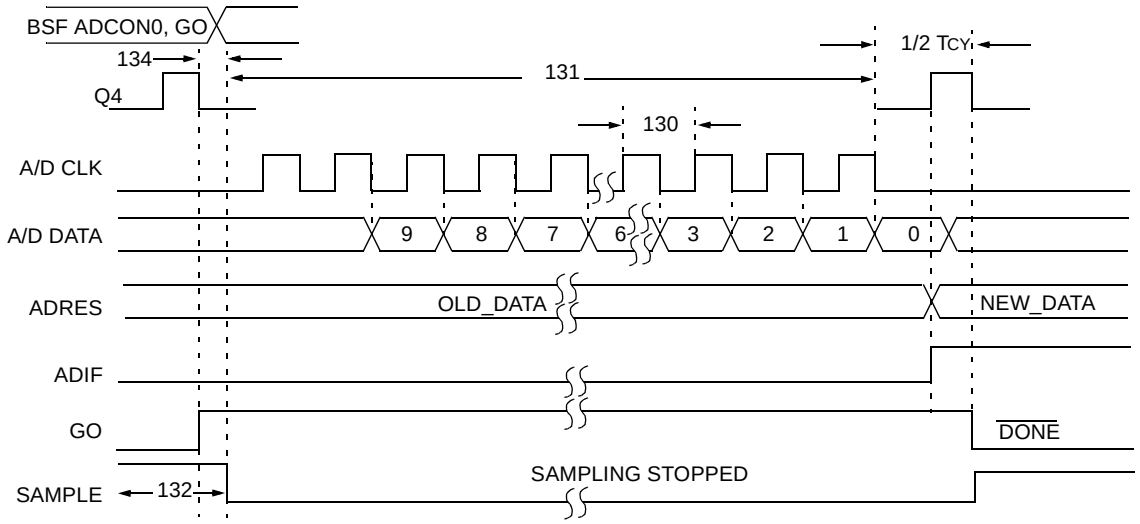
TABLE 15-10: DC CHARACTERISTICS: VREF

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC Characteristics Section 15.1.					
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
D400	VRL	Output Voltage	2.0	2.048	2.1	V	VDD ≥ 2.7V, -40°C ≤ TA ≤ +85°C	
	VRH		4.0	4.096	4.2	V	VDD ≥ 4.5V, -40°C ≤ TA ≤ +85°C	
D400A	VRL	Output Voltage	1.9	2.048	2.2	V	VDD ≥ 2.7V, -40°C ≤ TA ≤ +125°C	
	VRH		4.0	4.096	4.3	V	VDD ≥ 4.5V, -40°C ≤ TA ≤ +125°C	
D404*	IVREFSO	External Load Source	—	—	5	mA		
D405*	IVREFSI	External Load Sink	—	—	-5	mA		
*	CL	External Capacitor Load	—	—	200	pF		
D406*	ΔVout/ ΔIout	VRH Load Regulation	—	0.6	1	mV/mA	VDD ≥ 5V	ISOURCE = 0 mA to 5 mA
			—	1	4			ISINK = 0 mA to 5 mA
		VRL Load Regulation	—	0.6	1		VDD ≥ 3V	ISOURCE = 0 mA to 5 mA
			—	2	4			ISINK = 0 mA to 5 mA

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-16: PIC16C717 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D RC clock source is selected, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-15: PIC16C717 AND PIC16LC717 A/D CONVERSION REQUIREMENT (NORMAL MODE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130*(3)	TAD	A/D clock period	1.6	—	—	µs	Tosc based, VREF ≥ 2.5V
			3.0	—	—	µs	Tosc based, VREF full range
							ADCS<1:0> = 11 (A/D RC mode)
			3.0	6.0	9.0	µs	At VDD = 2.5V
			2.0	4.0	6.0	µs	At VDD = 5.0V
131*	TCNV	Conversion time (not including acquisition time) **(Note 1)**	—	11TAD	—	TAD	
132*	TACQ	Acquisition Time	**(Note 2)**	11.5	—	µs	
			5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD).
134*	TGO	Q4 to A/D clock start	—	TOSC/2	—	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

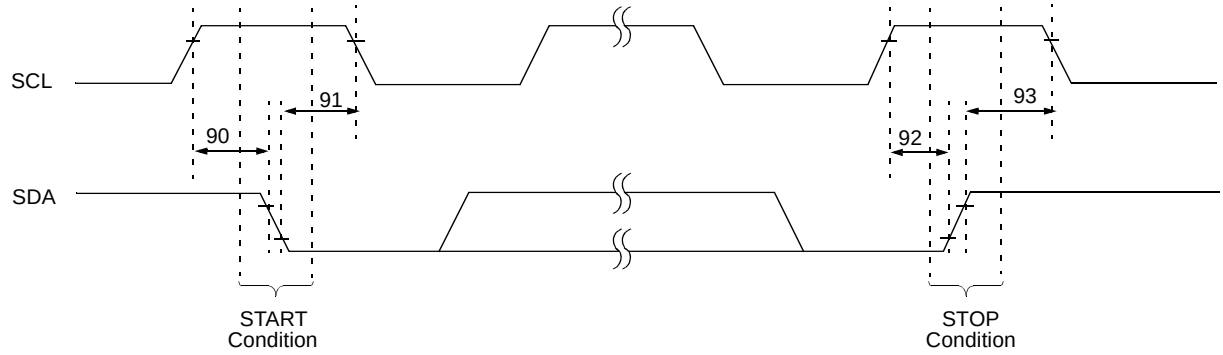
Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.6 for minimum conditions.

3: These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

15.6 Master SSP I²C Mode Timing Waveforms and Requirements

FIGURE 15-22: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS



Note: Refer to Figure 15-4 for load conditions.

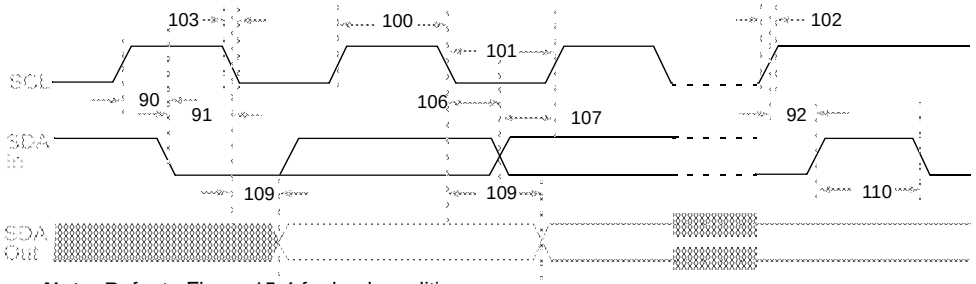
TABLE 15-21: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	Only relevant for a Repeated START condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
93*	THD:STO	STOP condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		

* These parameters are characterized but not tested. For the value required by the I²C specification, please refer to the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

Maximum pin capacitance = 10 pF for all I²C pins.

FIGURE 15-23: MASTER SSP I²C BUS DATA TIMING



Note: Refer to Figure 15-4 for load conditions.

FIGURE 16-18: MAXIMUM I_{PD} VS. V_{DD} (-40°C TO +125°C)

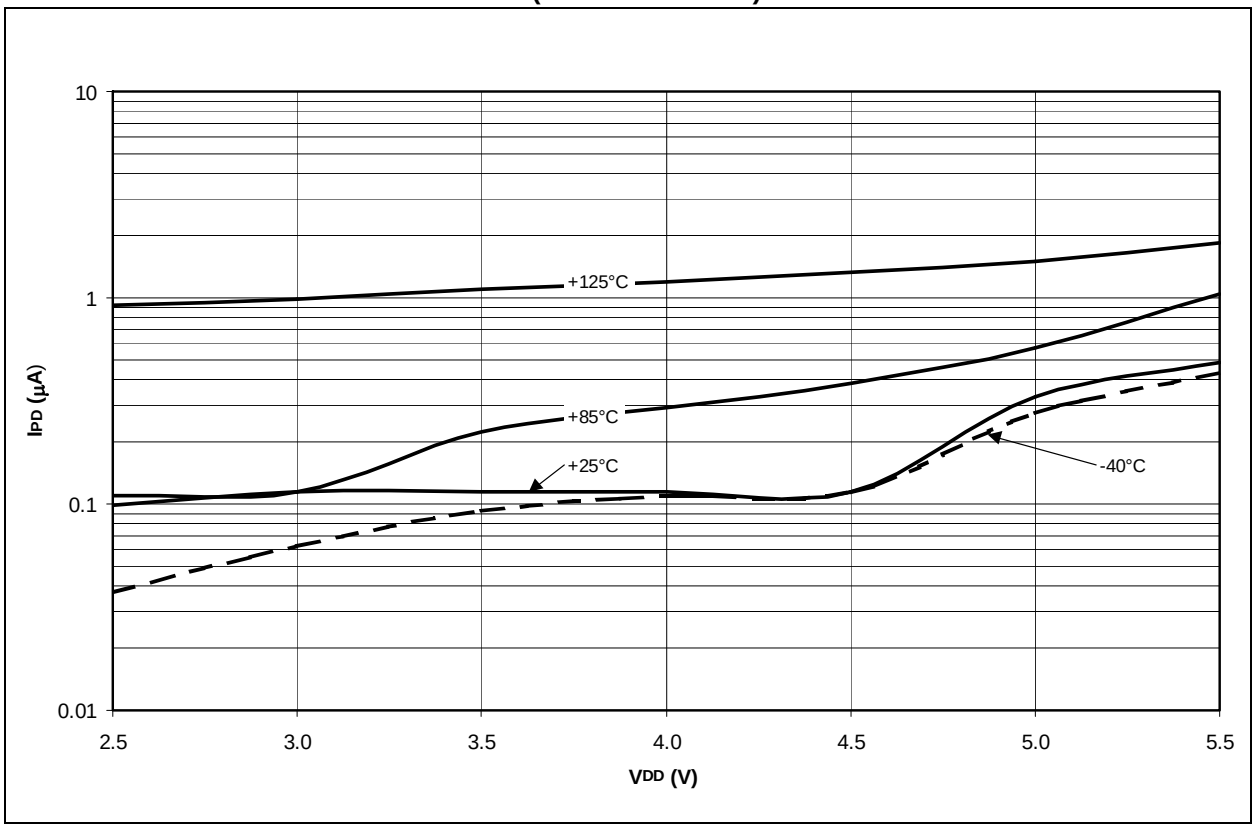
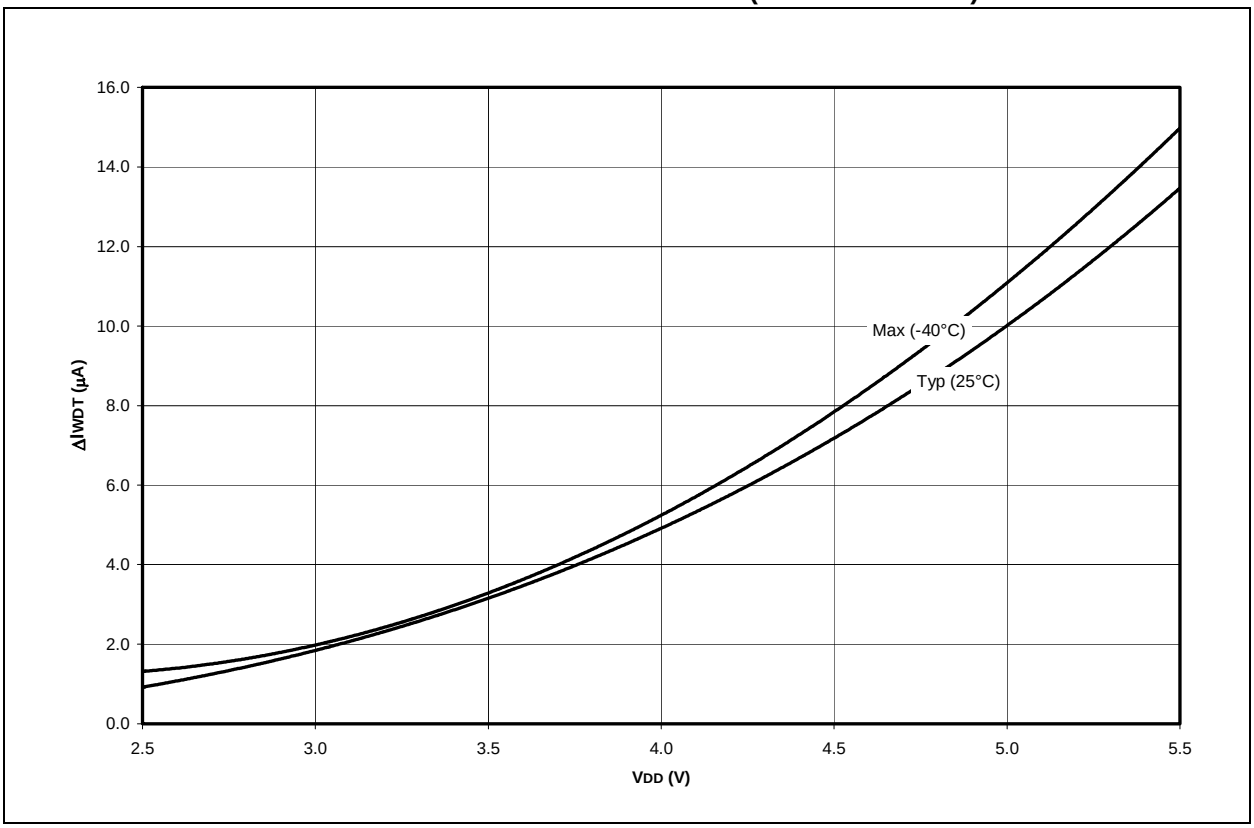


FIGURE 16-19: TYPICAL AND MAXIMUM ΔIWDT VS. VDD (-40°C TO +125°C)



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