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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 15 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 6x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lc770t-i-ss |

**EXAMPLE 3-1: Initializing PORTA**

```
BCF     STATUS, RP0     ; Select Bank 0
CLRF    PORTA           ; Initialize PORTA by
                        ; clearing output
                        ; data latches
BSF     STATUS, RP0     ; Select Bank 1
MOVLW   0Fh             ; Value used to
                        ; initialize data
                        ; direction
MOVWF   TRISA           ; Set RA<3:0> as inputs
                        ; RA<7:4> as outputs. RA<7:6>availability depends on oscillator selection.
MOVLW   03              ; Set RA<1:0> as analog inputs, RA<7:2> are digital I/O
MOVWF   ANSEL
BCF     STATUS, RP0     ; Return to Bank 0
```

**FIGURE 3-1: BLOCK DIAGRAM OF RA0/AN0, RA1/AN1/LVDIN**

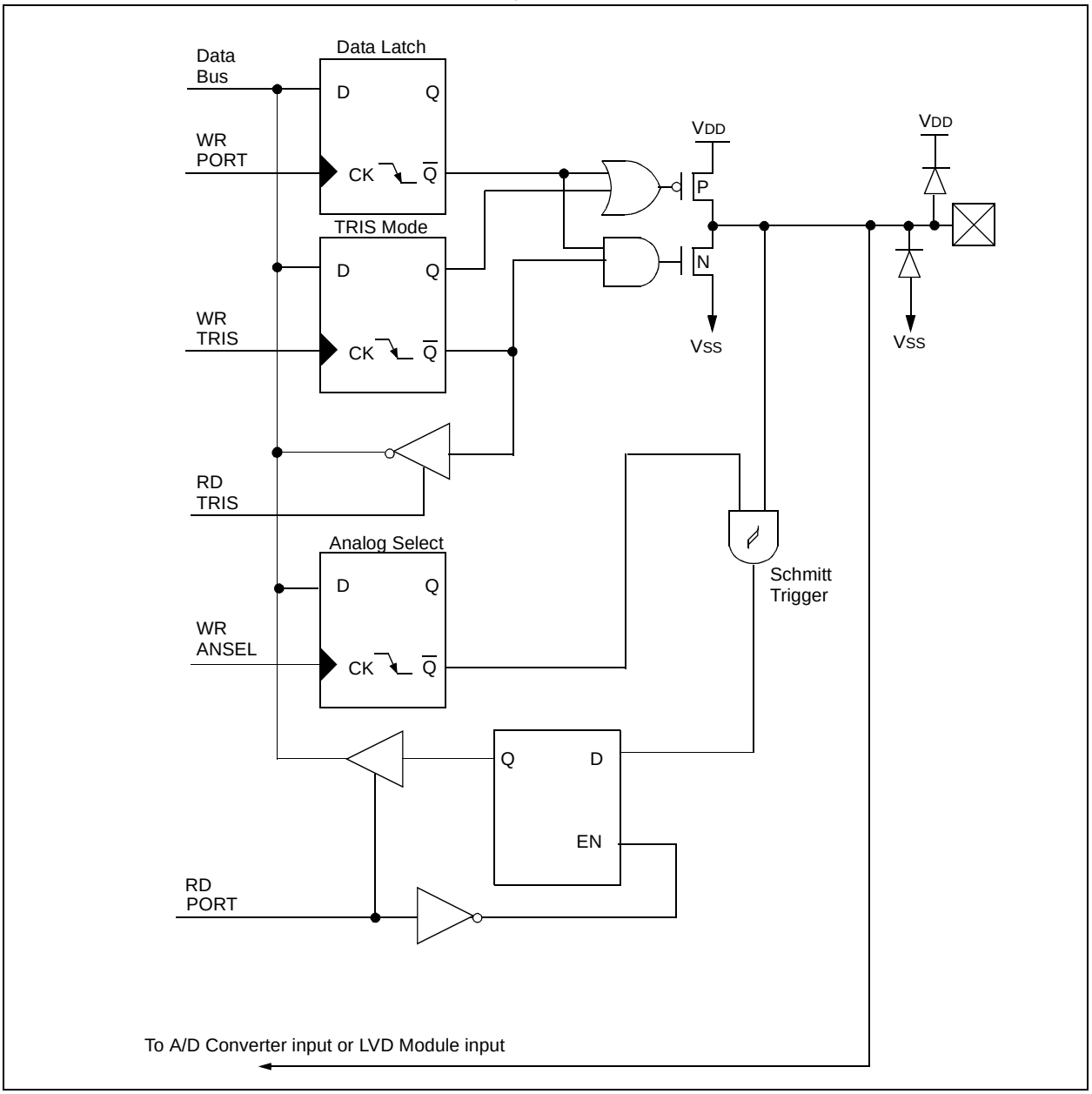
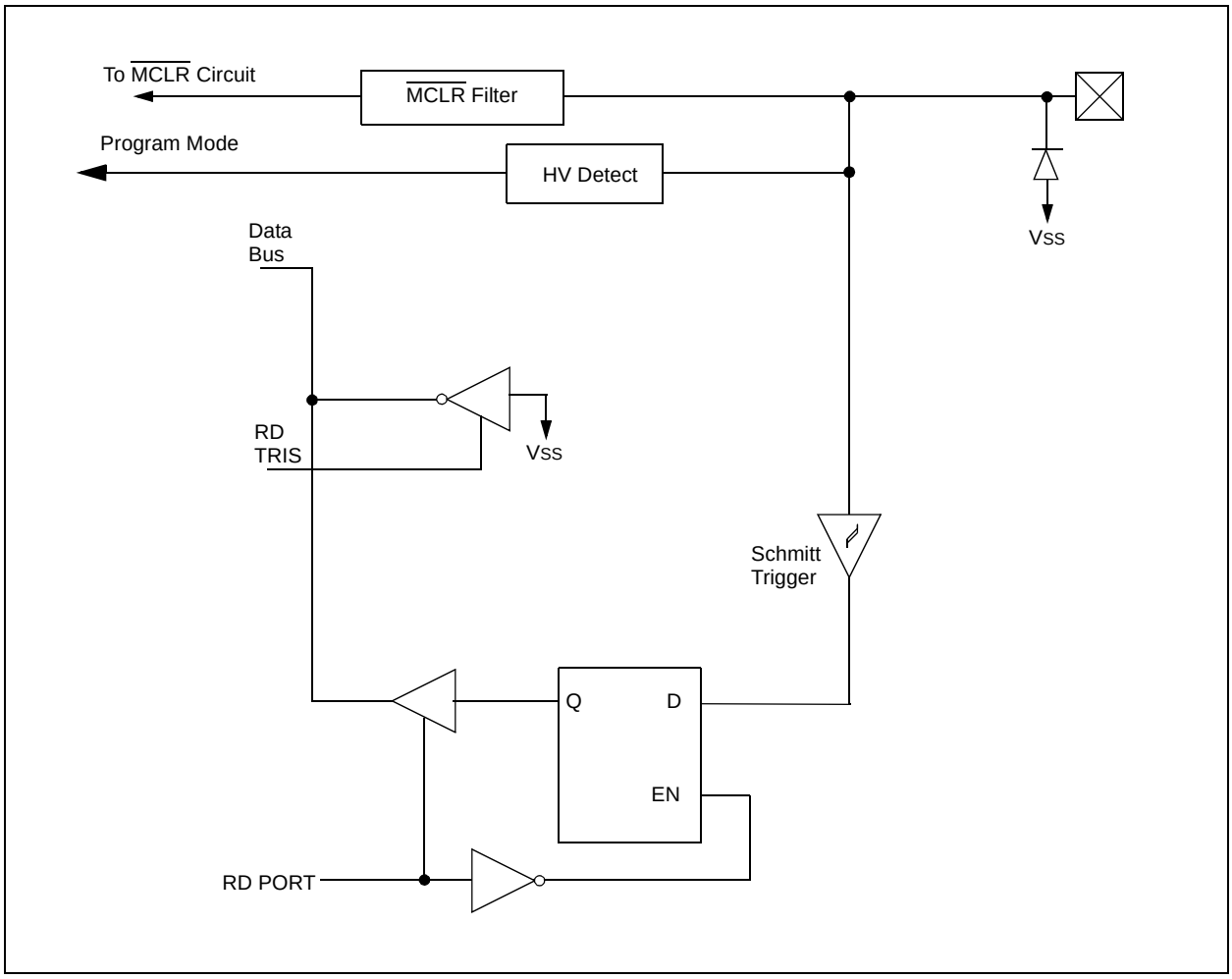


**FIGURE 3-4: BLOCK DIAGRAM OF RA5/$\overline{MCLR}$/VPP**



## 3.3 PORTB and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

**EXAMPLE 3-2: Initializing PORTB**

```
BCF     STATUS, RP0 ;
CLRF    PORTB       ; Initialize PORTB by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                    ; RB<5:4> as outputs
                    ; RB<7:6> as inputs
MOVLW   0x30        ; Set RB<1:0> as analog
                      inputs
MOVWF   ANSEL       ;
BCF     STATUS, RP0 ; Return to Bank 0
```

Each of the PORTB pins has an internal pull-up, which can be individually enabled from the WPUB register. A single global enable bit can turn on/off the enabled pull-ups. Clearing the $\overline{\text{RBPU}}$ bit, (OPTION_REG<7>), enables the weak pull-up resistors. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Each of the PORTB pins, if configured as input, also has an interrupt-on-change feature, which can be individually selected from the IOCB register. The RBIE bit in the INTCON register functions as a global enable bit to turn on/off the interrupt-on-change feature. The selected inputs are compared to the old value latched on the last read of PORTB. The "mismatch" outputs are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

a) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

**TABLE 3-3: PORTB FUNCTIONS**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RB0/AN4/INT | RB0 | TTL | CMOS | Bi-directional I/O(1) |
| | AN4 | AN | | A/D input |
| | INT | ST | | Interrupt input |
| RB1/AN5/$\overline{SS}$ | RB1 | TTL | CMOS | Bi-directional I/O(1) |
| | AN5 | AN | | A/D input |
| | $\overline{SS}$ | ST | | SSP slave select input |
| RB2/SCK/SCL | RB2 | TTL | CMOS | Bi-directional I/O(1) |
| | SCK | ST | CMOS | Serial clock I/O for SPI |
| | SCL | ST | OD | Serial clock I/O for $I^2C$ |
| RB3/CCP1/P1A | RB3 | TTL | CMOS | Bi-directional I/O(1) |
| | CCP1 | ST | CMOS | Capture 1 input/Compare 1 output |
| | P1A | | CMOS | PWM P1A output |
| RB4/SDI/SDA | RB4 | TTL | CMOS | Bi-directional I/O(1) |
| | SDI | ST | | Serial data in for SPI |
| | SDA | ST | OD | Serial data I/O for $I^2C$ |
| RB5/SDO/P1B | RB5 | TTL | CMOS | Bi-directional I/O(1) |
| | SDO | | CMOS | Serial data out for SPI |
| | P1B | | CMOS | PWM P1B output |
| RB6/T1OSO/T1CKI/P1C | RB6 | TTL | CMOS | Bi-directional I/O(1) |
| | T1OSO | | XTAL | Crystal/Resonator |
| | T1CKI | CMOS | | TMR1 clock input |
| | P1C | | CMOS | PWM P1C output |
| RB7/T1OSI/P1D | RB7 | TTL | CMOS | Bi-directional I/O(1) |
| | T1OSI | XTAL | | TMR1 crystal/resonator |
| | P1D | | CMOS | PWM P1D output |

**Note 1:** Bit programmable pull-ups.

**TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other RESETS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 06h, 106h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx xx11 | uuuu uu11 |
| 86h, 186h | TRISB | PORTB Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 81h, 181h | OPTION_REG | $\overline{RBPU}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 95h | WPUB | PORTB Weak Pull-up Control | | | | | | | | 1111 1111 | 1111 1111 |
| 96h | IOCB | PORTB Interrupt on Change Control | | | | | | | | 1111 0000 | 1111 0000 |
| 9Dh | ANSEL | — | — | ANS5 | ANS4 | ANS3 | ANS2 | ANS1 | ANS0 | --11 1111 | --11 1111 |

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

**TABLE 4-1: PROGRAM MEMORY READ REGISTER SUMMARY**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other RESETS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 18Ch | PMCON1 | Reserved | — | — | — | — | — | — | RD | 1--- ---0 | 1--- ---0 |
| 10Eh | PMDATH | — | — | PMD13 | PMD12 | PMD11 | PMD10 | PMD9 | PMD8 | --xx xxxx | --uu uuuu |
| 10Ch | PMDATL | PMD7 | PMD6 | PMD5 | PMD4 | PMD3 | PMD2 | PMD1 | PMD0 | xxxx xxxx | uuuu uuuu |
| 10Fh | PMADRH | — | — | — | — | PMA11 | PMA10 | PMA9 | PMA8 | ---- xxxx | ---- uuuu |
| 10Dh | PMADRL | PMA7 | PMA6 | PMA5 | PMA4 | PMA3 | PMA2 | PMA1 | PMA0 | xxxx xxxx | uuuu uuuu |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Program Memory Read.

## 6.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
  (Two 8-bit registers; TMR1H and TMR1L)
- Readable and writable (Both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- RESET from ECCP module trigger

Timer1 has a control register, shown in Register 6-1. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Figure 6-2 is a simplified block diagram of the Timer1 module.

Additional information on timer modules is available in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

### 6.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

The Operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

**REGISTER 6-1: TIMER1 CONTROL REGISTER (T1CON: 10h)**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON |
| bit 7 | | | | | | | bit 0 |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off **(1)**

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from pin RB6/T1OSO/T1CKI /P1C (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

**Note 1:** The oscillator inverter and feedback resistor are turned off to eliminate power drain.

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**TABLE 8-1: ECCP MODE - TIMER RESOURCE**

| ECCP Mode | Timer Resource |
|---|---|
| Capture | Timer1 |
| Compare | Timer1 |
| PWM | Timer2 |

## 8.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

An event is selected by control bits CCP1M<3:0> (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

### 8.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the TRISB<3> bit.

| **Note:** | If the RB3/CCP1/P1A pin is configured as an output, a write to the port can cause a capture condition. |
|---|---|

### 8.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work.

### 8.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in Operating mode.

### 8.1.4 ECCP PRESCALER

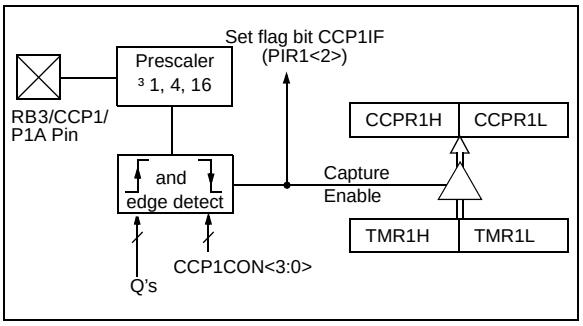
There are three prescaler settings, specified by bits CCP1M<3:0>. Whenever the ECCP module is turned off or the ECCP module is not in Capture mode, the prescaler counter is cleared. This means that any RESET will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 8-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

**EXAMPLE 8-1: Changing Between Capture Prescalers**

```
CLRF    CCP1CON     ; Turn ECCP module off
MOVLW   NEW_CAPT_PS ; Load WREG with the
                    ; new prescaler mode
                    ; value and ECCP ON
MOVWF   CCP1CON     ; Load CCP1CON with
                    ; this value
```

**FIGURE 8-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**




## 8.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 pin is:

- driven High
- driven Low
- toggle output (High to Low or Low to High)
- remains Unchanged

The action on the pin is based on the value of control bits CCP1M<3:0>. At the same time, interrupt flag bit CCP1IF is set.

Changing the ECCP mode select bits to the clear output on Match mode (CCP1M<3.0> = “1000”) presets the CCP1 output latch to the logic 1 level. Changing the ECCP mode select bits to the clear output on Match mode (CCP1M<3:0> = “1001”) presets the CCP1 output latch to the logic 0 level.

### 8.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the appropriate TRISB bit.

| **Note:** | Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the port data latch. |
|---|---|

### 8.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the ECCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

### 8.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only an ECCP interrupt is generated (if enabled).

### 8.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of ECCP resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special event trigger output of ECCP module will also start an A/D conversion if the A/D module is enabled.

| **Note:** | The special event trigger will not set the interrupt flag bit TMR1IF (PIR1<0>). |
|---|---|

**FIGURE 8-2: COMPARE MODE OPERATION BLOCK DIAGRAM**

Special event trigger will:
RESET Timer1, but not set interrupt flag bit TMR1IF (PIR1<0>).

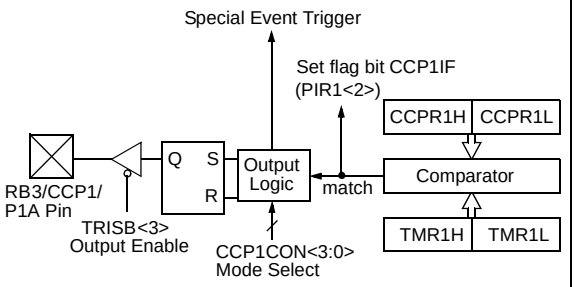
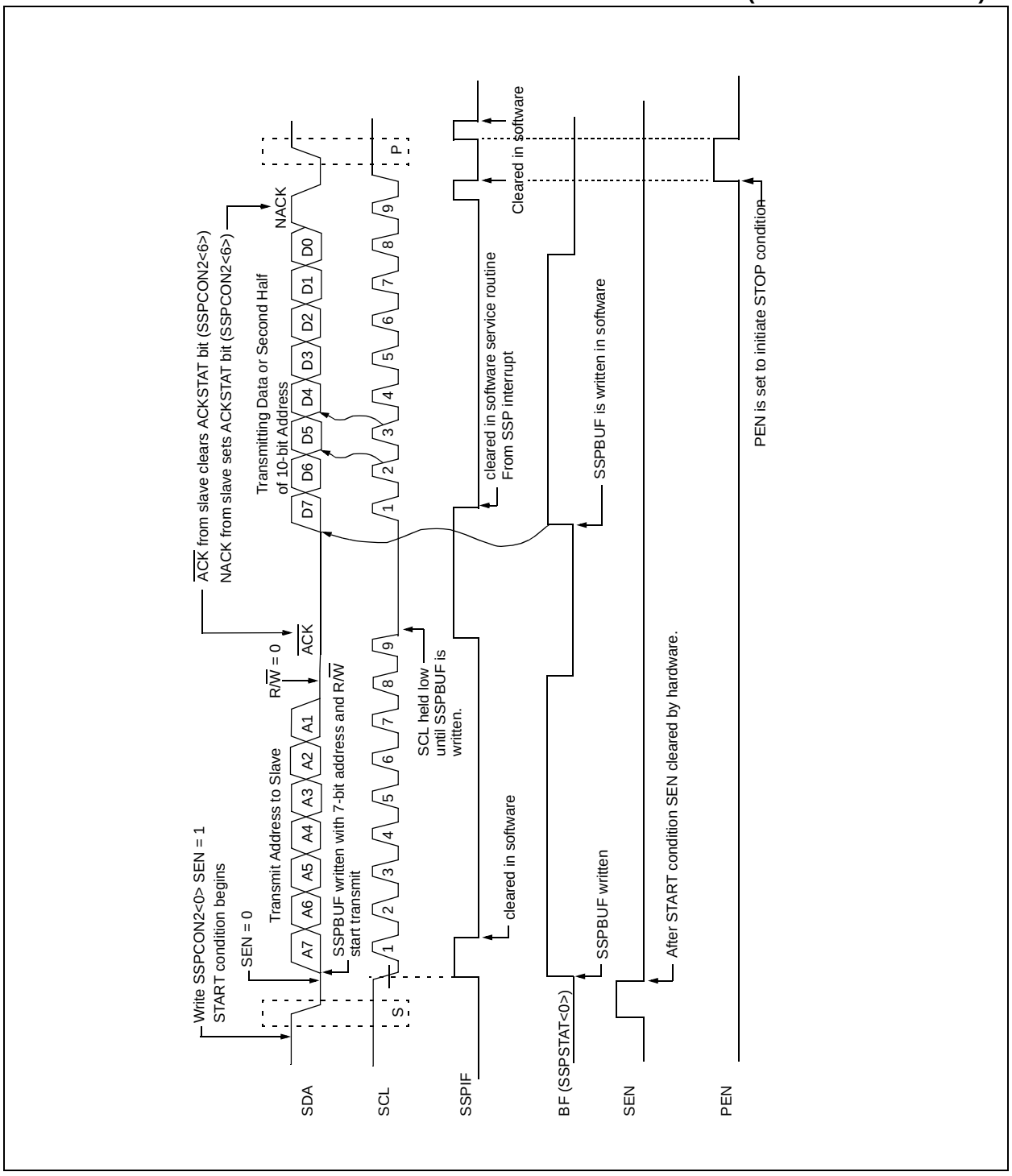



**TABLE 8-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other RESETS |
|---|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| PIR1 | PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| PIE1 | PSPIE(1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| TRISB | PORTB Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| TMR1L | Holding register for the Least Significant Byte of the 16-bit TMR1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| TMR1H | Holding register for the Most Significant Byte of the 16-bit TMR1register | | | | | | | | xxxx xxxx | uuuu uuuu |
| T1CON | — | — | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON | --00 0000 | --uu uuuu |
| CCPR1L | Capture/Compare/PWM register1 (LSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| CCPR1H | Capture/Compare/PWM register1 (MSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| CCP1CON | PWM1M1 | PWM1M0 | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0000 0000 | 0000 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

**FIGURE 9-18: I²C MASTER MODE WAVEFORMS FOR TRANSMISSION (7 OR 10-BIT ADDRESS)**



9.2.17.3 BUS COLLISION DURING A STOP CONDITION

Bus collision occurs during a STOP condition if:

a) After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.

b) After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The STOP condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the baud rate generator is loaded with SSPADD<6:0> and counts down to ‘0’. After the BRG times out SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 9-29). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 9-30).

**FIGURE 9-29: BUS COLLISION DURING A STOP CONDITION (CASE 1)**

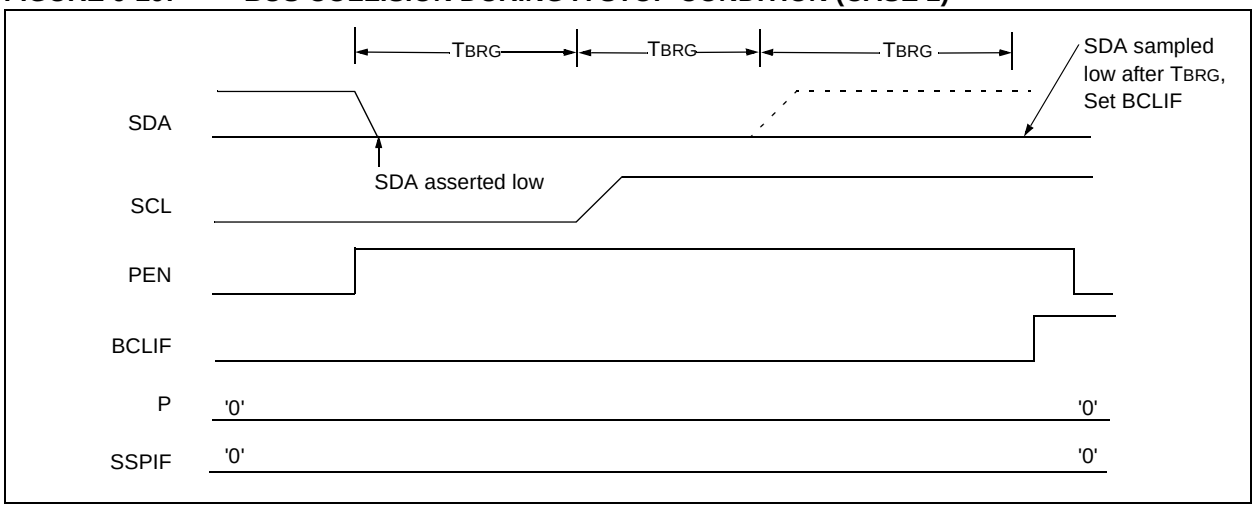



**FIGURE 9-30: BUS COLLISION DURING A STOP CONDITION (CASE 2)**

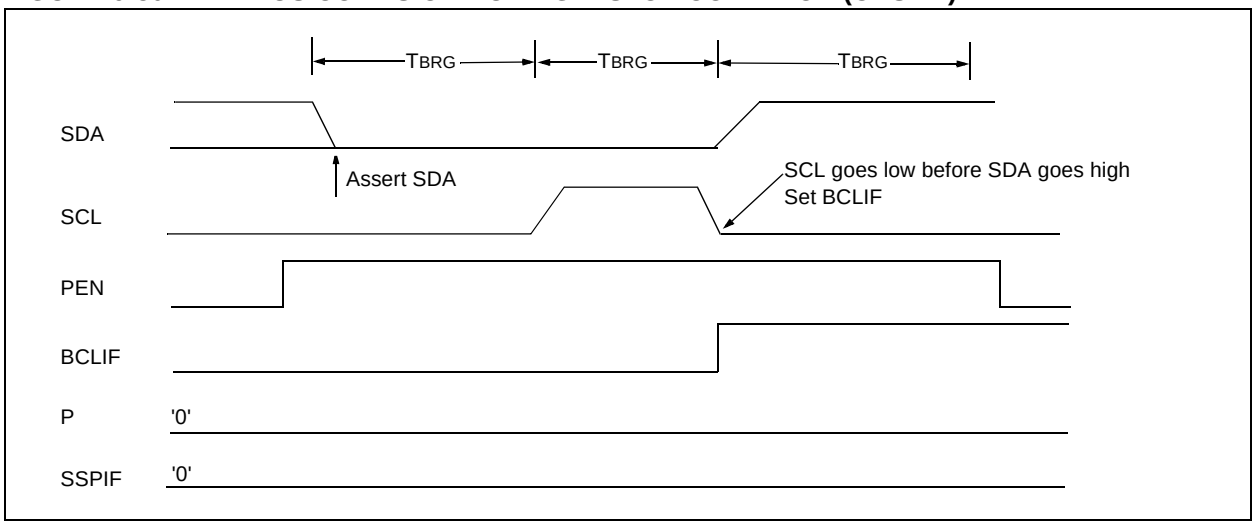


**FIGURE 12-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO $V_{DD}$): CASE 1**

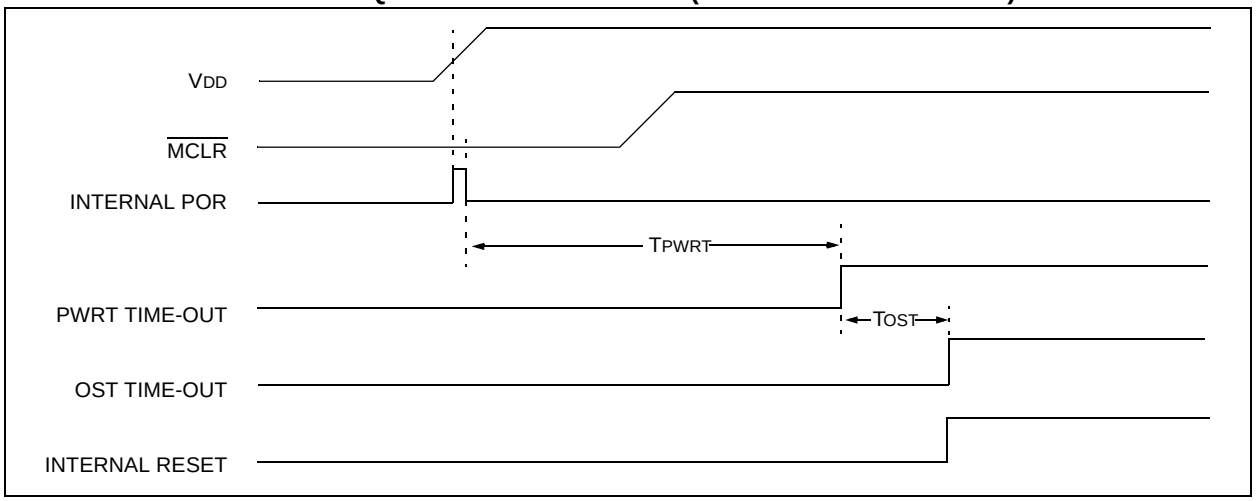



**FIGURE 12-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO $V_{DD}$): CASE 2**

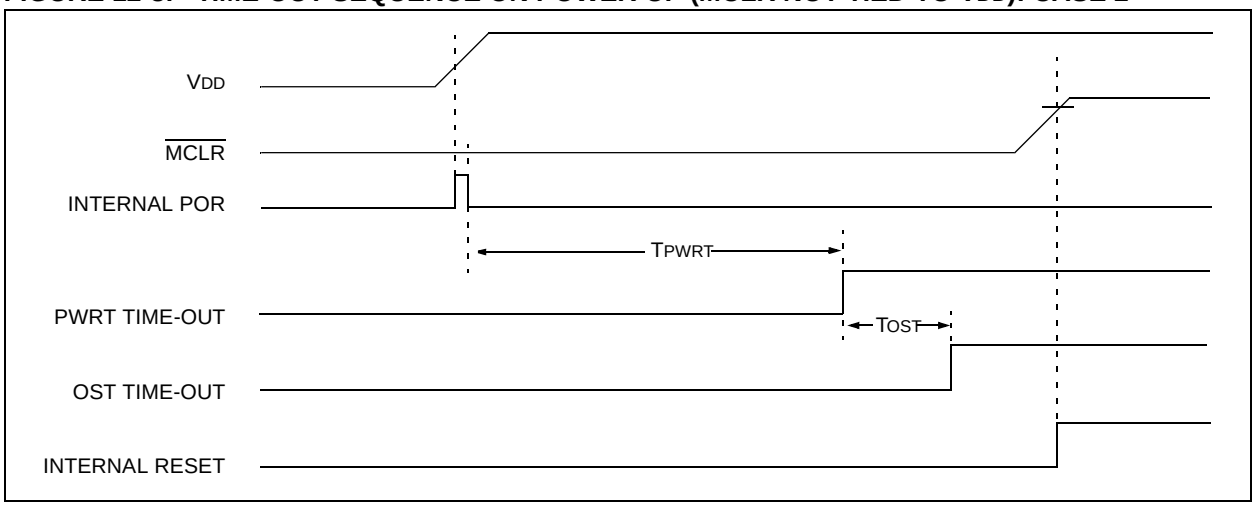
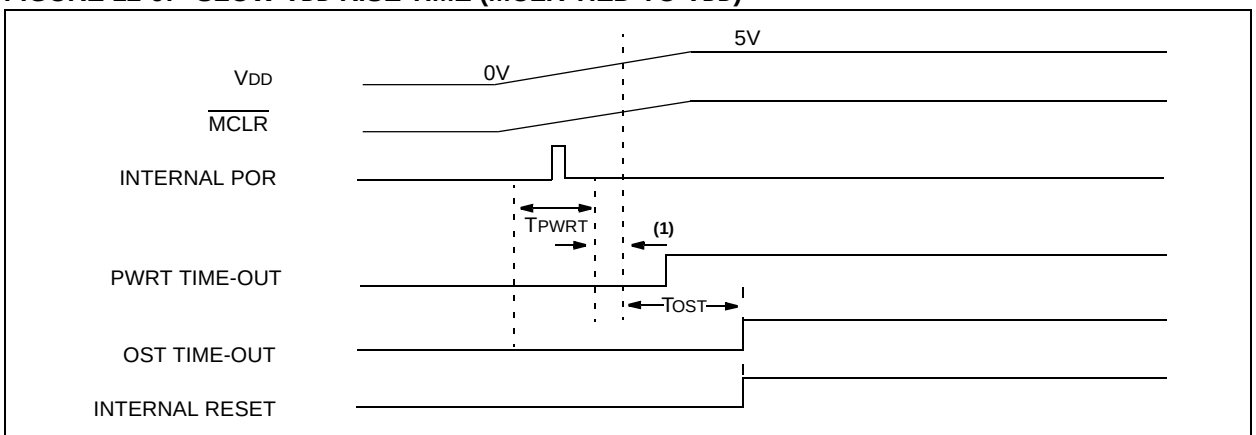



**FIGURE 12-9: SLOW $V_{DD}$ RISE TIME ($\overline{MCLR}$ TIED TO $V_{DD}$)**




**Note 1:** Time dependent on oscillator circuit

**FIGURE 15-6: EXTERNAL CLOCK TIMING**

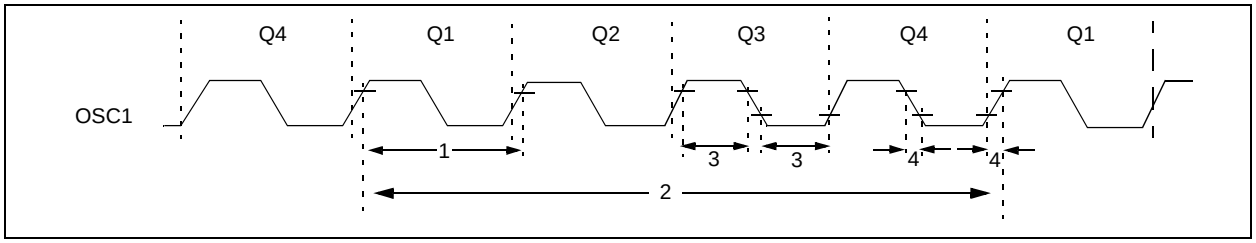



**TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS**

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 1A | FOSC | External CLKIN Frequency **(Note 1)** | DC | — | 4 | MHz | XT mode |
| | | | DC | — | 20 | MHz | EC mode |
| | | | DC | — | 20 | MHz | HS mode |
| | | | DC | — | 200 | kHz | LP mode |
| | | Oscillator Frequency **(Note 1)** | 0.1* | — | 4 | MHz | XT mode |
| | | | 4* | — | 20 | MHz | HS mode |
| | | | 5* | — | 200 | kHz | LP mode |
| 1 | TOSC | External CLKIN Period **(Note 1)** | 250 | — | — | ns | XT mode |
| | | | 50 | — | — | ns | EC mode |
| | | | 50 | — | — | ns | HS mode |
| | | | 5 | — | — | µs | LP mode |
| | | Oscillator Period **(Note 1)** | 250 | — | 10,000* | ns | XT mode |
| | | | 50 | — | 250* | ns | HS mode |
| | | | 5 | — | — | µs | LP mode |
| 2 | TCY | Instruction Cycle Time **(Note 1)** | 200 | TCY | DC | ns | TCY = 4/FOSC |
| 3* | TosL, TosH | External Clock in (OSC1) High or Low Time | 100 | — | — | ns | XT mode |
| | | | 2.5 | — | — | µs | LP mode |
| | | | 15 | — | — | ns | HS mode |
| | | | | | | | EC mode |
| 4* | TosR, TosF | External Clock in (OSC1) Rise or Fall Time | — | — | 25 | ns | XT mode |
| | | | — | — | 50 | ns | LP mode |
| | | | — | — | 15 | ns | HS mode |
| | | | | | | | EC mode |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Max. Frequency" values with a square wave applied to the OSC1/CLKIN pin.

When an external clock input is used, the "Min." frequency (or Max. TCY) limit is "DC" (no clock) for all devices.

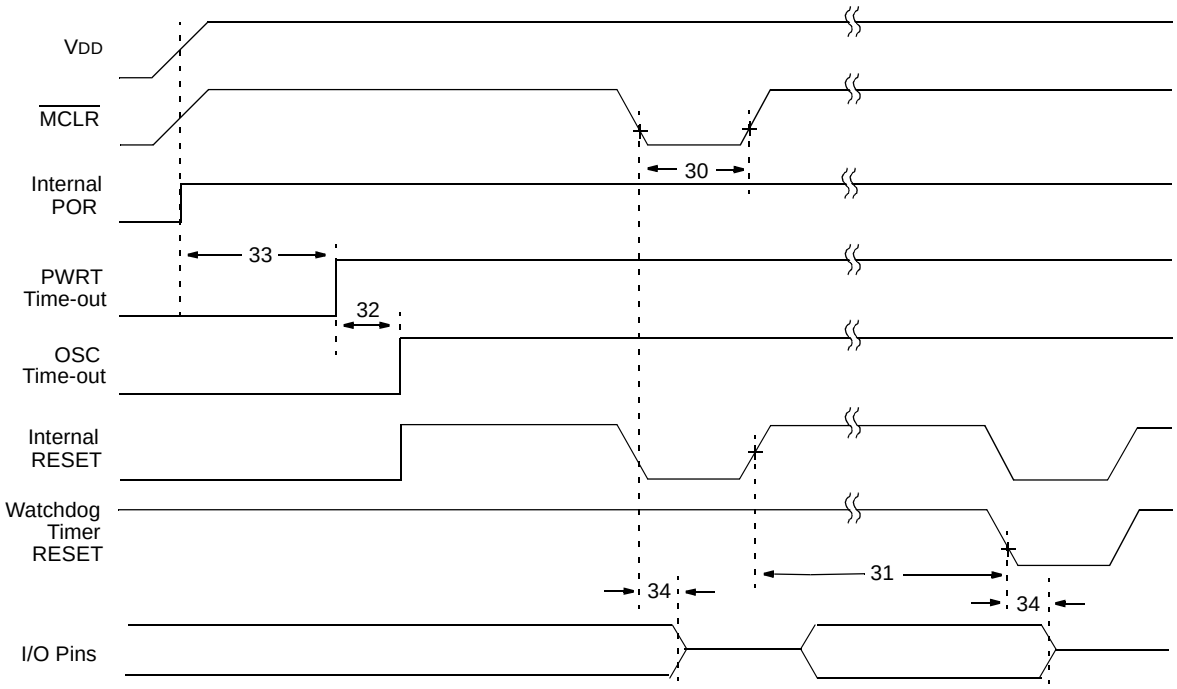
**TABLE 15-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC16C717/770/771 AND PIC16LC717/770/771**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>-40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended<br>Operating Voltage VDD range is described in Section and Section | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)*** | **Max** | **Units** | **Conditions** |
| | FIRC | Internal Calibrated RC Frequency | 3.65 | 4.00 | 4.28 | MHz | VDD = 5.0V |
| | | Internal RC Frequency* | 3.55 | 4.00 | 4.31 | MHz | VDD = 2.5V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 15-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




**Note:** Refer to Figure 15-4 for load conditions.

**FIGURE 15-8: BROWN-OUT RESET TIMING**

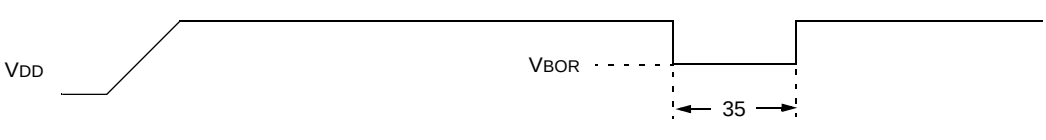


**TABLE 15-6: ENHANCED CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)**

| Param. No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1 input low time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**717/770/771 | 10 | — | — | ns | |
| | | | | PIC16**LC**717/770/771 | 20 | — | — | ns | |
| 51* | TccH | CCP1 input high time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**717/770/771 | 10 | — | — | ns | |
| | | | | PIC16**LC**717/770/771 | 20 | — | — | ns | |
| 52* | TccP | CCP1 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1, 4 or 16) |
| 53* | TccR | CCP1 output fall time | | PIC16**C**717/770/771 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**717/770/771 | — | 25 | 45 | ns | |
| 54* | TccF | CCP1 output fall time | | PIC16**C**717/770/771 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**717/770/771 | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 15.4 Analog Peripherals Characteristics: PIC16C717/770/771 & PIC16LC717/770/771 (Commercial, Industrial, Extended)

### 15.4.1 BANDGAP MODULE

**FIGURE 15-12: BANDGAP START-UP TIME**

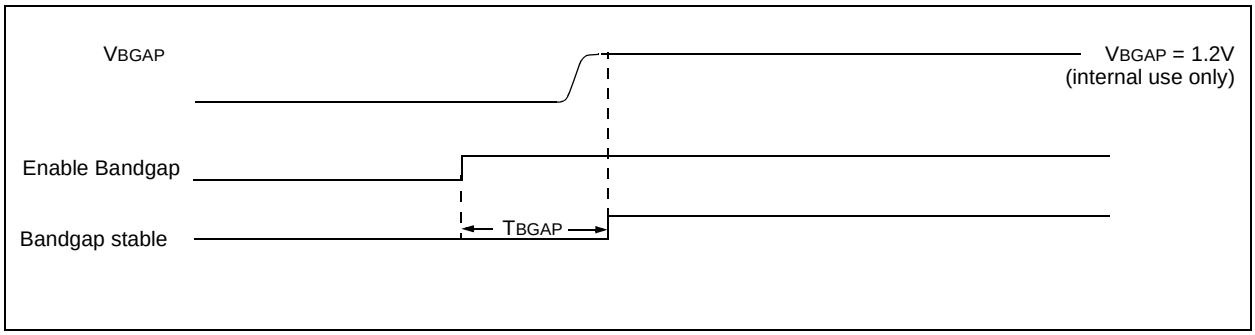



**TABLE 15-7: BANDGAP START-UP TIME**

| Param. No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 36* | TBGAP | Bandgap start-up time | — | 19 | 33 | μS | Defined as the time between the instant that the bandgap is enabled and the moment that the bandgap reference voltage is stable. |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 15-12: PIC16C770/771 AND PIC16LC770/771 A/D CONVERSION REQUIREMENTS (NORMAL MODE)**

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 130*(3) | TAD | A/D clock period | 1.6 | — | — | µs | Tosc based, VREF ≥ 2.5V |
| | | | 3.0 | — | — | µs | Tosc based, VREF full range |
| | | | | | | | ADCS<1:0> = 11 (A/D RC mode) |
| | | | 3.0 | 6.0 | 9.0 | µs | At VDD = 2.5V |
| | | | 2.0 | 4.0 | 6.0 | µs | At VDD = 5.0V |
| 131* | TCNV | Conversion time (not including acquisition time) **(Note 1)** | — | 13TAD | — | TAD | |
| 132* | TACQ | Acquisition Time | **Note 2** | 11.5 | — | µs | |
| | | | 5* | — | — | µs | The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 1mV @ 4.096V) from the last sampled voltage (as stated on CHOLD). |
| 134* | TGO | Q4 to A/D clock start | — | TOSC/2 | — | — | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

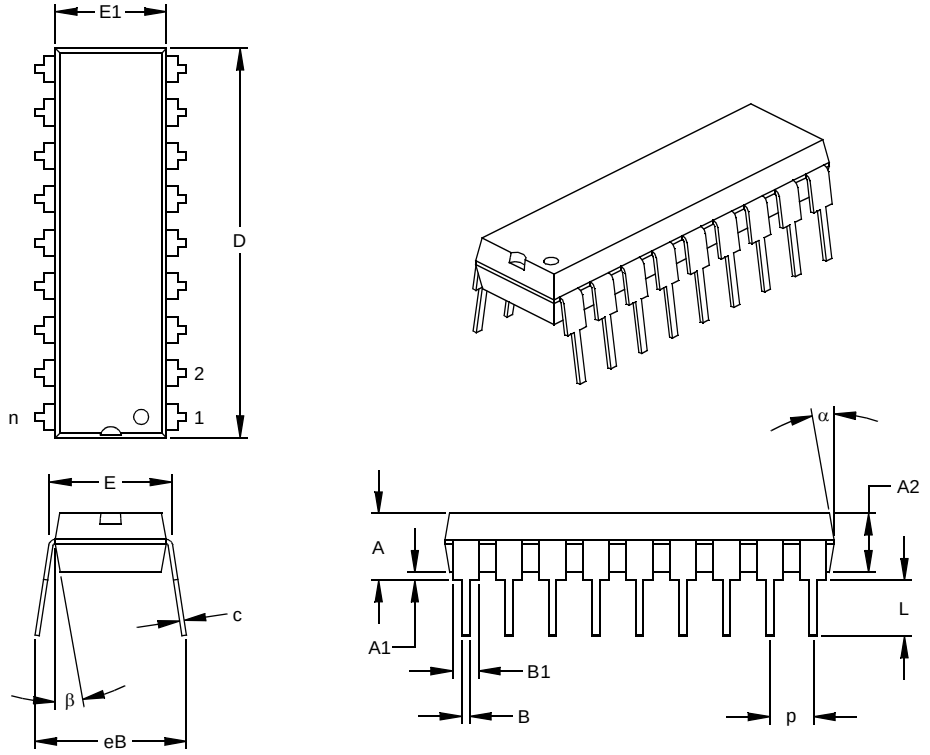
**Note 1:** ADRES register may be read on the following TCY cycle.

**2:** See Section 11.6 for minimum conditions.

**3:** These numbers multiplied by 8 if VRH or VRL is selected as A/D reference.

## 17.2 18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .890 | .898 | .905 | 22.61 | 22.80 | 22.99 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic

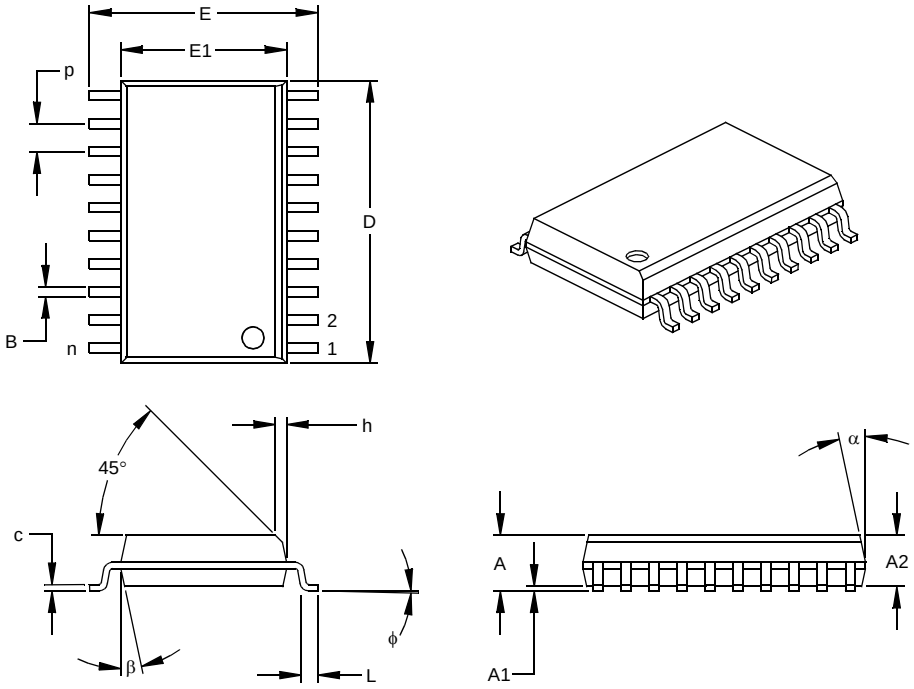
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

### 17.6 20-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

DRAWING NOT AVAILABLE

## 17.7 20-Lead Plastic Small Outline (SO) – Wide, 300 mi (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 20 | | | 20 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .291 | .295 | .299 | 7.39 | 7.49 | 7.59 |
| Overall Length | D | .496 | .504 | .512 | 12.60 | 12.80 | 13.00 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .013 | 0.23 | 0.28 | 0.33 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-094

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