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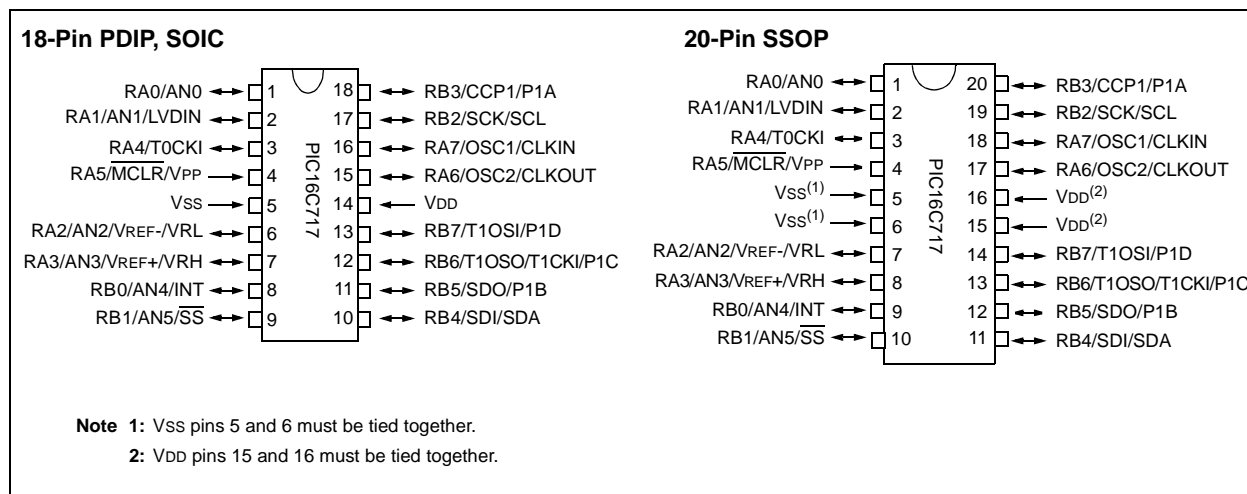
Applications of "**Embedded - Microcontrollers**"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc771t-e-so

PIC16C717/770/771

Pin Diagrams

18-Pin PDIP, SOIC

```
RA0/AN0          1   18   RB3/CCP1/P1A
RA1/AN1/LVDIN    2   17   RB2/SCK/SCL
RA4/T0CKI        3   16   RA7/OSC1/CLKIN
RA5/MCLR/VPP     4   15   RA6/OSC2/CLKOUT
VSS              5   14   VDD
RA2/AN2/VREF-/VRL 6  13   RB7/T1OSI/P1D
RA3/AN3/VREF+/VRH 7  12   RB6/T1OSO/T1CKI/P1C
RB0/AN4/INT      8   11   RB5/SDO/P1B
RB1/AN5/SS       9   10   RB4/SDI/SDA
```
PIC16C717

20-Pin SSOP

```
RA0/AN0           1   20   RB3/CCP1/P1A
RA1/AN1/LVDIN     2   19   RB2/SCK/SCL
RA4/T0CKI         3   18   RA7/OSC1/CLKIN
RA5/MCLR/VPP      4   17   RA6/OSC2/CLKOUT
VSS(1)            5   16   VDD(2)
VSS(1)            6   15   VDD(2)
RA2/AN2/VREF-/VRL 7  14   RB7/T1OSI/P1D
RA3/AN3/VREF+/VRH 8  13   RB6/T1OSO/T1CKI/P1C
RB0/AN4/INT       9   12   RB5/SDO/P1B
RB1/AN5/SS       10   11   RB4/SDI/SDA
```
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Note 1: VSS pins 5 and 6 must be tied together.
2: VDD pins 15 and 16 must be tied together.

Key Features PICmicro™ Mid-Range MCU Family Reference Manual, (DS33023)	PIC16C717	PIC16C770	PIC16C771
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR, MCLR, WDT (PWRT, OST)	POR, BOR, MCLR, WDT (PWRT, OST)	POR, BOR, MCLR, WDT (PWRT, OST)
Program Memory (14-bit words)	2K	2K	4K
Data Memory (bytes)	256	256	256
Interrupts	10	10	10
I/O Ports	Ports A,B	Ports A,B	Ports A,B
Timers	3	3	3
Enhanced Capture/Compare/PWM (ECCP) modules	1	1	1
Serial Communications	MSSP	MSSP	MSSP
12-bit Analog-to-Digital Module	—	6 input channels	6 input channels
10-bit Analog-to-Digital Module	6 input channels	—	—
Instruction Set	35 Instructions	35 Instructions	35 Instructions

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The special function registers can be classified into two sets; core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in that peripheral feature section.

TABLE 2-1: PIC16C717/770/771 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 0											
00h[3]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
01h	TMR0	Timer0 module's register								xxxx xxxx	45
02h[3]	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	22
03h[3]	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	14
04h[3]	FSR	Indirect data memory address pointer								xxxx xxxx	23
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	25
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xx11	33
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah[1,3]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	22
0Bh[3]	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	16
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0---0000	18
0Dh	PIR2	LVDIF	—	—	—	BCLIF	—	—	—	0--- 0---	20
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	47
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	47
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	47
11h	TMR2	Timer2 module's register								0000 0000	51
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	51
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	70
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	67
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	54
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	54
17h	CCP1CON	PWM1M1	PWM1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	53
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	A/D High Byte Result Register								xxxx xxxx	107
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON	0000 0000	107

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non Power-up) Resets include external RESET through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

3: These registers can be addressed from any bank.

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2.2.2.1   STATUS REGISTER

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit.   This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF,  BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

> **Note:** The C and DC bits operate as a borrow and digit borrow bit, respectively, in sub-traction. See the SUBLW and SUBWF instructions for examples.

REGISTER 2-1:   STATUS REGISTER (STATUS: 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

bit 7   bit 0

bit 7   **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h - 1FFh)
`0` = Bank 0, 1 (00h - FFh)

bit 6-5   **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h - 1FFh)
`10` = Bank 2 (100h - 17Fh)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4   **TO:** Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3   **PD:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2   **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1   **DC:** Digit carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for borrow the polarity is reversed)
`1` = A carry-out from the 4th low order bit of the result occurred
`0` = No carry-out from the 4th low order bit of the result

bit 0   **C:** Carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

> **Note:** For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF,  RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.2.2.4   PIE1 REGISTER

This register contains the individual enable bits for the peripheral interrupts.

> **Note:** Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

REGISTER 2-4:   PERIPHERAL INTERRUPT ENABLE REGISTER 1 (PIE1: 8Ch)

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE

bit 7   bit 0

bit 7   **Unimplemented:** Read as '0'

bit 6   **ADIE:** A/D Converter Interrupt Enable bit

1 = Enables the A/D interrupt
0 = Disables the A/D interrupt

bit 5-4   **Unimplemented:** Read as '0'

bit 3   **SSPIE:** Synchronous Serial Port Interrupt Enable bit

1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2   **CCP1IE:** CCP1 Interrupt Enable bit

1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1   **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit

1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0   **TMR1IE:** TMR1 Overflow Interrupt Enable bit

1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.2.2.5   PIR1 REGISTER

This register contains the individual flag bits for the peripheral interrupts.

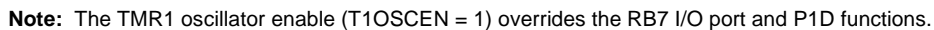| **Note:**	Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5:   PERIPHERAL INTERRUPT REGISTER 1 (PIR1: 0Ch)

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

bit 7   **Unimplemented:** Read as '0'.

bit 6   **ADIF:** A/D Converter Interrupt Flag bit

1 = An A/D conversion completed
0 = The A/D conversion is not complete

bit 5-4   **Unimplemented:** Read as '0'

bit 3   **SSPIF:** Synchronous Serial Port (SSP) Interrupt Flag

1 = The SSP interrupt condition has occurred, and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:
    SPI
        A transmission/reception has taken place.
    I^{2}C Slave / Master
        A transmission/reception has taken place.
    I^{2}C Master
        The initiated START condition was completed by the SSP module.
        The initiated STOP condition was completed by the SSP module.
        The initiated Restart condition was completed by the SSP module.
        The initiated Acknowledge condition was completed by the SSP module.
        A START condition occurred while the SSP module was IDLE (Multi-master system).
        A STOP condition occurred while the SSP module was IDLE (Multi-master system).
0 = No SSP interrupt condition has occurred.

bit 2   **CCP1IF:** CCP1 Interrupt Flag bit

Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1   **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0   **TMR1IF:** TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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FIGURE 3-10:   BLOCK DIAGRAM OF THE RB7/T1OSI/P1D

Note: The TMR1 oscillator enable (T1OSCEN = 1) overrides the RB7 I/O port and P1D functions.

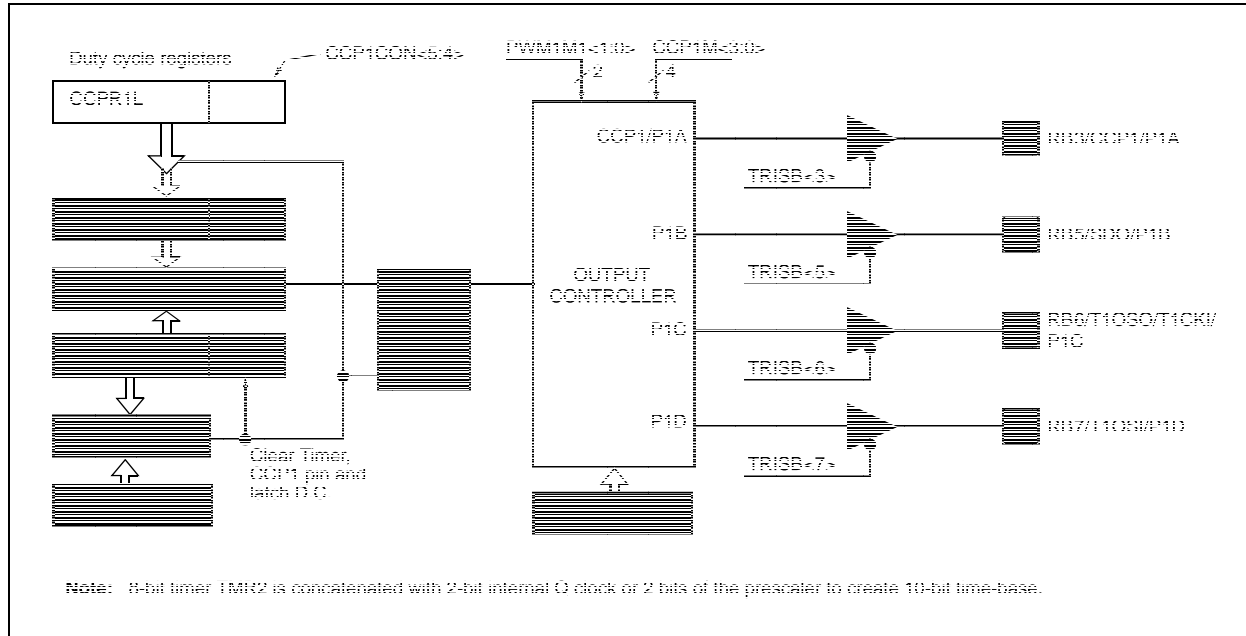## 8.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the ECCP module produces up to a 10-bit resolution PWM output. Figure 8-3 shows the simplified PWM block diagram.

FIGURE 8-3: **SIMPLIFIED PWM BLOCK DIAGRAM**

Note: 8-bit timer TMR2 is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base.

8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM PERIOD} = [(PR2) + 1] \bullet 4 \bullet \text{TOSC} \bullet (\text{TMR2 PRESCALE VALUE})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

> **Note:** The Timer2 postscaler (see Section 7.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

8.3.5 PROGRAMMABLE DEADBAND DELAY

In half-bridge or full-bridge applications, driven by half-bridge outputs (see Figure 8-7), the power switches normally require longer time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches will be on for a short period of time, until one switch completely turns off. During this time, a very high current, called shoot-through current, will flow through both power switches,

shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on the power switch is normally delayed to allow the other switch to completely turn off.

In the Half-Bridge Output mode, a digitally program-mable deadband delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 8-6 for illustration. The P1DEL register sets the amount of delay.

REGISTER 8-2: PWM DELAY REGISTER (P1DEL: 97H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1DEL7	P1DEL6	P1DEL5	P1DEL4	P1DEL3	P1DEL2	P1DEL1	P1DEL0

bit 7   bit 0

bit 7-0   **P1DEL<7:0>: PWM Delay Count for Half-Bridge Output Mode:** Number of $F_{OSC}/4$ ($T_{OSC} \cdot 4$) cycles between the P1A transition and the P1B transition.
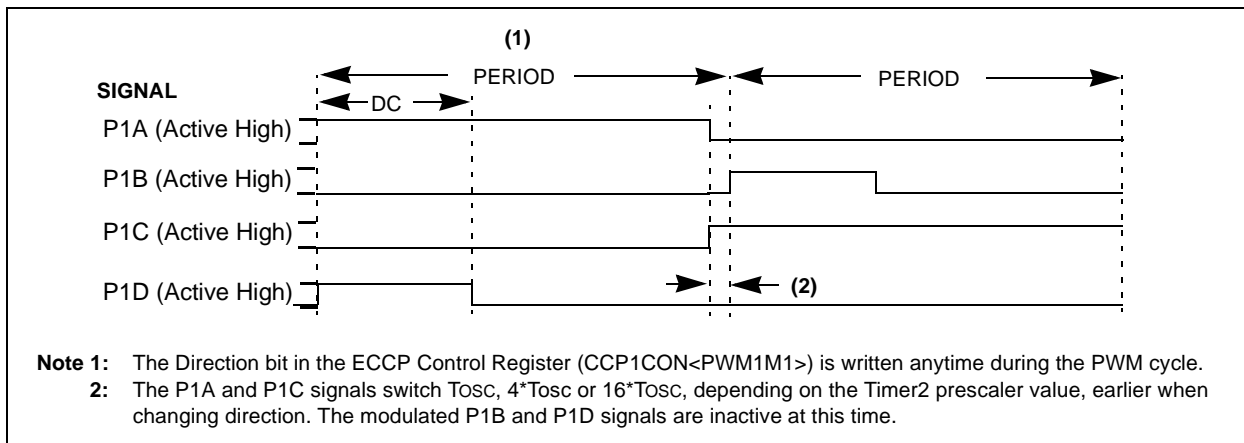
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

8.3.6 DIRECTION CHANGE IN FULL-BRIDGE OUTPUT MODE

In the Full-Bridge Output mode, the PWM1M1 bit in the CCP1CON register allows user to control the Forward/Reverse direction. When the application firmware changes this direction control bit, the ECCP module will assume the new direction on the next PWM cycle. The current PWM cycle still continues, however, the non-

modulated outputs, P1A and P1C signals, will transition to the new direction TOSC, 4•TOSC or 16•TOSC (for Timer2 prescale T2CKRS<1:0> = 00, 01 and 1x respectively) earlier, before the end of the period. During this transition cycle, the modulated outputs, P1B and P1D, will go to the inactive state. See Figure 8-10 for illustration.

FIGURE 8-10: PWM DIRECTION CHANGE

Note 1: The Direction bit in the ECCP Control Register (CCP1CON<PWM1M1>) is written anytime during the PWM cycle.
      2: The P1A and P1C signals switch TOSC, 4*Tosc or 16*TOSC, depending on the Timer2 prescaler value, earlier when changing direction. The modulated P1B and P1D signals are inactive at this time.

REGISTER 9-2:   SYNC SERIAL PORT CONTROL REGISTER (SSPCON: 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0

bit 7   bit 0

bit 7   **WCOL:** Write Collision Detect bit

<u>Master Mode:</u>

1 = A write to the SSPBUF register was attempted while the I^{2}C conditions were not valid for a transmission to be started

0 = No collision

<u>Slave Mode:</u>

1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)

0 = No collision

bit 6   **SSPOV:** Receive Overflow Indicator bit

<u>In SPI mode</u>

1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register. (Must be cleared in software).

0 = No overflow

<u>In I^{2}C mode</u>

1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode. (Must be cleared in software).

0 = No overflow

bit 5   **SSPEN:** Synchronous Serial Port Enable bit

In both modes, when enabled, the I/O pins must be properly configured as input or output.

<u>In SPI mode</u>

1 = Enables serial port and configures SCK, SDO, SDI, and $\overline{SS}$ as the source of the serial port pins

0 = Disables serial port and configures these pins as I/O port pins

<u>In I^{2}C mode</u>

1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins

0 = Disables serial port and configures these pins as I/O port pins

bit 4   **CKP:** Clock Polarity Select bit

<u>In SPI mode</u>

1 = IDLE state for clock is a high level

0 = IDLE state for clock is a low level

<u>In I^{2}C Slave mode SCK release control</u>

1 = Enable clock

0 = Holds clock low (clock stretch) (used to ensure data setup time)

<u>In I^{2}C Master mode</u>

Unused in this mode

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

9.2.7   MULTI-MASTER OPERATION

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET or when the MSSP module is disabled. Control of the I^{2}C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware, with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A START Condition
- A Repeated START Condition
- An Acknowledge Condition

Refer to Application Note AN578, *"Use of the SSP Module in the I^{2}C™ Multi-Master Environment."*

9.2.8   I^{2}C MASTER OPERATION

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON and by setting the SSPEN bit. Once Master mode is enabled, the user has six options.

1. Assert a START condition on SDA and SCL.
2. Assert a Repeated START condition on SDA and SCL.
3. Write to the SSPBUF register initiating transmission of data/address.
4. Generate a STOP condition on SDA and SCL.
5. Configure the I^{2}C port to receive data.
6. Generate an Acknowledge condition at the end of a received byte of data.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the I^{2}C bus will not be released.

| Note:	The MSSP Module, when configured in I^{2}C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a START condition and immediately write the SSPBUF register to initiate transmission before the START condition is complete. In this case, the SSPBUF will not be written to, and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

9.2.9   BAUD RATE GENERATOR

The baud rate generator used for SPI mode operation is used in the I^{2}C Master mode to set the SCL clock frequency. Standard SCL clock frequencies are 100 kHz, 400 kHz, and 1 MHz. One of these frequencies can be achieved by setting the SSPADD register to the appropriate number for the selected Fosc frequency. One half of the SCL period is equal to [(SSPADD+1) •2]/Fosc.

The baud rate generator reload value is contained in the lower seven bits of the SSPADD register (Figure 9-14). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload occurs. The BRG count is decremented twice per instruction cycle (T$_{CY}$) on the Q2 and Q4 clock.

In I^{2}C Master mode, the BRG is reloaded automatically provided that the SCL line is sampled high. For example, if Clock Arbitration is taking place, the BRG reload will be suppressed until the SCL line is released by the slave allowing the pin to float high (Figure 9-15).

FIGURE 9-14:   BAUD RATE GENERATOR BLOCK DIAGRAM
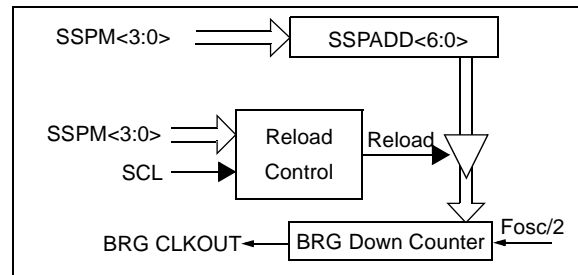
9.2.14   ACKNOWLEDGE SEQUENCE
TIMING

An Acknowledge sequence is enabled by setting the Acknowledge sequence enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit ACKDT (SSPCON2<5>) is presented on the SDA pin. If the user wishes to generate an Acknowledge ($\overline{ACK}$), then the ACKDT bit should be cleared. Otherwise, the user should set the ACKDT bit (NACK) before starting an Acknowledge sequence. The baud rate generator is then loaded from SSPADD<6:0> and counts for one rollover period (T$_{BRG}$). The SCL pin is then de-asserted (pulled high). When the SCL pin is sampled high (clock arbitration), the baud rate generator is reloaded and counts for another T$_{BRG}$. At the completion of the T$_{BRG}$ period, the following events occur (see Figure 9-20):

• The SCL pin is pulled low.
• The ACKEN bit is automatically cleared.
• The baud rate generator is turned off.
• The MSSP module goes into IDLE mode.

9.2.14.1   WCOL STATUS FLAG

If the user writes the SSPBUF when an Acknowledge sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 9-20:   ACKNOWLEDGE SEQUENCE WAVEFORM

Acknowledge sequence starts here,
Write to SSPCON2
ACKEN = 1, ACKDT = 0

ACKEN automatically cleared

T$_{BRG}$ T$_{BRG}$

SDA   D0 $\overline{ACK}$

SCL   8   9

SSPIF

SSPIF occurs at the end of receive

Cleared in software

Cleared in software

SSPIF occurs at the end of Acknowledge sequence

Note: T$_{BRG}$ = one baud rate generator period.
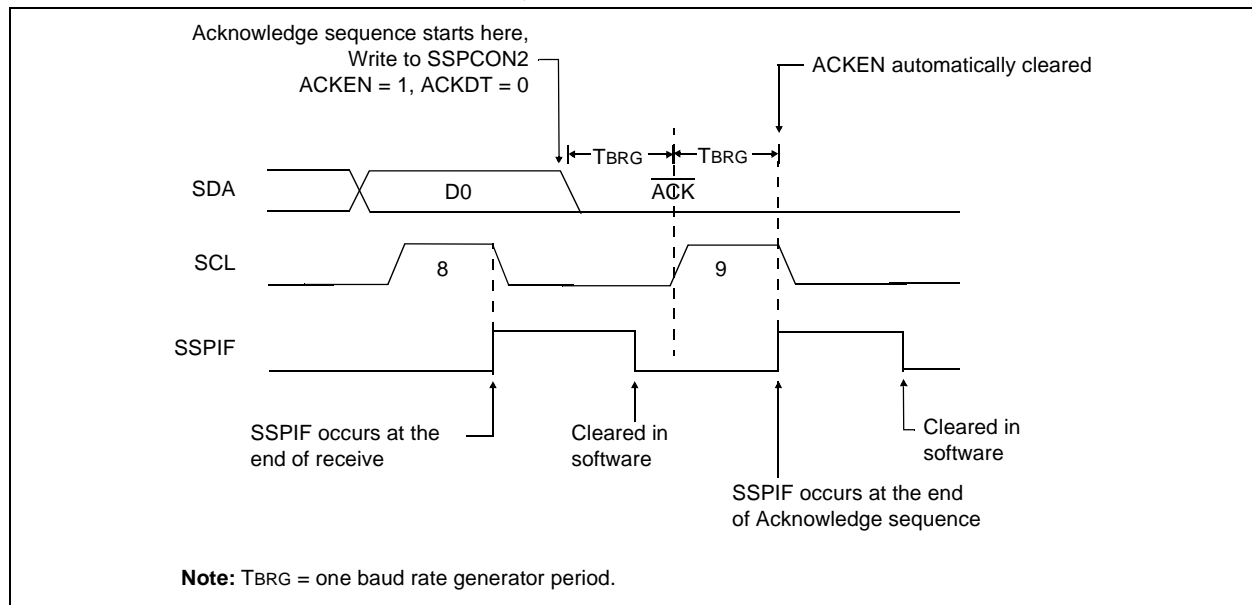
NOTES:

PIC16C717/770/771

10.1 Bandgap Voltage Reference

The bandgap module generates a stable voltage reference of over a range of temperatures and device supply voltages. This module is enabled anytime any of the following are enabled:

• Brown-out Reset
• Low-voltage Detect
• Either of the internal analog references (VRH, VRL)

Whenever the above are all disabled, the bandgap module is disabled and draws no current.

10.2 Internal VREF for A/D Converter

The bandgap output voltage is used to generate two stable references for the A/D converter module. These references are enabled in software to provide the user with the means to turn them on and off in order to minimize current consumption. Each reference can be individually enabled.

The VRH reference is enabled with control bit VRHEN (REFCON<7>). When this bit is set, the gain amplifier is enabled. After a specified start-up time a stable reference of 4.096V nominal is generated and can be used by the A/D converter as a reference input.

The VRL reference is enabled by setting control bit VRLEN (REFCON<6>). When this bit is set, the gain amplifier is enabled. After a specified start-up time a stable reference of 2.048V nominal is generated and can be used by the A/D converter as a reference input.

Each voltage reference is available for external use via VRL and VRH pins.

Each reference, if enabled, can be output on an external pin by setting the VRHOEN (high reference output enable) or VRLOEN (low reference output enable) control bit. If the reference is not enabled, the VRHOEN and VRLOEN bits will have no effect on the corresponding pin. The device specific pin can then be used as general purpose I/O.

> **Note:** If VRH or VRL is enabled and the other reference (VRL or VRH), the BOR, and the LVD modules are not enabled, the bandgap will require a start-up time before the bandgap reference is stable. Before using the internal VRH or VRL reference, ensure that the bandgap reference voltage is stable by monitoring the BGST bit in the LVD-CON register. The voltage references will not be reliable until the bandgap is stable as shown by BGST being set.

FIGURE 10-1: BLOCK DIAGRAM OF LVD AND VOLTAGE REFERENCE CIRCUIT
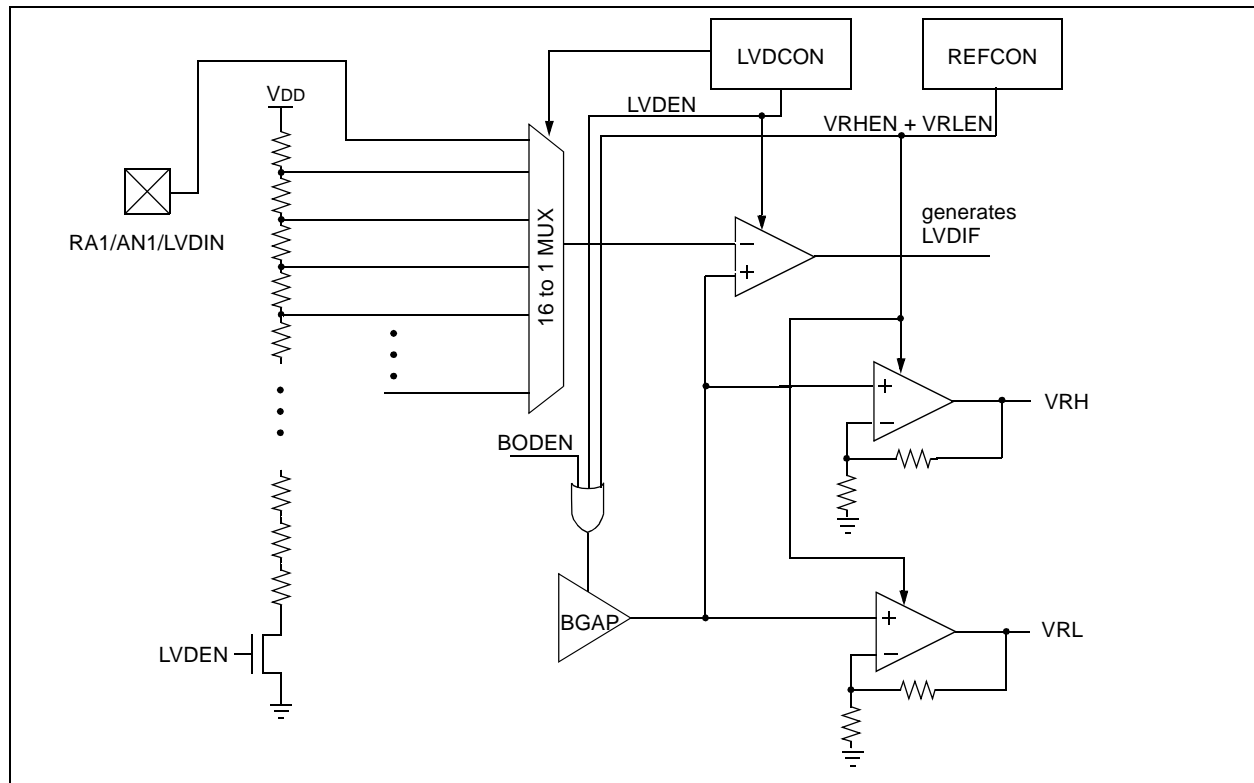
REGISTER 11-2: **A/D CONTROL REGISTER 1 (ADCON1: 9Fh)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG2	VCFG1	VCFG0	Reserved	Reserved	Reserved	Reserved

bit 7   bit 0

bit 7   **ADFM:** A/D Result Format Select bit
          `1` = Right justified
          `0` = Left justified

bit 6-4   **VCFG<2:0>:** Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
`000`	AVDD[(1)]	AVSS[(2)]
`001`	External VREF+	External VREF-
`010`	Internal VRH	Internal VRL
`011`	External VREF+	AVSS[(2)]
`100`	Internal VRH	AVSS[(2)]
`101`	AVDD[(1)]	External VREF-
`110`	AVDD[(1)]	Internal VRL
`111`	Internal VRL	AVSS

bit 3-0   **Reserved:** Do not use.

Note 1: This parameter is VDD for the PIC16C717.

2: This parameter is VSS for the PIC16C717.

| Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

The value that is in the ADRESH and ADRESL registers are not modified for a Power-on Reset. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

The A/D conversion results can be left justified (ADFM bit cleared), or right justified (ADFM bit set). Figure 11-1 through Figure 11-2 show the A/D result data format of the PIC16C717/770/771.

FIGURE 11-1: **PIC16C770/771 12-BIT A/D RESULT FORMATS**
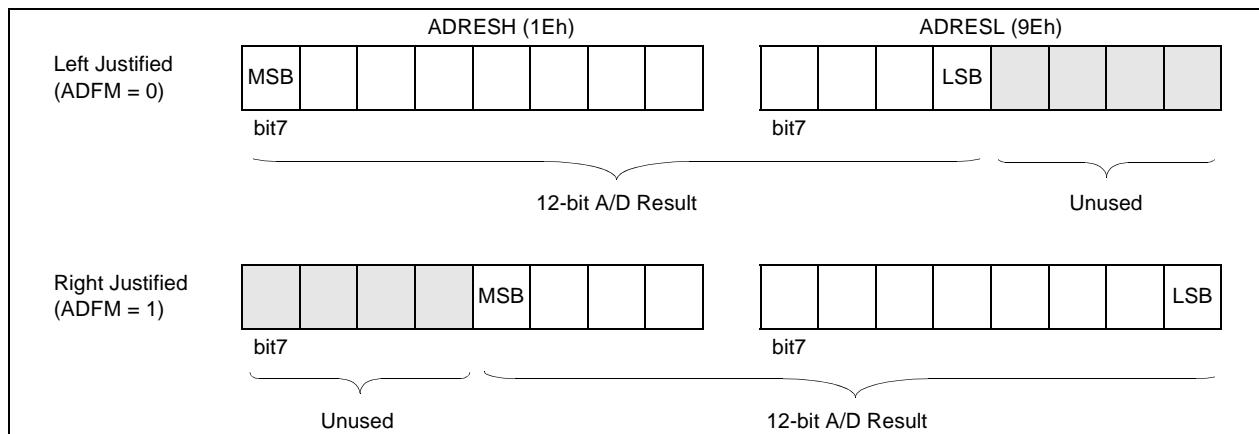
FIGURE 12-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1
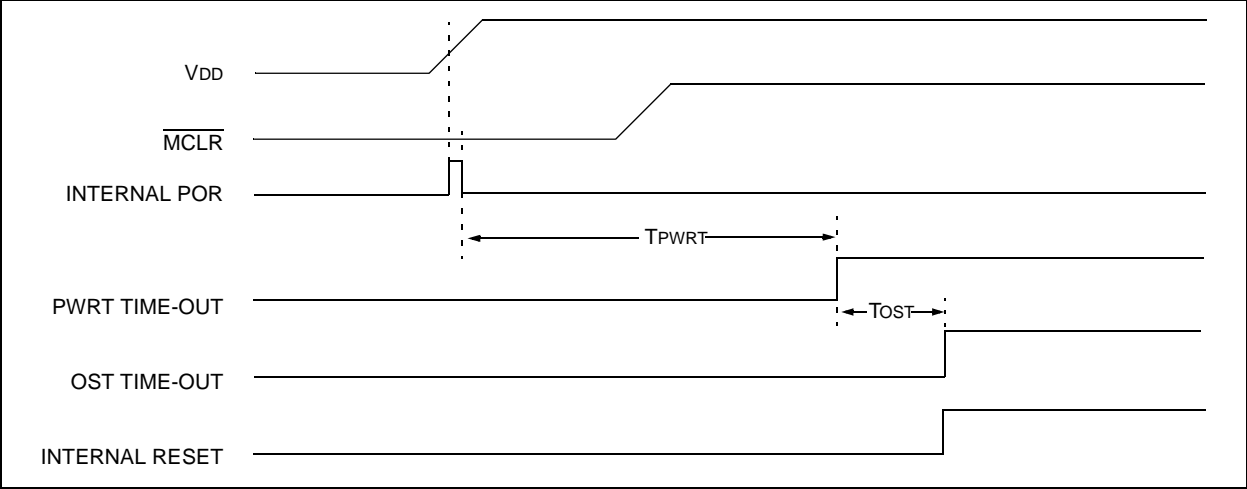
FIGURE 12-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2
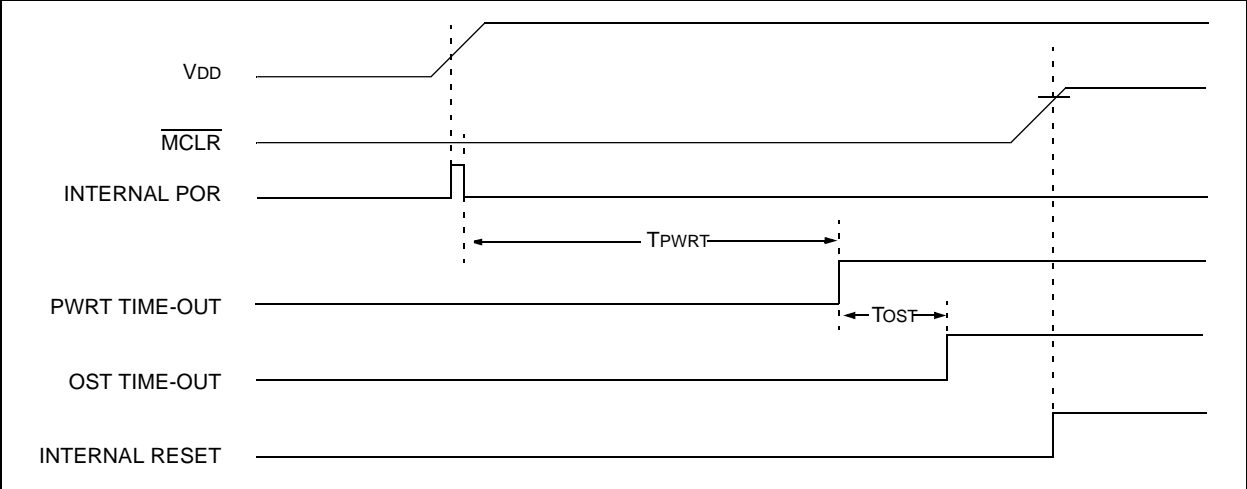
FIGURE 12-9: SLOW VDD RISE TIME (MCLR TIED TO VDD)

Note 1: Time dependent on oscillator circuit
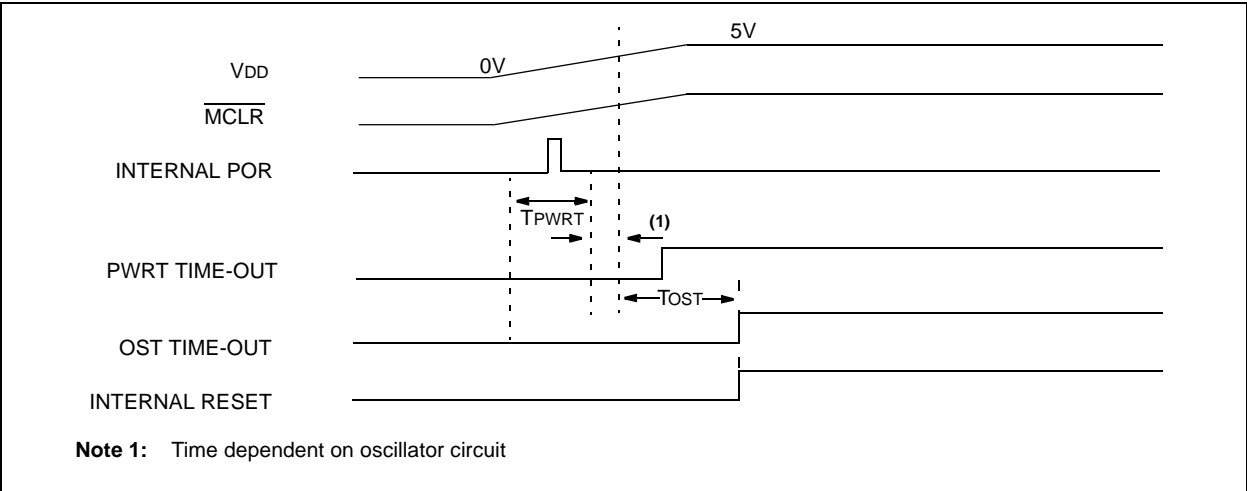
14.0   DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ® Demonstration Board

14.1   MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

14.2   MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

14.3   MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.
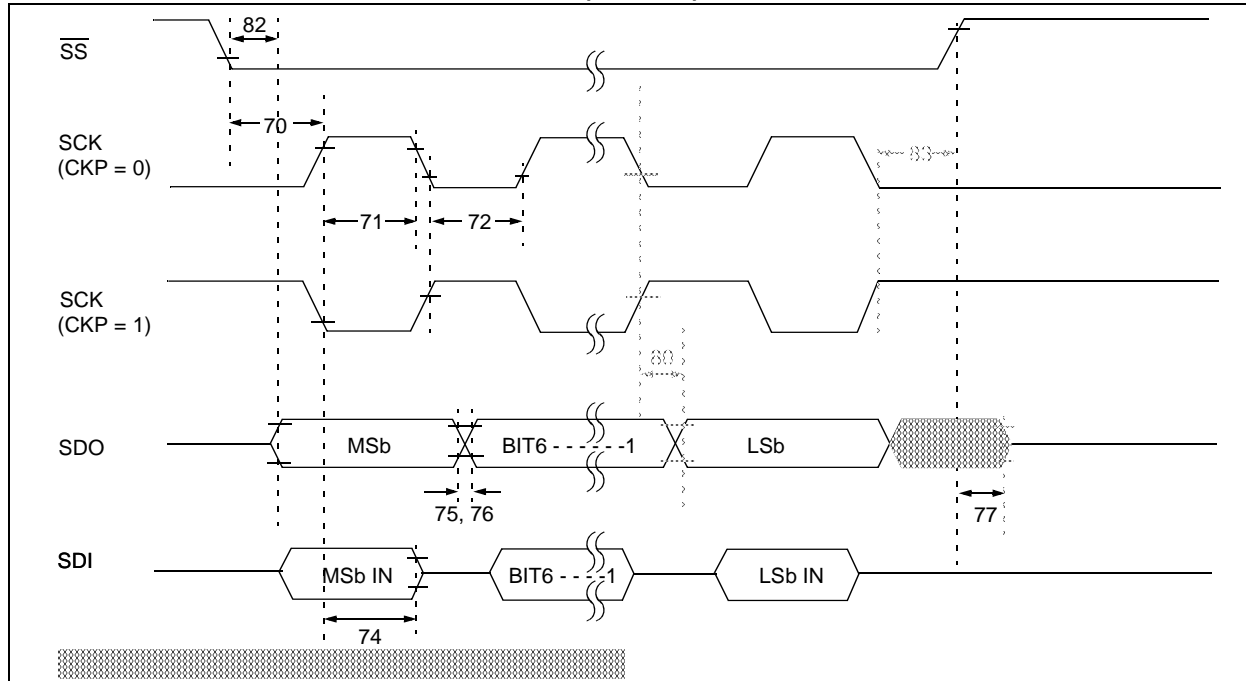
FIGURE 15-21: **SPI SLAVE MODE TIMING (CKE = 1)**

TABLE 15-20: SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input		TCY	—	—	ns	
71*	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A*			Single Byte	40	—	—	ns	**Note 1**
72*	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A*			Single Byte	40	—	—	ns	**Note 1**
73A*	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	**Note 1**
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75*	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
76*	TdoF	SDO data output fall time		—	10	25	ns	
77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output hi-impedance		10	—	50	ns	
78*	TscR	SCK output rise time (Master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX	—	20	45	ns	
79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX	—	—	100	ns	
82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX	—	—	100	ns	
83*	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge		1.5TCY + 40	—	—	ns	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1:   Specification 73A is only required if specifications 71A and 72A are used.

17.3   18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

**Note:**   For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
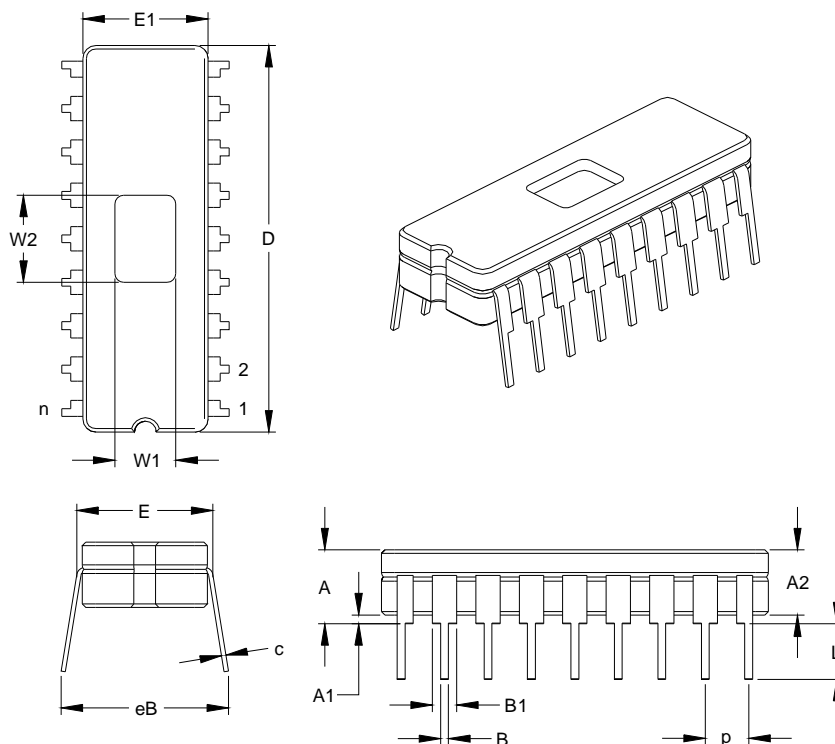
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

*Controlling Parameter
JEDEC Equivalent: MO-036
Drawing No. C04-010

17.5   20-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
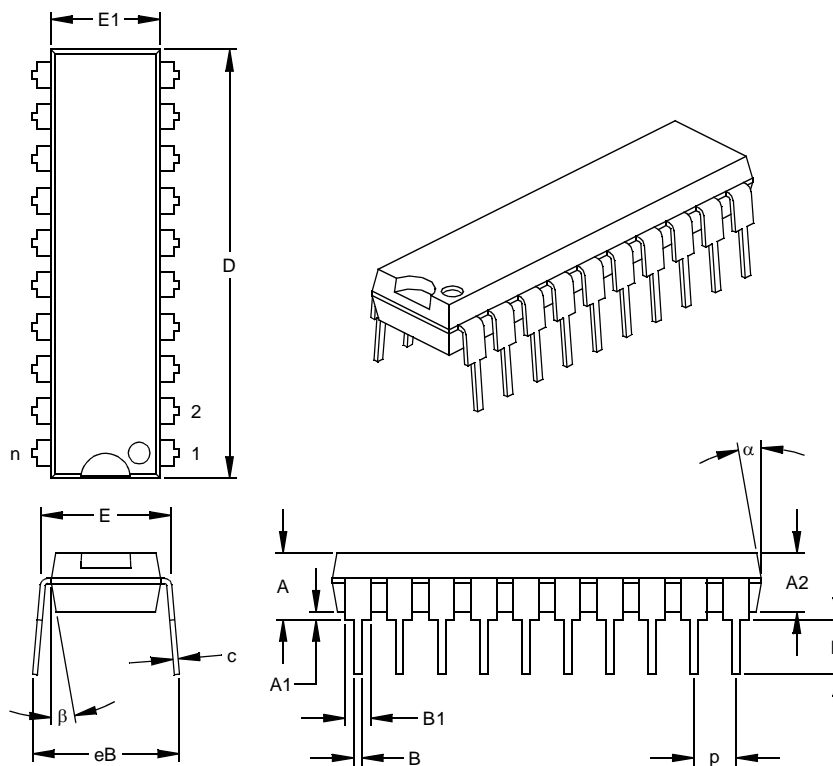
	Units		INCHES*			MILLIMETERS	
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-019

17.8   20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
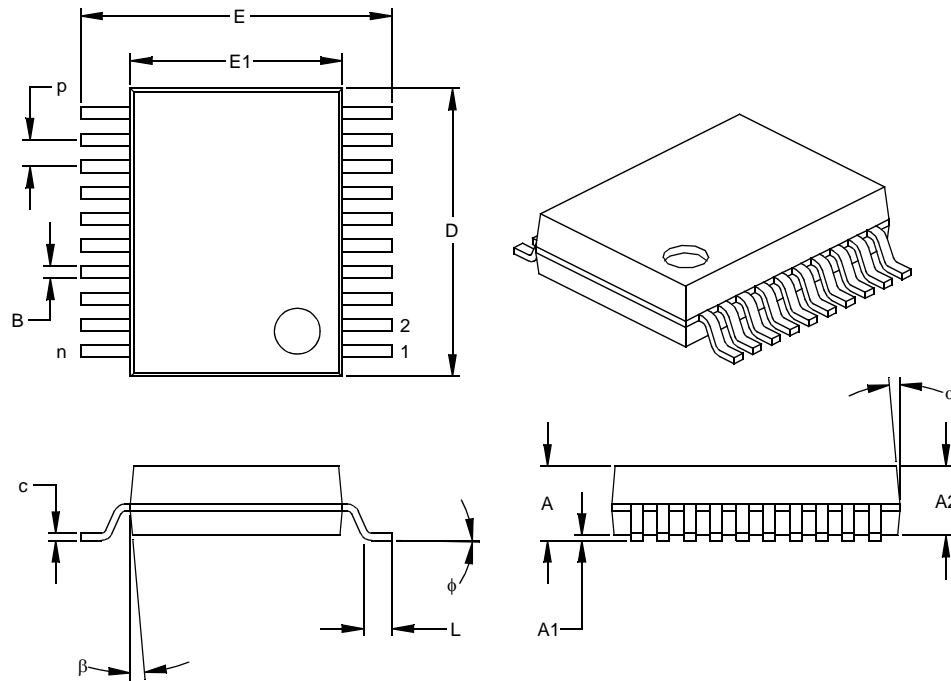
	Units	INCHES*			MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072