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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc771t-i-ss

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FIGURE 2-3: REGISTER FILE MAP

Indirect addr. ⁽¹⁾ 00h Indirect addr. ⁽¹⁾ 80h Indirect addr. ⁽¹⁾ 100h Indirect addr. ⁽¹⁾ 100h TMR0 01h OPTION.REG 81h TMR0 101h OPTION.REG 181h PCL 02h PCL 82h STATUS 103h FSR 04h FSR 84h FSR 104h FSR 184h PORTA 05h TRISA 85h 105h TRISB 186h O7h STATUS 86h 107h 186h 187h 06h TRISB 86h 107h 186h 187h 08h 89h 107h 186h 187h 188h 09h 89h 107h 188h 187h 188h PCLATH 0Ah PCLATH 8Ah PCLATH 10Ah PCLATH 188h PIR2 0Dh PIE1 8Ch PMDATL 10Dh 18Ch PIR2 0Dh PE14 8Ch PMADRL	A	File Address	A	File ddress		File Address	А	File Address
TMR0 01h OPTION_REG 81h TMR0 101h OPTION_REG 181h PCL 02h PCL 82h PCL 102h PCL 182h STATUS 03h STATUS 83h STATUS 103h STATUS 183h PORTA 05h TRISA 85h FSR 104h FSR 183h PORTB 06h TRISB 86h PORTB 106h TRISB 187h 08h 88h 107h 187h 188h 188h 09h PCLATH 8Ah PCLATH 108h 188h PORTB 06h ITRISB 86h PORTB 108h 188h PIR1 0Ch PIL 8Ch PMDATH 10Ch PRCON1 188h PIR2 0Ch PIE2 8Dh PMADRH 10Ch 186h TIMR1 0Fh SSPCON 8Fh PMADRH 10Fh 18Fh TIMR2	Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
PCL 02h PCL 82h PCL 102h PCL 182h STATUS 03h STATUS 83h STATUS 103h STATUS 183h FSR 04h FSR 84h FSR 104h FSR 184h PORTA 05h TRISB 86h PORTB 105h TRISB 186h PORTB 06h TRISB 86h PORTB 106h TRISB 188h 07h 87h 107h 187h 188h 188h PCLATH 0Ah PCLATH 8Ah PCLATH 10Ah PCLATH 188h PIR2 0Dh PIE2 8Dh PMDATH 10Ch 188h TMR1L 0Eh PCON 8Eh PMDATH 10Dh 18Ch TMR1H 0Fh SSPEON 8Fh PMADRH 10Fh 18Fh TMR2 11h SSPEON 90h 110h 190h 190h SSPE	TMR0	01h	OPTION REG	81h	TMR0	101h	OPTION REG	181h
STATUS 03h STATUS 83h STATUS 103h STATUS 183h FSR 04h FSR 84h FSR 104h FSR 184h PORTA 05h TRISA 85h 105h TRISB 185h ORH 06h TRISB 86h PORTB 107h 188h O7h 87h 107h 188h 187h 188h O8h 88h 108h 188h 188h O9h 89h 109h 188h 188h PCLATH 0Ah PCLATH 8Ah PCLATH 10Ah PRZ 0Dh PIE1 8Ch PMDATL 10Ch PMCON1 TMR1L 0Eh PCON 8Eh PMDATL 10Ch PMCON1 18Ch TMR1L 0Eh PCON 8Eh PMADRL 10Ch 190h 190h TMR2 11h SSPCON2 91h 111h 192h 192h 192h </td <td>PCL</td> <td>02h</td> <td>PCL</td> <td>82h</td> <td>PCL</td> <td>102h</td> <td>PCL</td> <td>182h</td>	PCL	02h	PCL	82h	PCL	102h	PCL	182h
FSR 04h FSR 84h FSR 104h FSR 184h PORTA 05h TRISA 85h 105h TRISB 186h PORTB 06h TRISB 86h PORTB 106h TRISB 186h 07h 87h 87h 107h 188h 187h 08h 88h 108h 188h 188h 09h 88h 108h 188h 09h 88h 108h 188h 1NTCON 08h NTCON 188h PIR1 0Ch PIE1 8Ch PMDATL 10Ch PMCON1 1RTCON 08h INTCON 8Bh PMADRL 10Dh 18Dh TMR1L 0Ch PIE2 8Dh PMADRH 10Ch 18Ch TTCON 10h SPCON2 91h 111h 192h 192h SSPBUF 13h SSPCON 14h SSPAD 93h 113h 193h	STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
PORTA 05h TRISA 85h 105h 105h 185h PORTB 06h TRISB 86h PORTB 106h TRISB 186h 07h 87h 107h 87h 107h 187h 08h 88h 108h 118h 188h 09h 89h 109h 188h 09h 89h 109h 188h 09h 89h 109h 188h 09h 89h 107N 18h 1NTCON 08h INTCON 18h PIR2 0Dh PIE2 8Dh PMDATL 100h PIR2 0Dh PIE2 8Dh PMDATL 100h 18bh TMR1H 0Fh PCN 8Fh PMDATL 100h 18bh TMR2 11h SSPCON2 91h 112h 192h SSPBUF 13h SSPSDON 14h SSPSDON 14h SSPSDON 18h <td< td=""><td>FSR</td><td>04h</td><td>FSR</td><td>84h</td><td>FSR</td><td>104h</td><td>FSR</td><td>184h</td></td<>	FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTB 06h TRISB 86h PORTB 106h TRISB 186h 07h 87h 87h 107h 187h 187h 08h 88h 109h 188h 188h 09h 88h 109h 188h PCLATH 0Ah PCLATH 8Ah PCLATH 10Ah PIR1 0Ch PIE1 8Ch PMDATL 10Ch PMCONI PIR1 0Ch PIE2 8Ch PMDATL 10Ch PMCONI 18Ch TIMR1L 0Ch PIE2 8Ch PMDATL 10Ch 18Ch TMR1H 0Ch PR2 9Ch 111h 190h 190h TIMR2 11h SSPCON2 91h 111h 191h 191h TZCON 12h PR2 92h 112h 192h 192h SSPBUF 13h SSPADD 93h 1113h 193h 193h CCPR1H 16h IOCB </td <td>PORTA</td> <td>05h</td> <td>TRISA</td> <td>85h</td> <td></td> <td>105h</td> <td></td> <td>185h</td>	PORTA	05h	TRISA	85h		105h		185h
O7h B87h 107h 187h 08h 88h 88h 108h 188h 09h 88h 88h 108h 188h PCLATH 0Ah PCLATH 8Ah 109h 188h PIR1 0Ch PIE1 8Ch PMDATL 100h PMCON1 PIR2 0Dh PIE2 8Dh PMDATL 10Dh PMCON1 TMR1L 0Eh PCON 8Eh PMDATH 10Eh 18Eh TMR1H 0Fh 8Eh PMDATH 10Eh 18Eh TMR2 11h SSPCON2 91h 111h 191h TMR2 11h SSPSTAT 94h 112h 192h SSPEUF 13h SSPSTAT 94h 118h 198h CCPR1L 15h WPUB 95h 115h 197h 19h 99h 111h 197h 197h 197h 19h 99h 1115h 198h	PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
O8h B8h 108h 188h O9h 88h 89h 109h 188h PCLATH 0Ah PCLATH 8Ah PCLATH 10Ah PCLATH INTCON 0Bh INTCON 8Bh INTCON 10Bh INTCON 18Bh PIR1 0Ch PIE1 8Ch PMDATL 10Ch PMCONI 18Ch PIR2 0Dh PIE2 8Dh PMDATL 10Dh 18Ch TMR1L 0Eh PCON 8Eh PMDATH 10Eh 18Ch TMR2 11h SSPCON2 91h 1110h 190h TMR2 11h SSPCON2 91h 1112h 192h SSPEON 13h SSPADD 93h 113h 193h CCPR1L 15h WPUB 95h 1116h 196h CCPR1H 16h IOCB 96h 1117h 197h 19h 99h 1117h 199h 199h		07h		87h		107h		187h
O9h O9h PCLATH 89h 109h 189h PCLATH 0Ah PCLATH 8Ah PCLATH 10Ah PCLATH 18Ah INTCON 0Bh INTCON 8Ah PCLATH 10Ah PCLATH 18Ah PIR1 0Ch PIE1 8Ch PMDATL 10Ch PMCONI 18Bh TMR1L 0Eh PCON 8Eh PMDATL 10Dh 18Ch TMR1H 0Fh BSPCON 8Eh PMADRH 10Fh 18Eh TMR1H 0Fh SSPCON2 91h 110h 190h 190h TCCON 12h PR2 92h 112h 192h 192h SSPBUF 13h SSPCON2 94h 114h 194h 193h CCPR1L 15h WPUB 95h 115h 192h 192h CCPR1L 16h IOCB 96h 117h 197h 197h 19h 99h 117h		08h		88h		108h		188h
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INTCON 0Bh INTCON 8Bh INTCON 10Bh INTCON 18Bh PIR1 0Ch PIE1 8Ch PMDATL 10Ch PMCON1 18Ch PIR2 0Dh PIE2 8Dh PMDATL 10Dh 18Dh TMR1L 0Eh PCON 8Eh PMDATL 10Dh 18Dh TMR1H 0Fh BFh PMDATL 10Dh 18Dh 18Dh TMR1L 0Fh BFh PMADRH 10Fh 18Fh 18Fh TICON 10h 90h 111h 190h 190h 190h TMR2 11h SSPCON2 91h 111h 191h 191h SSPEON 14h SSPSTAT 94h 111h 192h 193h SSPCON 14h SSPSTAT 94h 114h 194h 194h CCPR1L 15h WPUB 95h 115h 195h 197h General 19h 99h	PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
PIR1 OCh PIE1 8Ch PMDATL 10Ch PMCON1 18Ch PIR2 0Dh PIE2 8Dh PMADRL 10Dh 18Dh 18Dh TMR1L 0Eh PCON 8Eh PMDATH 10Eh 18Dh TMR1H 0Fh 8Fh PMADRH 10Fh 18Fh TMR2 11h SSPCON2 91h 110h 190h TZCON 12h PR2 92h 112h 192h SSPBUF 13h SSPADD 93h 113h 193h SSPCON 14h SSPSTAT 94h 114h 194h CCPR1L 15h WPUB 95h 115h 195h CCPR1H 16h IOCB 96h 117h 197h 18h 98h 117h 197h 197h 19h 99h 117h 197h 197h 10h ANSEL 92h 117h 198h 10h	INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR2 ODh PIE2 8Dh PMADRL 10Dh 18Dh TMR1L 0Eh PCON 8Eh PMDATH 10Eh 18Eh TMR1H 0Fh 8Fh PMADRH 10Fh 18Eh TICON 10h 90h 110h 19Ph TICON 10h 90h 110h 19Ph TICON 10h SSPCON2 91h 111h 19Ph SSPBUF 13h SSPCON2 91h 112h 192h SSPBUF 13h SSPADD 93h 113h 193h SSPCON 14h SSPSTAT 94h 114h 194h CCPR1L 15h WPUB 95h 115h 195h CCPR1H 16h IOCB 96h 116h 196h CCP1CON 17h P1DEL 97h 117h 197h 19h 99h 1118h 199h 199h 199h 10h ANSEL 9Ah </td <td>PIR1</td> <td>0Ch</td> <td>PIE1</td> <td>8Ch</td> <td>PMDATL</td> <td>10Ch</td> <td>PMCON1</td> <td>18Ch</td>	PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
TMR1L OEh PCON 8Eh PMDATH 10Eh 18Eh TMR1H OFh 8Fh PMADRH 10Fh 18Fh TMR2 11h SSPCON2 91h 110h 190h TZCON 12h PR2 92h 112h 192h SSPBUF 13h SSPADD 93h 113h 193h SSPEON 14h SSPSTAT 94h 114h 194h CCPR1L 15h WPUB 95h 115h 195h CCPR1H 16h IOCB 96h 116h 196h CCP1CON 17h P1DEL 97h 117h 197h 18h 98h 118h 198h 198h 19h 99h 118h 199h 199h 10h ANSEL 9Dh 111h 192h 10h ANSEL 9Dh 11Dh 19Dh ADCON0 1Fh ADCON1 9Fh 11Ch 12Oh	PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh		18Dh
TMR1H OFh SFh PMADRH 10Fh 18Fh T1CON 10h 90h 91h 110h 190h TMR2 11h SSPCON2 91h 111h 191h T2CON 12h PR2 92h 112h 192h SSPBUF 13h SSPADD 93h 113h 193h SSPCON 14h SSPSTAT 94h 114h 194h CCPR1L 15h WPUB 95h 115h 195h CCPR1H 16h IOCB 96h 116h 196h CCP1CON 17h P1DEL 97h 117h 197h 18h 98h 91h 118h 198h 19h 99h 119h 19h 19h 19h 99h 111h 192h 1Ah 9Ah 111Ah 19Ah 19h 99h 111Ah 19h 19h 19h 9CO 110h 19Ch <td>TMR1L</td> <td>0Eh</td> <td>PCON</td> <td>8Eh</td> <td>PMDATH</td> <td>10Eh</td> <td></td> <td>18Eh</td>	TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh		18Eh
T1CON 10h 90h 110h 190h TMR2 11h SSPCON2 91h 111h 190h TZCON 12h PR2 92h 112h 192h SSPBUF 13h SSPADD 93h 113h 193h SSPCON 14h SSPSTAT 94h 114h 193h CCPR1L 15h WPUB 95h 115h 193h CCPR1H 16h IOCB 96h 116h 196h CCPR1H 16h IOCB 97h 117h 197h 18h 98h 118h 198h 199h 19h 99h 117h 197h 19h 99h 119h 199h 19h 99h 119h 199h 19h 99h 119h 199h 19h 99h 119h 199h 19h 99h 119h 19h 19h 90h 110h 19Ch	TMR1H	0Fh		8Fh	PMADRH	10Fh		18Fh
TMR2 11h SSPCON2 91h 111h 111h 191h TZCON 12h PR2 92h 112h 192h SSPBUF 13h SSPADD 93h 113h 193h SSPCON 14h SSPSTAT 94h 114h 194h CCPR1L 15h WPUB 95h 115h 194h CCPR1H 16h IOCB 96h 116h 196h CCP1CON 17h P1DEL 97h 117h 197h 18h 98h 91h 118h 198h 19h 99h 119h 199h 10h ANSEL 90h 110h 192h 10h ANSEL 90h 110h 192h 192h ADCON0 1Fh ADCON1 9Fh 1120h 140h 19Fh General Purpose Register 80 Bytes 120h 1A0h 1A0h General Purpose F6h	T1CON	10h		90h		110h		190h
T2CON 12h PR2 92h 112h 192h SSPBUF 13h SSPADD 93h 113h 193h SSPCON 14h SSPSTAT 94h 114h 193h CCPR1L 15h WPUB 95h 115h 193h CCPR1H 16h IOCB 96h 116h 196h CCPR1H 16h IOCB 96h 116h 196h CCP1CON 17h P1DEL 97h 117h 197h 18h 98h 118h 198h 199h 19h 99h 119h 199h 1Ah 9Ah 119h 199h 1Ah 9Ah 119h 199h 1Ah 9Ah 119h 199h 1Ah 9Ah 110h 192h 1Ah 9Ah 110h 192h 16h REFCON 9Ch 110h 19Dh 1Dh ADCON1 9Fh 110h	TMR2	11h	SSPCON2	91h		111h		191h
SSPBUF 13h SSPADD 93h 113h 193h SSPCON 14h SSPSTAT 94h 114h 194h CCPR1L 15h WPUB 95h 115h 194h CCPR1L 15h WPUB 95h 115h 194h CCPR1H 16h IOCB 96h 116h 199h CCP1CON 17h P1DEL 97h 117h 197h 18h 98h 118h 199h 199h 19h 99h 99h 119h 199h 1Ah 9Ah 118h 198h 19h 99h 99h 119h 199h 1Ah 9Ah 9Ah 11Ah 192h 15h LVDCON 9Ch 110h 192h 10h ANSEL 9Dh 11Dh 19Dh 19Dh ADCON0 1Fh ADCON1 9Fh 11Eh 19Fh 20h General Purpose <	T2CON	12h	PR2	92h		112h		192h
SSPCON 14h SSPSTAT 94h 114h 194h CCPR1L 15h WPUB 95h 115h 195h CCPR1H 16h IOCB 96h 116h 196h CCPR1ON 17h P1DEL 97h 117h 197h 18h 98h 98h 118h 198h 19h 99h 99h 119h 199h 1Ah 98h 118h 198h 19h 99h 99h 119h 199h 10h ANSEL 90h 118h 192h 10h ANSEL 90h 110h 192h ADRESH 1Eh ADRESL 9Eh 110h 192h ADCON0 1Fh ADCON1 9Fh 11Fh 19Fh 20h General Purpose Register 80 Bytes 140h 96 Bytes 7Fh A0h 120h 120h 140h A0h General Purpos	SSPBUF	13h	SSPADD	93h		113h	-	193h
CCPR1L 15h WPUB 95h 115h 195h CCPR1H 16h IOCB 96h 116h 196h CCP1CON 17h P1DEL 97h 117h 197h 18h 98h 118h 198h 198h 19h 99h 99h 119h 199h 10h Ah 98h 118h 198h 10h Ah 99h 119h 199h 10h ANSEL 90h 110h 19Ch ADRESH 1Eh ADRESL 90h 110h 19Ch ADCON0 1Fh ADCON1 9Fh 11Eh 19Fh ADCON0 1Fh ADCON1 9Fh 11Eh 19Fh A0h General Purpose Register 80 Bytes 14Oh 14Oh 96 Bytes Fh Fh 16Fh 1EFh 1FOh 70h-7Fh Fh Fh 17Oh acccesses 70h - 7Fh	SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1H16hIOCB96h116h196hCCP1CON17hP1DEL97h117h197h18h98h118h198h19h99h91h118h198h19h99h99h119h199h1Ah9Ah11Ah19Ah1BhREFCON9Bh118h19Bh1ChLVDCON9Ch11Ch19Ch1DhANSEL9Dh11Dh19DhADRESH1EhADRESL9Eh11EhADCON01FhADCON19Fh11Eh20hGeneral Purpose Register 80 BytesGeneral Purpose Register 80 Bytes16Fh96 Bytes7FhEFh16Fh7Fh7FhFFh17OhBank 0Bank 1Bank 2Bank 2	CCPR1L	15h	WPUB	95h		115h	-	195h
CCP1CON17hP1DEL97h117h117h197h18h18h98h98h118h198h19h19h99h119h199h1Ah9Ah9Ah11Ah19Ah1BhREFCON9Bh11Bh19Bh1ChLVDCON9Ch11Ch19Ch1DhANSEL9Dh11Dh19PhADRESH1EhADRESL9Eh11EhADCON01FhADCON19Fh11Fh20hGeneral Purpose RegisterSeneral Purpose Register16Fh96 BytesGeneral Purpose RegisterEFh F0h16Fh70h-7FhFFhFFh177hBank 07FhBank 1Bank 2	CCPR1H	16h	IOCB	96h		116h		196h
18h98h118h198h19h99h99h119h1Ah9Ah119h1Ah9Ah119h1BhREFCON9Bh1ChLVDCON1ChLVDCON1DhANSEL9Dh110hADRESH1EhADRESL9Eh1FhADCON120hGeneralPurposeRegister96 BytesGeneral7FhFPhADRESLFPh7FhFFhBank 0FFhBank 0FFhBank 0FFhBank 0FFhBank 1Bank 1	CCP1CON	17h	P1DEL	97h		117h		197h
19h99h119h199h1Ah9Ah9Ah119h199h1BhREFCON9Bh11Ah19Ah1ChLVDCON9Ch11Ch19Bh1DhANSEL9Dh11Ch19ChADRESH1EhADRESL9Eh11DhADCON01FhADCON19Fh11Fh20hGeneral Purpose Register20hAoh120h96 BytesFhEFh16Fh1EFh7Fh7FhFFhFFh17Dhaccesses 70h-7FhBank 07FhBank 1FFhBank 2Bank 2		18h		98h		118h		198h
1Ah9Ah11Ah19Ah1BhREFCON9Bh11Bh19Bh1ChLVDCON9Ch11Bh19Ch1DhANSEL9Dh11Ch19ChADRESH1EhADRESL9Eh11EhADCON01FhADCON19Fh11Fh20hGeneral Purpose Register 80 BytesA0h120h96 BytesFhEFh16Fh1Fh7FhRecesses 70h-7FhFFh16Fh1FhBank 0FFhFFh170haccesses 70h - 7Fh1FhBank 0Bank 1FFhBank 2Bank 2		19h		99h		119h		199h
1BhREFCON9Bh11Bh19Bh1ChLVDCON9Ch9Ch11Ch19Ch1DhANSEL9Dh11Dh19DhADRESH1EhADRESL9Eh11Eh19EhADCON01FhADCON19Fh11Fh19Fh20hCeneral Purpose Register 80 BytesA0h120h1A0hGeneral Purpose Register 80 BytesEFh F0h6eneral Purpose Register 80 Bytes16Fh 170h1EFh96 Bytes7FhFFhFFh F0h16Fh accesses 70h - 7Fh17Fh1FFhBank 07FhBank 1Bank 2Bank 2Bank 2Bank 2		1Ah		9Ah		11Ah		19Ah
IChLVDCON9Ch11Ch19Ch1DhANSEL9Dh11Dh19DhADRESH1EhADRESL9Eh11EhADCON01FhADCON19Fh11Fh20hA0hGeneral Purpose RegisterA0h120hGeneral Purpose RegisterGeneral Purpose RegisterGeneral Purpose RegisterGeneral Purpose Register16Fh96 Bytes7FhFPhFPh16Fh7Fh7FhFFhFPh17FhBank 07FhFFhFPh17FhBank 0FPhFPhFPh17FhBank 0FPhFPhFPh17FhBank 0FPhFPhFPhFPhBank 1FPhFPhFPhFPhFonFPhFP		1Bh	REFCON	9Bh		11Bh		19Bh
1DhANSEL9Dh11Dh19DhADRESH1EhADRESL9Eh11Eh19EhADCON01FhADCON19Fh11Fh19Fh20hA0hA0h120h120h1A0hGeneral Purpose Register 80 BytesGeneral Purpose Register 80 BytesGeneral Purpose Register 80 Bytes16Fh16Fh96 Bytes7Fh7FhFFhF0haccesses 70h-7Fh170hBank 07FhFFhFFh17Fh17FhBank 0FFhFFhFFh17Fh17Fh		1Ch	LVDCON	9Ch		11Ch		19Ch
ADRESH1EhADRESL9Eh11Eh11Eh19EhADCON01FhADCON19Fh11Fh11Fh19Fh20hA0hA0h120h1A0hGeneral Purpose Register 80 BytesGeneral Purpose Register 80 BytesGeneral Purpose Register 80 BytesGeneral Purpose Register 80 Bytes11Fh19Fh96 BytesF0hAccesses T0h-7FhEFh16Fh T0h - 7Fh1EFhBank 0FFhFFhT7h17Fh1FFh		1Dh	ANSEL	9Dh		11Dh		19Dh
ADCON01FhADCON19Fh11Fh19Fh20h20hA0hA0h120h140hGeneral Purpose RegisterGeneral Purpose RegisterGeneral Purpose Register120h1A0h96 BytesEFh6Bh16Fh16Fh96 Bytes7Fh7FhF0haccesses 70h-7Fh16FhBank 07FhBank 1Bank 2Bank 2	ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
20hA0h120h1A0hGeneral Purpose RegisterGeneral Purpose Register 80 BytesGeneral Purpose Register 80 Bytes120h1A0h96 BytesGeneral Purpose Register 80 BytesEFh F0h16Fh accesses 70h - 7Fh16Fh 170h1EFh accesses 70h - 7FhBank 0FFhFFh16Fh 170h - 7Fh1FhBank 0Bank 1Bank 2Bank 2Bank 2	ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose RegisterGeneral Purpose Register 80 BytesGeneral Purpose Register 80 BytesGeneral Purpose Register 80 BytesGeneral Purpose Register 80 BytesIEFh 16Fh 16Fh 170h1EFh accesses 70h - 7Fh96 Bytes7Fh7FhF0h F0haccesses 70h - 7Fh16Fh 170h16Fh accesses 70h - 7Fh16Fh 170hBank 07FhFFhFFh16Fh accesses 70h - 7Fh17Fh1FFh		20h		A0h		120h		1A0h
General Purpose Register Purpose Register Purpose Register Purpose Register Purpose Register 96 Bytes EFh 16Fh 1EFh 7Fh 7Fh F0h accesses 70h-7Fh 170h accesses 70h - 7Fh 170h Bank 0 Fh Bank 1 Bank 2 Bank 2 Bank 2			General		General			
Purpose Register Register Register 96 Bytes EFh 16Fh 96 Bytes F0h accesses 7Fh 7Fh FFh Bank 0 Bank 1 Bank 2	General		Purpose		Purpose			
Register 96 Bytes 80 Bytes 16Fh 1EFh 96 Bytes F0h accesses 170h accesses 1Fh 7Fh 7Fh FFh TFh 17Fh 17Fh	Purpose		Register		Register			
96 Bytes EFh 16Fh 16Fh 1EFh accesses F0h accesses 170h accesses 1F0h 7Fh 7Fh FFh FFh 17Fh 17Fh 1FFh	Register		OU Dytes		80 Bytes			
Bank 0 7Fh Accesses 70h-7Fh F0h FFh Accesses 70h - 7Fh 170h 70h - 7Fh accesses 70h - 7Fh 170h accesses 70h - 7Fh 1F0h Bank 0 Bank 1 Bank 2 17Fh 17Fh 1FFh	96 Bytes			EFh		16Fh		1EFh
Th Toh-7Fh Toh - 7Fh Toh - 7Fh Bank 0 7Fh Bank 1 Bank 2 17Fh 17Fh			accesses	F0h	accesses	170h	accesses	1F0h
Bank 0 Bank 1 Bank 2 Bank 2 Bank 2		75	70h-7Fh		70h - 7Fh		70h - 7Fh	
	Bank 0	/FN	Bank 1	FFN	Bank 2	17Fh	Bank 3	1FFh

Unimplemented data memory locations, read as '0'.
* Not a physical register.

2.2.2.1 STATUS REGISTER

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as $000u \ u1uu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note:	The C and DC bits operate as a borrow							
	and digit borrow bit, respectively, in sub-							
	traction. See the SUBLW and SUBWF							
	instructions for examples.							

REGISTER 2-1: STATUS REGISTER (STATUS: 03h, 83h, 103h, 183h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x		
	IRP	RP1	RP0	TO	PD	Z	DC	С		
	bit 7							bit 0		
bit 7	IRP: Register Bank Select bit (used for indirect addressing)									
	1 = Bank 2, 3 (100h - 1FFh)									
bit 6-5	RP<1:0>: 1	Register Bar	hk Select bit	s (used for c	lirect addres	ssina)				
	11 = Bank	3 (180h - 1F	FFh)			Joinig/				
	10 = Bank	2 (100h - 17	′Fh)							
	01 = Bank	1 (80h - FFh	ר) א							
	Each bank	is 128 bytes	1) S							
bit 4	TO: Time-c	out bit								
	1 = After po	ower-up, CL	RWDT instruc	ction, or SLE	EP instruction	on				
	0 = A WDT	time-out oc	curred							
bit 3	PD: Power	-down bit			_					
	1 = After po 0 = By exe	ower-up or b cution of the	e SLEEP inst	T instructio	n					
bit 2	Z: Zero bit									
	1 = The res	sult of an ari	thmetic or lo	gic operatio	n is zero					
1.11.4	0 = 1 he res	sult of an arr	thmetic or lo	gic operatio	n is not zero) 	// 			
bit 1	DC: Digit c is reversed	arry/borrow)	bit (ADDWF, 2	ADDLW,SUB	LW,SUBWF I	instructions)	(for borrow	the polarity		
	1 = A carry	-out from the	e 4th low ord	der bit of the	result occu	rred				
h it 0	0 = NO carl	ry-out from t	ne 4th Iow o	rder dit of tr						
DITU	\mathbf{L} : Carry/bo	orrow bit (AL	o Most Signi	, SUBLW , SU	JBWF INStruct	ctions)				
	0 = No carr	ry-out from t	he Most Sign	nificant bit of	f the result of	occurred				
			U							
	Note:	For borrow,	the polarity	is reversed.	A subtraction	on is execut	ted by addin	g the two's		
	(complement	of the seco	nd operand gh or low or	. ⊢or rotate der bit of the	(RRF, RLF source reg) instruction: ister.	s, this dit is		
			· · · · ·	,		0				
	Legend:									
	R = Reada	ble bit	W = W	ritable bit	U = Unim	nplemented	bit, read as	0'		
	- n = Value at POR $'1'$ = Bit is set $'0'$ = Bit is cleared x = Bit is unknown									

3.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

3.1 I/O Port Analog/Digital Mode

The PIC16C717/770/771 have two I/O ports: PORTA and PORTB. Some of these port pins are mixed-signal (can be digital or analog). When an analog signal is

present on a pin, the pin must be configured as an analog input to prevent unnecessary current draw from the power supply. The Analog Select Register (ANSEL) allows the user to individually select the Digital/Analog mode on these pins. When the Analog mode is active, the port pin will always read 0.

- **Note 1:** On a Power-on Reset, the ANSEL register configures these mixed-signal pins as Analog mode.
 - 2: If a pin is configured as Analog mode, the RA pin will always read '0' and RB pin will always read '1', even if the digital output is active.

REGISTER 3-1: ANALOG SELECT REGISTER (ANSEL: 9Dh)

| R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| — | — | ANS5 | ANS4 | ANS3 | ANS2 | ANS1 | ANS0 |
| bit 7 | | | | | | | bit 0 |

bit 7-6 **Reserved:** Do not use

0 = Digital I/O. Pin is assigned to port or special function.

1 = Analog Input. Pin is assigned as analog input.

Note: Setting a pin to an analog input disables the digital input buffer on the pin. The corresponding TRIS bit should be set to Input mode when using pins as analog inputs.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented b	oit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.2 PORTA and the TRISA Register

PORTA is a 8-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pins RA<3:0> are multiplexed with analog functions, such as analog inputs to the A/D converter, analog VREF inputs, and the onboard bandgap reference outputs. When the analog peripherals are using any of

these pins as analog input/output, the ANSEL register must have the proper value to individually select the Analog mode of the corresponding pins.

Note:	Upon RESET, the ANSEL register config-
	ures the RA<3:0> pins as analog inputs.
	All RA<3:0> pins will read as '0'.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output.

Pin RA5 is multiplexed with the device RESET (MCLR) and programming input (VPP) functions. The RA5/ MCLR/VPP input only pin has a Schmitt Trigger input buffer. All other RA port pins have Schmitt Trigger input buffers and full CMOS output buffers.

Pins RA6 and RA7 are multiplexed with the oscillator input and output functions.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

bit 5-0 **ANS<5:0>:** Analog Select between analog or digital function on pins AN<5:0>, respectively.

9.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI™)
- Inter-Integrated Circuit (I²C[™])

9.1.5 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

9.1.6 SLAVE SELECT SYNCHRONIZATION

The \overline{SS} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SS} pin control enabled (SSPCON<3:0> = 0100). The pin must not be driven low for the \overline{SS} pin to function as an input. TRISB<1> must be set. When the \overline{SS} pin is low, transmission and reception are enabled and the

SDO pin is driven. When the \overline{SS} pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/ pull-down resistors may be desirable, depending on the application.

- Note 1: When the SPI module is in Slave mode with SS pin control enabled, (SSP-CON<3:0> = 0100) the SPI module will RESET if the SS pin is set to VDD.
 - 2: If the SPI is used in Slave Mode with CKE = '1', then SS pin control must be enabled.

When the SPI module RESETS, the bit counter is forced to 0. This can be done by either forcing the SS pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.



FIGURE 9-4: SLAVE SYNCHRONIZATION WAVEFORM

PIC16C717/770/771



FIGURE 9-6: SPI SLAVE MODE WAVEFORM (CKE = 1)



9.2 MSSP I²C Operation

The MSSP module in I^2C mode fully implements all master and slave functions (including general call support) and provides interrupts on START and STOP bits in hardware to determine when the bus is free (multimaster function). The MSSP module implements the Standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used to transfer data. They are the SCL pin (clock) and the SDA pin (data). The MSSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>). The SCL and SDA pins are "glitch" filtered when operating as inputs. This filter functions in both the 100 kHz and 400 kHz modes. When these pins operate as outputs in the 100 kHz mode, there is a slew rate control of the pin that is independent of device frequency.

Before selecting any I^2C mode, the SCL and SDA pins must be programmed as inputs by setting the appropriate TRIS bits. This allows the MSSP module to configure and drive the I/O pins as required by the I^2C protocol.

The MSSP module has six registers for I^2C operation. They are listed below.

- SSP Control Register (SSPCON)
- SSP Control Register2 (SSPCON2)
- SSP STATUS Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows for control of the I^2C operation. Four mode selection bits (SSPCON<3:0>) configure the MSSP as any one of the following I^2C modes:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Master mode SCL Freq = FOSC / [4 • (SSPADD + 1)]
- I²C Slave mode with START and STOP interrupts (7-bit address)
- I²C Slave mode with START and STOP interrupts (10-bit address)
- Firmware Controlled Master mode

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START (S) or STOP (P) bit. It specifies whether the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer.

SSPBUF is the register to which the transfer data is written, and from which the transfer data is read. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled, buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is

transferred from the SSPSR register to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read a receiver overflow occurs, in which case, the SSPOV bit (SSPCON<6>) is set and the byte in the SSPSR is lost.

FIGURE 9-7: I²C SLAVE MODE BLOCK DIAGRAM



9.2.1 UPWARD COMPATIBILITY WITH SSP MODULE

The MSSP module includes three SSP modes of operation to maintain upward compatibility with the SSP module. These modes are:

- Firmware controlled Master mode (slave idle)
- 7-bit Slave mode with START and STOP condition interrupts.
- 10-bit Slave mode with START and STOP condition interrupts.

The firmware controlled Master mode enables the START and STOP condition interrupts but all other I²C functions are generated through firmware including:

- · Generating the START and STOP conditions
- · Generating the SCL clock
- Supplying the SDA bits in the proper time and phase relationship to the SCL signal.

In firmware controlled Master mode, the SCL and SDA lines are manipulated by clearing and setting the corresponding TRIS bits. The output level is always low irrespective of the value(s) in the PORT register. A '1' is output by setting the TRIS bit and a '0' is output by clearing the TRIS bit

The 7-bit and 10-bit Slave modes with START and STOP condition interrupts operate identically to the MSSP Slave modes except that START and STOP conditions generate SSPIF interrupts.

9.2.2.3 SLAVE RECEPTION

When the R/W bit of the address byte is clear (SSPSR<0> = 0) and an address match occurs, the R/ W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register on the falling edge of the eighth SCL pulse.

When the address <u>byte</u> overflow condition exists, then no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) or bit SSPOV (SSPCON<6>) is set. An MSSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the received byte.

Note: The SSPBUF will be loaded if the SSPOV bit is set and the BF flag is cleared. If a read of the SSPBUF was performed, but the user did not clear the state of the SSPOV bit before the next receive occurred, the ACK is not sent and the SSP-BUF is updated.

TABLE 9-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received			Concepto ACK	Set bit SSPIF	
BF	SSPOV	$SSPSR \to SSPBUF$	Pulse	(SSP Interrupt occurs if enabled)	
0	0	Yes	Yes	Yes	
1	0	No	No	Yes	
1	1	No	No	Yes	
0	1	Yes	No	Yes	

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

FIGURE 9-8: I²C SLAVE MODE WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



9.2.7 MULTI-MASTER OPERATION

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET or when the MSSP module is disabled. Control of the I²C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware, with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- · Address Transfer
- Data Transfer
- A START Condition
- A Repeated START Condition
- An Acknowledge Condition

Refer to Application Note AN578, "Use of the SSP Module in the l^2C^{TM} Multi-Master Environment."

9.2.8 I²C MASTER OPERATION

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON and by setting the SSPEN bit. Once Master mode is enabled, the user has six options.

- 1. Assert a START condition on SDA and SCL.
- 2. Assert a Repeated START condition on SDA and SCL.
- 3. Write to the SSPBUF register initiating transmission of data/address.
- 4. Generate a STOP condition on SDA and SCL.
- 5. Configure the I²C port to receive data.
- 6. Generate an Acknowledge condition at the end of a received byte of data.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the I^2C bus will not be released.

Note:	The MSSP Module, when configured in I^2C
	Master mode, does not allow queueing of
	events. For instance, the user is not
	allowed to initiate a START condition and
	immediately write the SSPBUF register to
	initiate transmission before the START
	condition is complete. In this case, the
	SSPBUF will not be written to, and the
	WCOL bit will be set, indicating that a write
	to the SSPBUF did not occur.

9.2.9 BAUD RATE GENERATOR

The baud rate generator used for SPI mode operation is used in the I²C Master mode to set the SCL clock frequency. Standard SCL clock frequencies are 100 kHz, 400 kHz, and 1 MHz. One of these frequencies can be achieved by setting the SSPADD register to the appropriate number for the selected Fosc frequency. One half of the SCL period is equal to [(SSPADD+1) \bullet 2]/Fosc.

The baud rate generator reload value is contained in the lower seven bits of the SSPADD register (Figure 9-14). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload occurs. The BRG count is decremented twice per instruction cycle (Tcr) on the Q2 and Q4 clock.

In I²C Master mode, the BRG is reloaded automatically provided that the SCL line is sampled high. For example, if Clock Arbitration is taking place, the BRG reload will be suppressed until the SCL line is released by the slave allowing the pin to float high (Figure 9-15).

FIGURE 9-14:

BAUD RATE GENERATOR BLOCK DIAGRAM



12.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when a VDD rise is detected (in the range of 1.5V - 2.1V). Enable the internal MCLR feature to eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details. For a long rise time, enable external MCLR function and use circuit as shown in Figure 12-5.

Two delay timers, (PWRT on OST), have been provided which hold the device in RESET after a POR (dependent upon device configuration) so that all operational parameters have been met prior to releasing the device to resume/begin normal operation.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions, or if necessary an external POR circuit may be implemented to delay end of RESET for as long as needed.





- Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
 - **2:** R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
 - **3:** $R1 = 100\Omega$ to $1 k\Omega$ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).
 - 4: External MCLR must be enabled (MCLRE = 1).

12.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed TPWRT time-out on power-up type RESETS only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the RESET condition (VDD rises above BOR trip point). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

12.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on a power-up type RESET or a wakeup from SLEEP.

12.7 Programmable Brown-Out Reset (PBOR)

The Programmable Brown-out Reset module is used to generate a RESET when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV<1:0> configuration word bits.

Configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below the specified trip point for longer than TBOR, (parameter #35), the brown-out situation will RESET the chip. A RESET may not occur if VDD falls below the trip point for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer will be invoked at that point and will keep the chip in RESET an additional TPWRT. If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will again begin a TPWRT time delay. Even though the PWRT is always enabled when brown-out is enabled, the PWRT configuration word bit should be cleared (enabled) when brown-out is enabled.

PIC16C717/770/771





FIGURE 15-2: PIC16LC717/770/771 VOLTAGE-FREQUENCY GRAPH, $0^{\circ}C \le TA \le +70^{\circ}C$



15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771				$\begin{array}{l lllllllllllllllllllllllllllllllllll$						
PIC16C717/770/771			Stand Opera	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions			
	Idd	Supply Current ⁽²⁾								
D010D D010E		PIC16LC7XX		1.0	2.0 3.0	mA	Fosc = 10 MHz, VDD = 3V, -40°C to 85°C Fosc = 10 MHz, VDD = 3V, -40°C to 125°C			
D010G				0.36	1.0	mA	Fosc = 4 MHz, Vdd = 2.5V, -40°C to 125°C			
D010K				11	45	μA	Fosc = 32 kHz, VDD = 2.5V, -40°C to 125°C			
	Idd	Supply Current ⁽²⁾								
D010 D010A		PIC16C7XX		4.0	7.5 12.0	mA	Fosc = 20 MHz, VDD = 5.5V, -40°C to 85°C Fosc = 20 MHz, VDD = 5.5V, -40°C to 125°C			
D010B D010C				2.5	5.0 6.0	mA	Fosc = 20 MHz, VDD = 4V, -40°C to 85°C Fosc = 20 MHz, VDD = 4V, -40°C to 125°C			
D010F				0.55	1.5	mA	Fosc = 4 MHz, VDD = 4V, -40°C to 125°C			
D010H D010J				30	80 95	μA	Fosc = 32 kHz, VDD = 4V, -40°C to 85°C Fosc = 32 kHz, VDD = 4V, -40°C to 125°C			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771		$\begin{array}{llllllllllllllllllllllllllllllllllll$								
PIC16C717/770/771			Stand Opera	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions			
		Base plus Module curren	ıt							
D021A	Iwdt	Watchdog Timer		2	10	μA	VDD = 3V, -40°C to 125°C			
D021	Iwdt	Watchdog Timer		5	20	μA	VDD = 4V, -40°C to 125°C			
D021	Iwdt	Watchdog Timer		5	20	μA	$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D025	IT10SC	Timer1 Oscillator		3	9	μA	VDD = 3V, -40°C to 125°C			
D025	IT10SC	Timer1 Oscillator		4	12	μA	$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D025	IT10SC	Timer1 Oscillator		4	12	μA	$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D026*	IAD	ADC Converter		300		μΑ	VDD = 5.5V, A/D on, not converting			
D026*	IAD	ADC Converter		300		μA	VDD = 5.5V, A/D on, not converting			
D027	IPLVD	Programmable Low		55	125	μΑ	$VDD = 4V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D027A		Voltage Detect			150		VDD = 4V, -40°C to 125°C			
D027	IPLVD	Programmable Low		55	125	μΑ	VDD = 4V, -40°C to 85°C			
D027A					150		$VDD = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D028	IPBOR	Programmable Brown-		55	125	μA	$VDD = 5V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D028A		out Reset			150		VDD = 5V, -40°C to 125°C			
D028	Ipbor	Programmable Brown-		55	125	μA	$VDD = 5V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D028A					150		$VDD = 5V, -40^{\circ}C$ to 125°C			
D029	IVRH	Voltage reference High		200	750 1.0	μA mA	$VDD = 5V, -40^{\circ}C$ to $85^{\circ}C$			
D029A	ly pu	Voltago reference High		200	750		VDD = 5V, -40 C to 125 C			
D029	IVRH	Voltage reference right		200	10	μA mA	$VDD = 5V, -40^{\circ}C$ to $125^{\circ}C$			
D030	IVRI	Voltage reference Low		200	750		$V_{DD} = 4V -40^{\circ}C$ to 85°C			
D030A		tenage reference Low		200	1.0	mA	$V_{DD} = 4V, -40^{\circ}C \text{ to } 125^{\circ}C$			
D030	Ivrl	Voltage reference Low		200	750	μA	$VDD = 4V, -40^{\circ}C \text{ to } 85^{\circ}C$			
D030A					1.0	mA	VDD = 4V, -40°C to 125°C			

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.2 DC Characteristics: PIC16C717/770/771 & PIC16LC717/770/771 (Commercial, Industrial, Extended)

			Standard Operating Conditions (unless otherwise stated)							
			Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial							
		FRISTICS	-40°C \leq TA \leq +85°C for industrial							
00011			-40°C \leq TA \leq +125°C for extended							
			Operating	voltage	e VDD ran	ige as	described in Section 15.1 and			
	-	• •••								
Param.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions			
NO.			-							
		Input Low Voltage								
	VIL	I/O ports	.,							
D030		with TTL buffer	Vss		0.15Vdd	V	For entire VDD range			
D030A			Vss		0.8V	V	$4.5V \le VDD \le 5.5V$			
D031		with Schmitt Trigger buffer	Vss		0.2Vdd	V	For entire VDD range			
D032		MCLR	Vss		0.2Vdd	V				
D033		OSC1 (in XT, HS, LP and EC)	Vss		0.3Vdd	V				
		Input High Voltage								
	Vін	I/O ports								
		with TTL buffer								
D040			2.0		Vdd	V	$4.5V \le VDD \le 5.5V$			
D040A			(0.25Vdd	—	Vdd	V	For entire VDD range			
			+ 0.8V)							
D041		with Schmitt Trigger buffer	0.8Vdd	—	Vdd	V	For entire VDD range			
D042		MCLR	0.8Vdd		Vdd	V				
D042A		OSC1 (XT, HS, LP and EC)	0.7Vdd	—	Vdd	V				
D070	IPURB	PORTB weak pull-up current	50	250	400	μA	VDD = 5V, VPIN = VSS			
		per pin								
		Input Leakage Current (1,2)								
D060	lı∟	I/O ports (with digital functions)	—		±1	μA	Vss \leq VPIN \leq VDD, Pin at hi-impedance			
D060A	lı∟	I/O ports (with analog func-	—		±100	nA	Vss \leq VPIN \leq VDD, Pin at hi-impedance			
Baad		tions)			. =					
D061		RA5/MCLR/VPP	_		±5	μA	VSS ≤ VPIN ≤ VDD			
D063		OSC1	—	_	±5	μA	Vss \leq VPIN \leq VDD, XI, HS, LP and EC			
		Quitmut Low Voltogo					osc conliguration			
080	Voi				0.6	V	$101 - 85 m^{1}$			
0000	VOL	Output High Voltago			0.0	v	10L = 8.5 MA, VDD = 4.5 V			
	√оц		Vpp - 0 7			V	104 - 30 mA VDD - 45 V			
D030	Von	I/O ports	VDD - 0.1		10.5	V	$\mathbf{D}\mathbf{A}\mathbf{a}$ in			
D150"	VOD	Open Drain High Voltage		_	10.5	V	RA4 pin			
		Capacitive Loading Specs on Output Pine*								
D100	202				15	ъĘ	In XT HS and I B modes when exter			
0100	CO3	0302 pm	_		15	pΓ	nal clock is used to drive OSC1			
D101	Cio	All I/O pins and OSC2 (in RC	_		50	рF				
D102	Св	mode) SCL SDA in L^2 C mode			400	pF				
		Vel nin			200	~~ ~ E				
					200	рг г				
	OVRL	VKL PIII			200	рг				

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.



TABLE 15-19: SPI MODE REQUIREMENTS (SLAVE MODE TIMING (CKE = 0)

Param. No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow input		Тсү	_	_	ns	
71*	TscH	SCK input high time	Continuous	1.25Tcy + 30	—	_	ns	
71A*		(Slave mode)	Single Byte	40	—	_	ns	Note 1
72*	TscL	SCK input low time	Continuous	1.25Tcy + 30	-	_	ns	
72A*		(Slave mode)	Single Byte	40	-	-	ns	Note 1
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to	100	_	_	ns		
73A*	Тв2в	Last clock edge of Byte1 to the of Byte2	1.5Tcy + 40	-	—	ns	Note 1	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to	100	_	_	ns		
75*	TdoR	SDO data output rise time	PIC16CXXX		10	25	ns	
			PIC16LCXXX		20	45	ns	
76*	TdoF	SDO data output fall time		_	10	25	ns	
77*	TssH2doZ	SS [↑] to SDO output hi-impedance		10	_	50	ns	
78*	TscR	SCK output rise time (Master	PIC16 C XXX	_	10	25	ns	
		mode)	PIC16LCXXX		20	45	ns	
79*	TscF	SCK output fall time (Master mode)		_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after	PIC16 C XXX	_	-	50	ns	
		SCK edge	PIC16LCXXX		_	100	ns	
83*	TscH2ssH, TscL2ssH	SS ↑ after SCK edge		1.5Tcy + 40	_	_	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

15.6 Master SSP I²C Mode Timing Waveforms and Requirements



FIGURE 15-22: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS

TABLE 15-21: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Тур	Max	Units	Conditions	
90*	TSU:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)	—	—		Only relevant for a Repeated	
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	—	_	ns	START	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—			condition	
91*	THD:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)	—	_		After this period the first clock	
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	—	—	ns	pulse is generated	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—				
92*	Tsu:sto	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	—	—			
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	—	—	ns		
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	—			
93*	THD:STO	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	—	_			
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	—	_	ns		
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—				

 * These parameters are characterized but not tested. For the value required by the I²C specification, please refer to the PICmicroTM Mid-Range MCU Family Reference Manual (DS33023).
Maximum pin capacitance = 10 pF for all I²C pins.







FIGURE 16-12: MAXIMUM IDD VS. VDD (INTRC 37 kHZ MODE)





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W

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NOTES: