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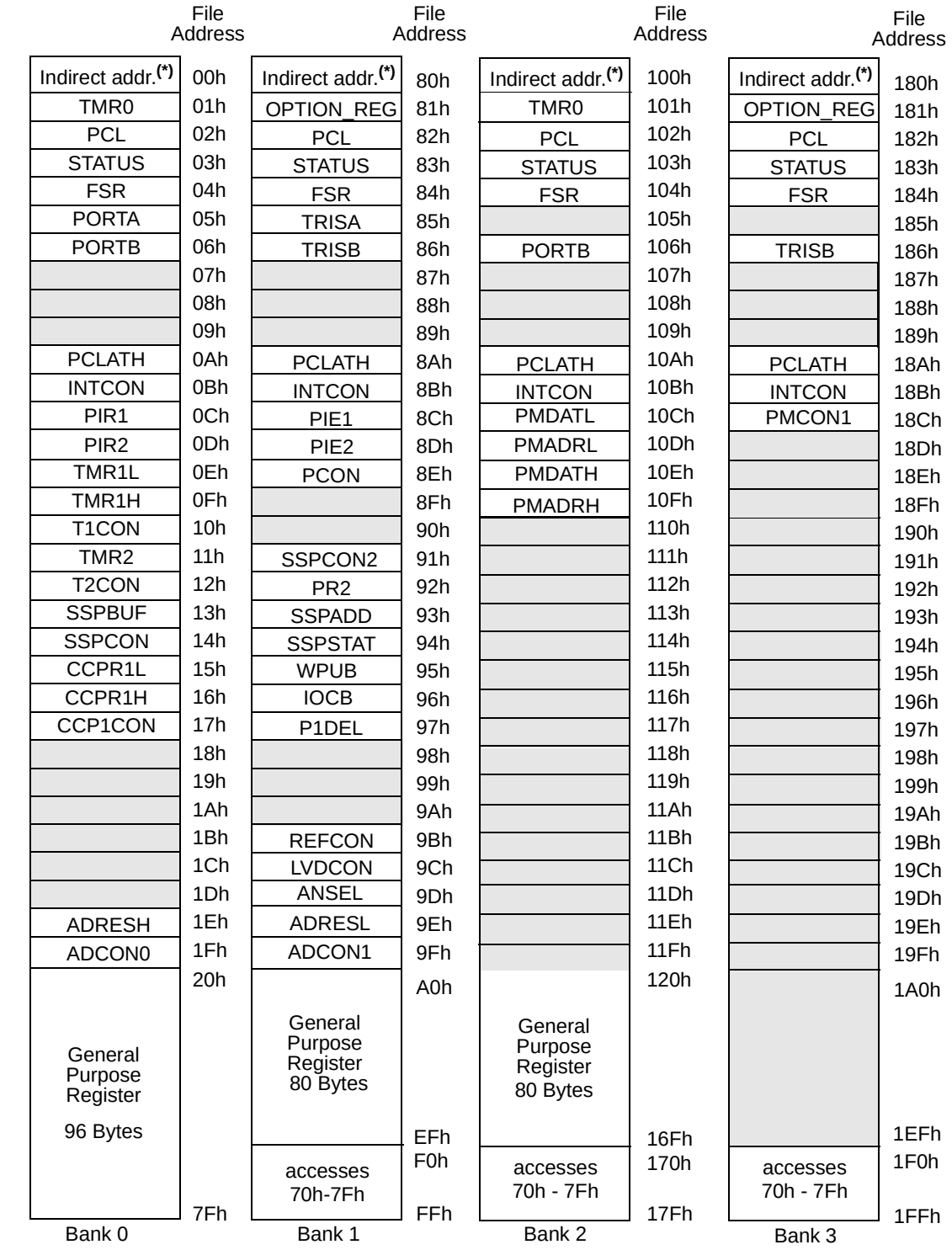
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc771t-i-ss

FIGURE 2-3: REGISTER FILE MAP



2.2.2.1 STATUS REGISTER

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions not affecting any status bits, see the "Instruction Set Summary."

Note:	The C and DC bits operate as a $\overline{\text{borrow}}$ and digit $\overline{\text{borrow}}$ bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 2-1: STATUS REGISTER (STATUS: 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h - 1FFh)
`0` = Bank 0, 1 (00h - FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h - 1FFh)
`10` = Bank 2 (100h - 17Fh)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{\text{borrow}}$ the polarity is reversed)
`1` = A carry-out from the 4th low order bit of the result occurred
`0` = No carry-out from the 4th low order bit of the result

bit 0 **C:** Carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note: For $\overline{\text{borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PIC Mid-Range MCU Family Reference Manual, (DS33023).

3.1 I/O Port Analog/Digital Mode

The PIC16C717/770/771 have two I/O ports: PORTA and PORTB. Some of these port pins are mixed-signal (can be digital or analog). When an analog signal is present on a pin, the pin must be configured as an analog input to prevent unnecessary current draw from the power supply. The Analog Select Register (ANSEL) allows the user to individually select the Digital/Analog mode on these pins. When the Analog mode is active, the port pin will always read 0.

Note 1:	On a Power-on Reset, the ANSEL register configures these mixed-signal pins as Analog mode.
2:	If a pin is configured as Analog mode, the RA pin will always read '0' and RB pin will always read '1', even if the digital output is active.

REGISTER 3-1: ANALOG SELECT REGISTER (ANSEL: 9Dh)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

bit 7-6 **Reserved:** Do not use

bit 5-0 **ANS<5:0>:** Analog Select between analog or digital function on pins AN<5:0>, respectively.
0 = Digital I/O. Pin is assigned to port or special function.
1 = Analog Input. Pin is assigned as analog input.

Note: Setting a pin to an analog input disables the digital input buffer on the pin. The corresponding TRIS bit should be set to Input mode when using pins as analog inputs.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.2 PORTA and the TRISA Register

PORTA is a 8-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pins RA<3:0> are multiplexed with analog functions, such as analog inputs to the A/D converter, analog V_{REF} inputs, and the onboard bandgap reference outputs. When the analog peripherals are using any of these pins as analog input/output, the ANSEL register must have the proper value to individually select the Analog mode of the corresponding pins.

Note:	Upon RESET, the ANSEL register configures the RA<3:0> pins as analog inputs. All RA<3:0> pins will read as '0'.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output.

Pin RA5 is multiplexed with the device RESET ($\overline{MCLR}$) and programming input (V_{PP}) functions. The RA5/$\overline{MCLR}$/V_{PP} input only pin has a Schmitt Trigger input buffer. All other RA port pins have Schmitt Trigger input buffers and full CMOS output buffers.

Pins RA6 and RA7 are multiplexed with the oscillator input and output functions.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

9.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI™)
- Inter-Integrated Circuit (I^2C™)

9.1.5 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

9.1.6 SLAVE SELECT SYNCHRONIZATION

The $\overline{SS}$ pin allows a Synchronous Slave mode. The SPI must be in Slave mode with $\overline{SS}$ pin control enabled (SSPCON<3:0> = 0100). The pin must not be driven low for the $\overline{SS}$ pin to function as an input. TRISB<1> must be set. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/ pull-down resistors may be desirable, depending on the application.

Note 1:	When the SPI module is in Slave mode with $\overline{SS}$ pin control enabled, (SSPCON<3:0> = 0100) the SPI module will RESET if the $\overline{SS}$ pin is set to VDD.
2:	If the SPI is used in Slave Mode with CKE = '1', then $\overline{SS}$ pin control must be enabled.

When the SPI module RESETS, the bit counter is forced to 0. This can be done by either forcing the $\overline{SS}$ pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 9-4: SLAVE SYNCHRONIZATION WAVEFORM

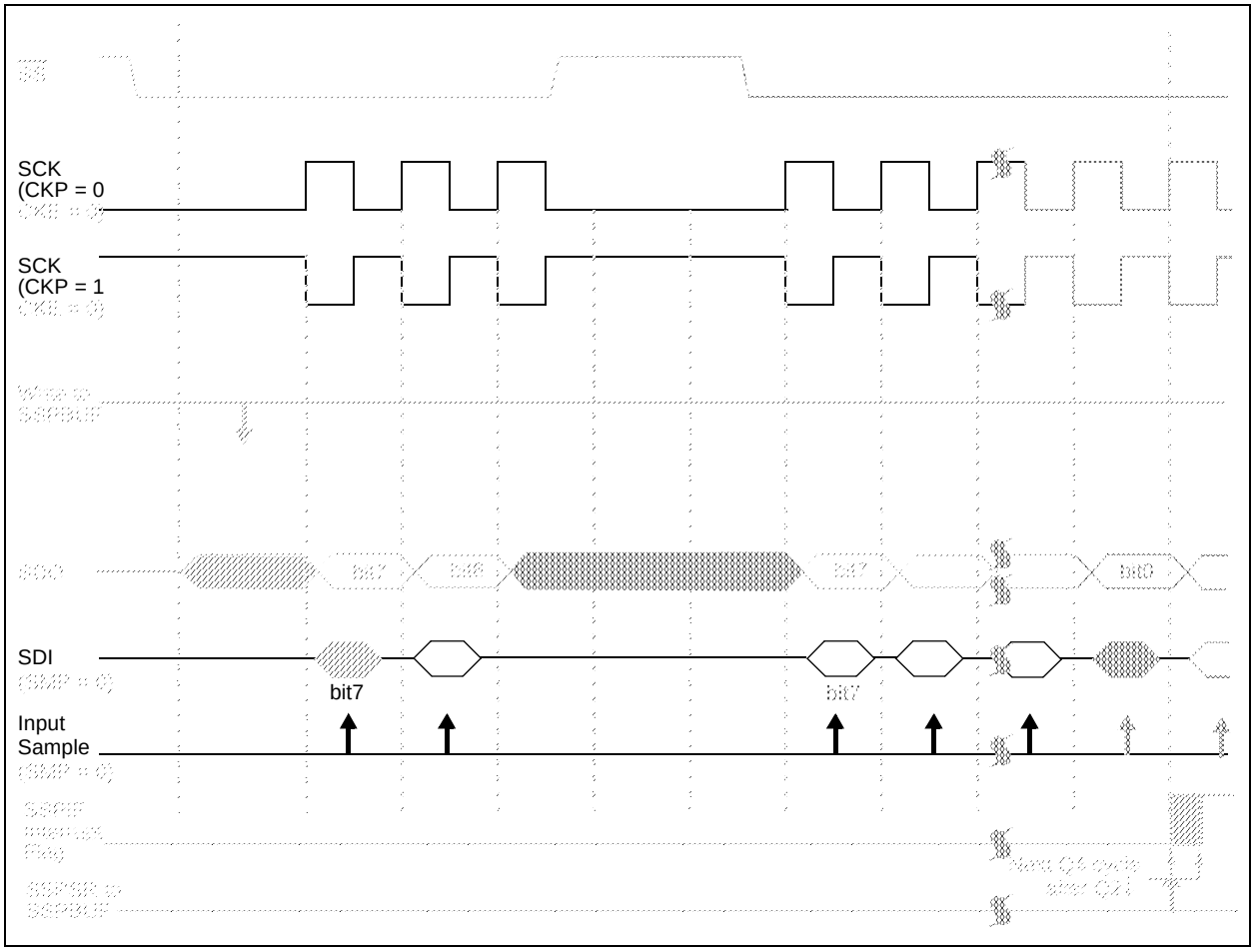


FIGURE 9-5: SPI SLAVE MODE WAVEFORM (CKE = 0)

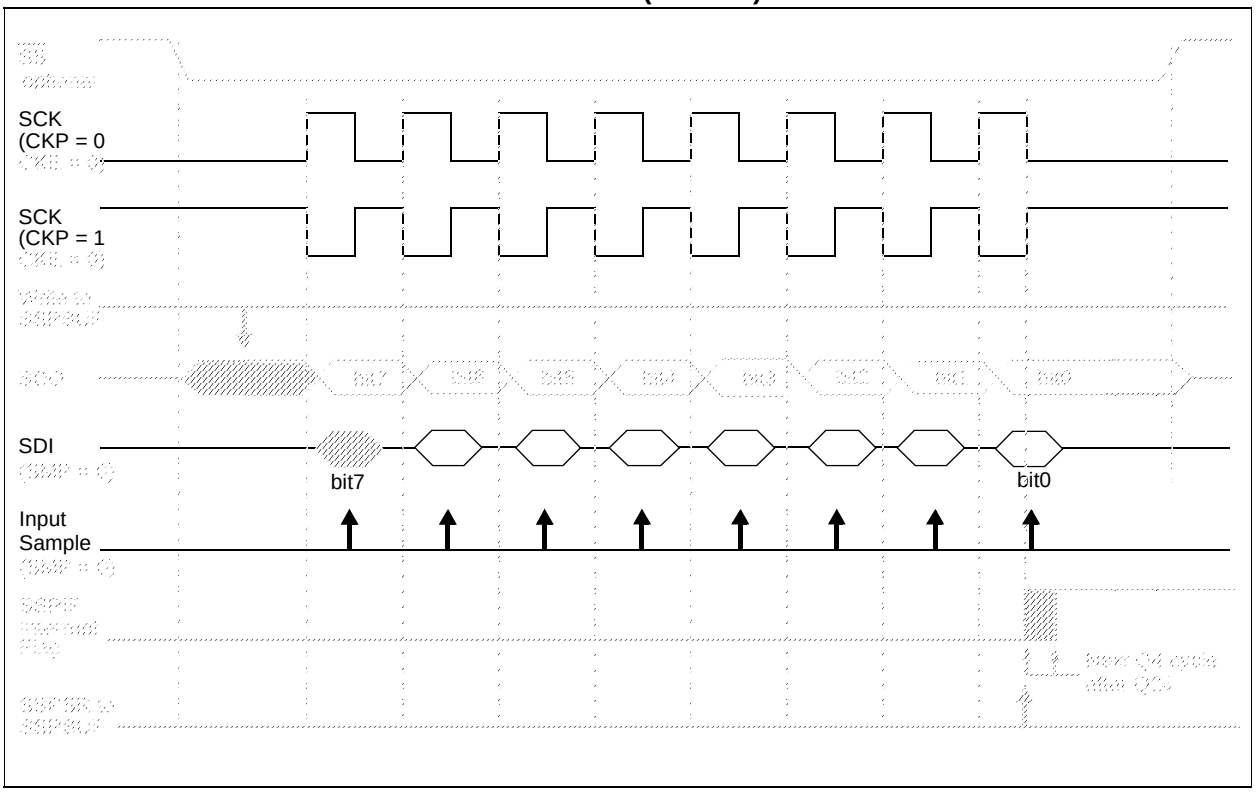
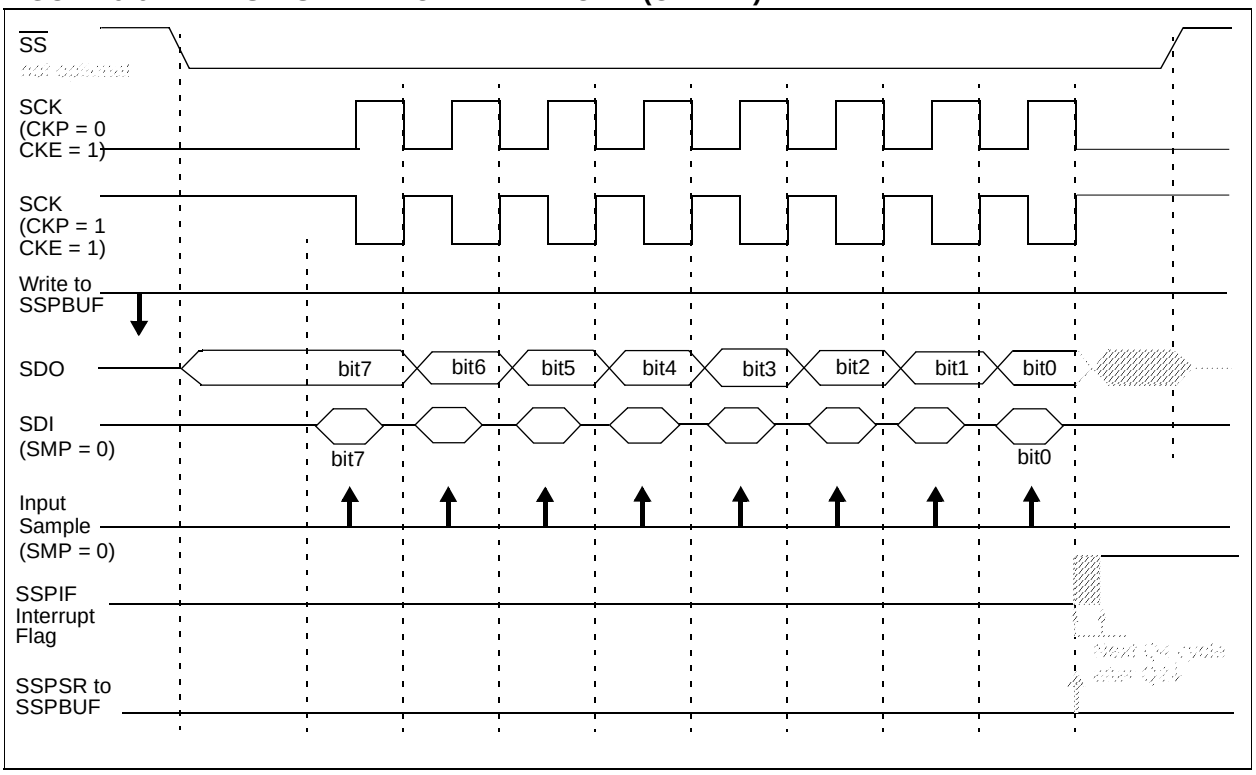


FIGURE 9-6: SPI SLAVE MODE WAVEFORM (CKE = 1)



9.2 MSSP I²C Operation

The MSSP module in I²C mode fully implements all master and slave functions (including general call support) and provides interrupts on START and STOP bits in hardware to determine when the bus is free (multimaster function). The MSSP module implements the Standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used to transfer data. They are the SCL pin (clock) and the SDA pin (data). The MSSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>). The SCL and SDA pins are "glitch" filtered when operating as inputs. This filter functions in both the 100 kHz and 400 kHz modes. When these pins operate as outputs in the 100 kHz mode, there is a slew rate control of the pin that is independent of device frequency.

Before selecting any I²C mode, the SCL and SDA pins must be programmed as inputs by setting the appropriate TRIS bits. This allows the MSSP module to configure and drive the I/O pins as required by the I²C protocol.

The MSSP module has six registers for I²C operation. They are listed below.

- SSP Control Register (SSPCON)
- SSP Control Register2 (SSPCON2)
- SSP STATUS Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

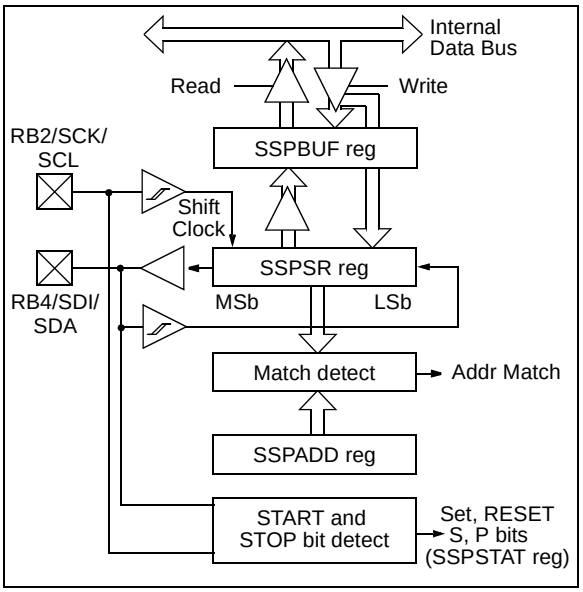
The SSPCON register allows for control of the I²C operation. Four mode selection bits (SSPCON<3:0>) configure the MSSP as any one of the following I²C modes:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Master mode
  SCL Freq = FOSC / [4 • (SSPADD + 1)]
- I²C Slave mode with START and STOP interrupts (7-bit address)
- I²C Slave mode with START and STOP interrupts (10-bit address)
- Firmware Controlled Master mode

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START (S) or STOP (P) bit. It specifies whether the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer.

SSPBUF is the register to which the transfer data is written, and from which the transfer data is read. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled, buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred from the SSPSR register to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read a receiver overflow occurs, in which case, the SSPOV bit (SSPCON<6>) is set and the byte in the SSPSR is lost.

FIGURE 9-7: I²C SLAVE MODE BLOCK DIAGRAM



9.2.1 UPWARD COMPATIBILITY WITH SSP MODULE

The MSSP module includes three SSP modes of operation to maintain upward compatibility with the SSP module. These modes are:

- Firmware controlled Master mode (slave idle)
- 7-bit Slave mode with START and STOP condition interrupts.
- 10-bit Slave mode with START and STOP condition interrupts.

The firmware controlled Master mode enables the START and STOP condition interrupts but all other I²C functions are generated through firmware including:

- Generating the START and STOP conditions
- Generating the SCL clock
- Supplying the SDA bits in the proper time and phase relationship to the SCL signal.

In firmware controlled Master mode, the SCL and SDA lines are manipulated by clearing and setting the corresponding TRIS bits. The output level is always low irrespective of the value(s) in the PORT register. A '1' is output by setting the TRIS bit and a '0' is output by clearing the TRIS bit

The 7-bit and 10-bit Slave modes with START and STOP condition interrupts operate identically to the MSSP Slave modes except that START and STOP conditions generate SSPIF interrupts.

9.2.2.3 SLAVE RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear (SSPSR<0> = 0) and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register on the falling edge of the eighth SCL pulse.

When the address byte overflow condition exists, then no Acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) or bit SSPOV (SSPCON<6>) is set.

An MSSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the received byte.

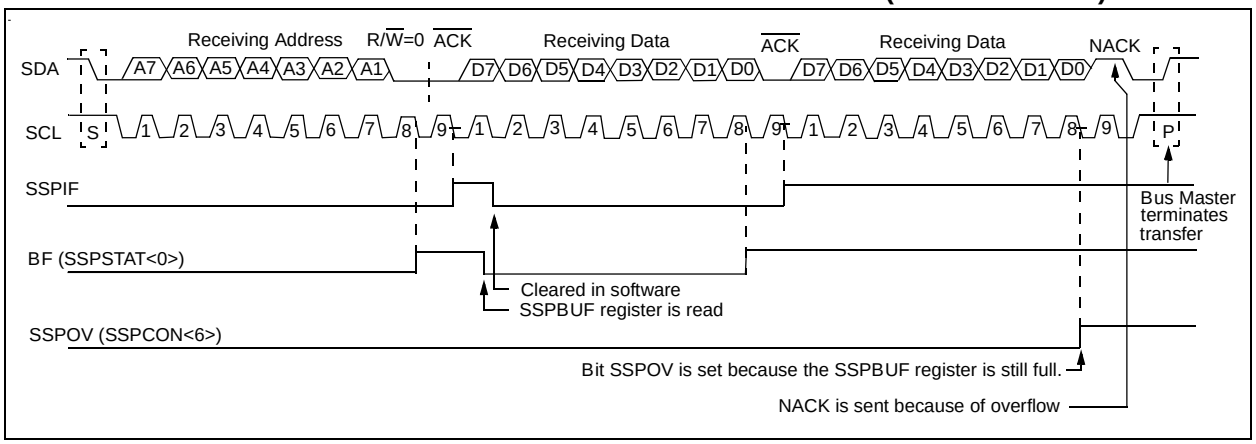
Note:	The SSPBUF will be loaded if the SSPOV bit is set and the BF flag is cleared. If a read of the SSPBUF was performed, but the user did not clear the state of the SSPOV bit before the next receive occurred, the $\overline{ACK}$ is not sent and the SSPBUF is updated.

TABLE 9-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received				
BF	**SSPOV**	**SSPSR → SSPBUF**	**Generate $\overline{ACK}$ Pulse**	**Set bit SSPIF (SSP Interrupt occurs if enabled)**
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	Yes	No	Yes

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

FIGURE 9-8: I^2C SLAVE MODE WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



9.2.7 MULTI-MASTER OPERATION

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET or when the MSSP module is disabled. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware, with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A START Condition
- A Repeated START Condition
- An Acknowledge Condition

Refer to Application Note AN578, *"Use of the SSP Module in the I^2C™ Multi-Master Environment."*

9.2.8 I^2C MASTER OPERATION

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON and by setting the SSPEN bit. Once Master mode is enabled, the user has six options.

1. Assert a START condition on SDA and SCL.
2. Assert a Repeated START condition on SDA and SCL.
3. Write to the SSPBUF register initiating transmission of data/address.
4. Generate a STOP condition on SDA and SCL.
5. Configure the I^2C port to receive data.
6. Generate an Acknowledge condition at the end of a received byte of data.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the I^2C bus will not be released.

Note:	The MSSP Module, when configured in I^2C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a START condition and immediately write the SSPBUF register to initiate transmission before the START condition is complete. In this case, the SSPBUF will not be written to, and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

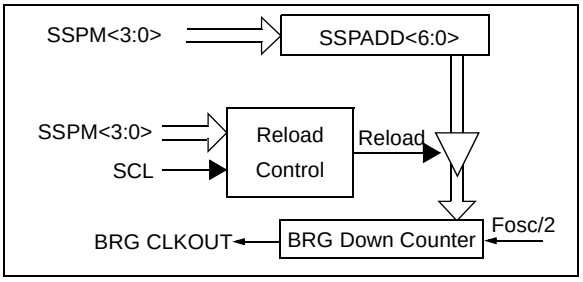
9.2.9 BAUD RATE GENERATOR

The baud rate generator used for SPI mode operation is used in the I^2C Master mode to set the SCL clock frequency. Standard SCL clock frequencies are 100 kHz, 400 kHz, and 1 MHz. One of these frequencies can be achieved by setting the SSPADD register to the appropriate number for the selected Fosc frequency. One half of the SCL period is equal to [(SSPADD+1) •2]/Fosc.

The baud rate generator reload value is contained in the lower seven bits of the SSPADD register (Figure 9-14). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload occurs. The BRG count is decremented twice per instruction cycle (TCY) on the Q2 and Q4 clock.

In I^2C Master mode, the BRG is reloaded automatically provided that the SCL line is sampled high. For example, if Clock Arbitration is taking place, the BRG reload will be suppressed until the SCL line is released by the slave allowing the pin to float high (Figure 9-15).

FIGURE 9-14: BAUD RATE GENERATOR BLOCK DIAGRAM



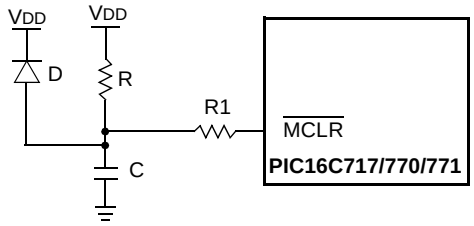
12.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when a VDD rise is detected (in the range of 1.5V - 2.1V). Enable the internal MCLR feature to eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details. For a long rise time, enable external MCLR function and use circuit as shown in Figure 12-5.

Two delay timers, (PWRT on OST), have been provided which hold the device in RESET after a POR (dependent upon device configuration) so that all operational parameters have been met prior to releasing the device to resume/begin normal operation.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions, or if necessary an external POR circuit may be implemented to delay end of RESET for as long as needed.

FIGURE 12-5: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD RAMP)



Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

4: External MCLR must be enabled (MCLRE = 1).

12.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed TPWRT time-out on power-up type RESETS only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the RESET condition (VDD rises above BOR trip point). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

12.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

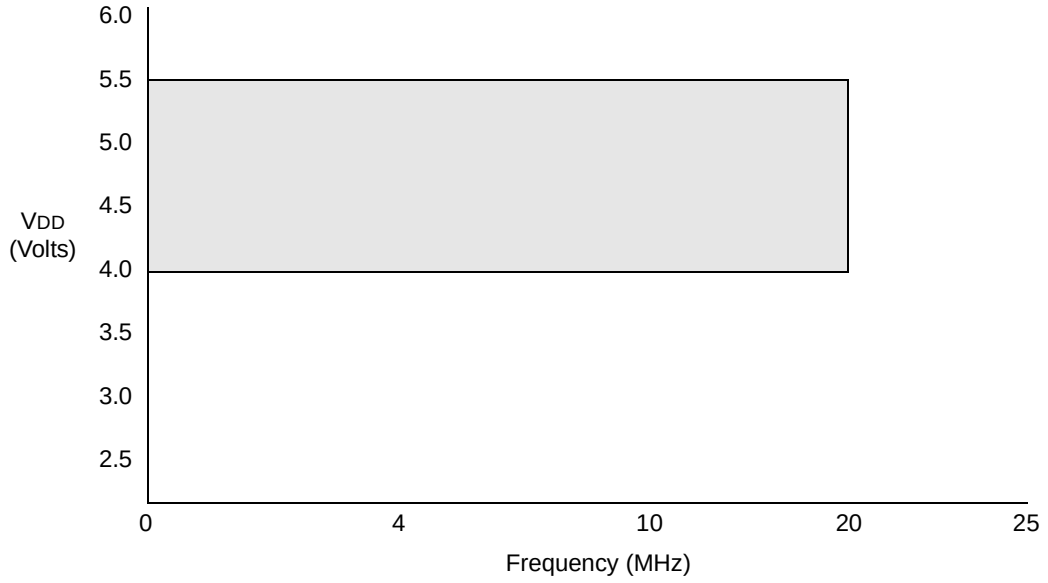
The OST time-out is invoked only for XT, LP and HS modes and only on a power-up type RESET or a wake-up from SLEEP.

12.7 Programmable Brown-Out Reset (PBOR)

The Programmable Brown-out Reset module is used to generate a RESET when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV<1:0> configuration word bits.

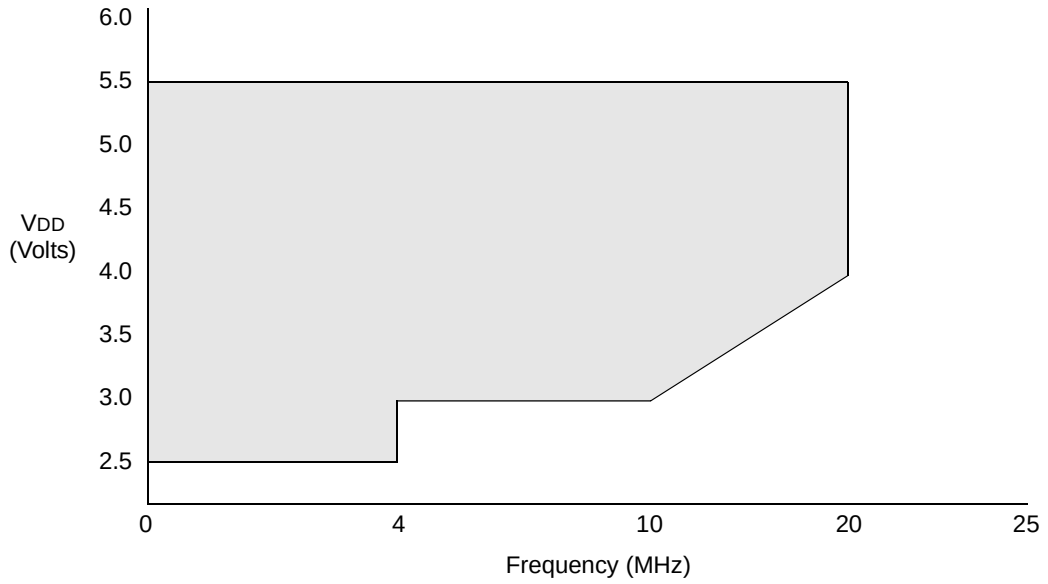
Configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below the specified trip point for longer than TBOR, (parameter #35), the brown-out situation will RESET the chip. A RESET may not occur if VDD falls below the trip point for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer will be invoked at that point and will keep the chip in RESET an additional TPWRT. If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will again begin a TPWRT time delay. Even though the PWRT is always enabled when brown-out is enabled, the PWRT configuration word bit should be cleared (enabled) when brown-out is enabled.

FIGURE 15-1: PIC16C717/770/771 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-2: PIC16LC717/770/771 VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16C717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IDD	**Supply Current(2)**					
D010D		**PIC16LC7XX**		1.0	2.0	mA	FOSC = 10 MHz, VDD = 3V, -40°C to 85°C
D010E					3.0		FOSC = 10 MHz, VDD = 3V, -40°C to 125°C
D010G				0.36	1.0	mA	FOSC = 4 MHz, VDD = 2.5V, -40°C to 125°C
D010K				11	45	µA	FOSC = 32 kHz, VDD = 2.5V, -40°C to 125°C
	IDD	**Supply Current(2)**					
D010		**PIC16C7XX**		4.0	7.5	mA	FOSC = 20 MHz, VDD = 5.5V, -40°C to 85°C
D010A					12.0		FOSC = 20 MHz, VDD = 5.5V, -40°C to 125°C
D010B				2.5	5.0	mA	FOSC = 20 MHz, VDD = 4V, -40°C to 85°C
D010C					6.0		FOSC = 20 MHz, VDD = 4V, -40°C to 125°C
D010F				0.55	1.5	mA	FOSC = 4 MHz, VDD = 4V, -40°C to 125°C
D010H				30	80	µA	FOSC = 32 kHz, VDD = 4V, -40°C to 85°C
D010J					95		FOSC = 32 kHz, VDD = 4V, -40°C to 125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active Operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

15.1 DC Characteristics: PIC16C717/770/771 (Commercial, Industrial, Extended) PIC16LC717/770/771 (Commercial, Industrial, Extended) (Continued)

PIC16LC717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16C717/770/771			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Base plus Module current					
D021A	IWDT	Watchdog Timer		2	10	µA	VDD = 3V, -40°C to 125°C
D021	IWDT	Watchdog Timer		5	20	µA	VDD = 4V, -40°C to 125°C
D021	IWDT	Watchdog Timer		5	20	µA	VDD = 4V, -40°C to 125°C
D025	IT1OSC	Timer1 Oscillator		3	9	µA	VDD = 3V, -40°C to 125°C
D025	IT1OSC	Timer1 Oscillator		4	12	µA	VDD = 4V, -40°C to 125°C
D025	IT1OSC	Timer1 Oscillator		4	12	µA	VDD = 4V, -40°C to 125°C
D026*	IAD	ADC Converter		300		µA	VDD = 5.5V, A/D on, not converting
D026*	IAD	ADC Converter		300		µA	VDD = 5.5V, A/D on, not converting
D027	IPLVD	Programmable Low Voltage Detect		55	125	µA	VDD = 4V, -40°C to 85°C
D027A					150		VDD = 4V, -40°C to 125°C
D027	IPLVD	Programmable Low Voltage Detect		55	125	µA	VDD = 4V, -40°C to 85°C
D027A					150		VDD = 4V, -40°C to 125°C
D028	IPBOR	Programmable Brown-out Reset		55	125	µA	VDD = 5V, -40°C to 85°C
D028A					150		VDD = 5V, -40°C to 125°C
D028	IPBOR	Programmable Brown-out Reset		55	125	µA	VDD = 5V, -40°C to 85°C
D028A					150		VDD = 5V, -40°C to 125°C
D029	IVRH	Voltage reference High		200	750	µA	VDD = 5V, -40°C to 85°C
D029A					1.0	mA	VDD = 5V, -40°C to 125°C
D029	IVRH	Voltage reference High		200	750	µA	VDD = 5V, -40°C to 85°C
D029A					1.0	mA	VDD = 5V, -40°C to 125°C
D030	IVRL	Voltage reference Low		200	750	µA	VDD = 4V, -40°C to 85°C
D030A					1.0	mA	VDD = 4V, -40°C to 125°C
D030	IVRL	Voltage reference Low		200	750	µA	VDD = 4V, -40°C to 85°C
D030A					1.0	mA	VDD = 4V, -40°C to 125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.2 DC Characteristics: PIC16C717/770/771 & PIC16LC717/770/771 (Commercial, Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in Section 15.1 and Section 15.2.				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range
D030A			VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	For entire VDD range
D032		$\overline{MCLR}$	VSS	—	0.2VDD	V	
D033		OSC1 (in XT, HS, LP and EC)	VSS	—	0.3VDD	V	
		Input High Voltage					
	VIH	I/O ports		—			
		with TTL buffer					
D040			2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25VDD + 0.8V)	—	VDD	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS, LP and EC)	0.7VDD	—	VDD	V	
D070	IPURB	PORTB weak pull-up current per pin	50	250	400	µA	VDD = 5V, VPIN = VSS
		Input Leakage Current (1,2)					
D060	IIL	I/O ports (with digital functions)	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A	IIL	I/O ports (with analog functions)	—	—	±100	nA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		RA5/$\overline{MCLR}$/VPP	—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS, LP and EC osc configuration
		Output Low Voltage					
D080	VOL	I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(2)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D150*	VOD	**Open Drain High Voltage**	—	—	10.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins*					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC	—	—	50	pF	
D102	CB	mode) SCL, SDA in I2C mode	—	—	400	pF	
	CVRH	VRH pin	—	—	200	pF	VRH output enabled
	CVRL	VRL pin	—	—	200	pF	VRL output enabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

FIGURE 15-20: SPI SLAVE MODE TIMING (CKE = 0)

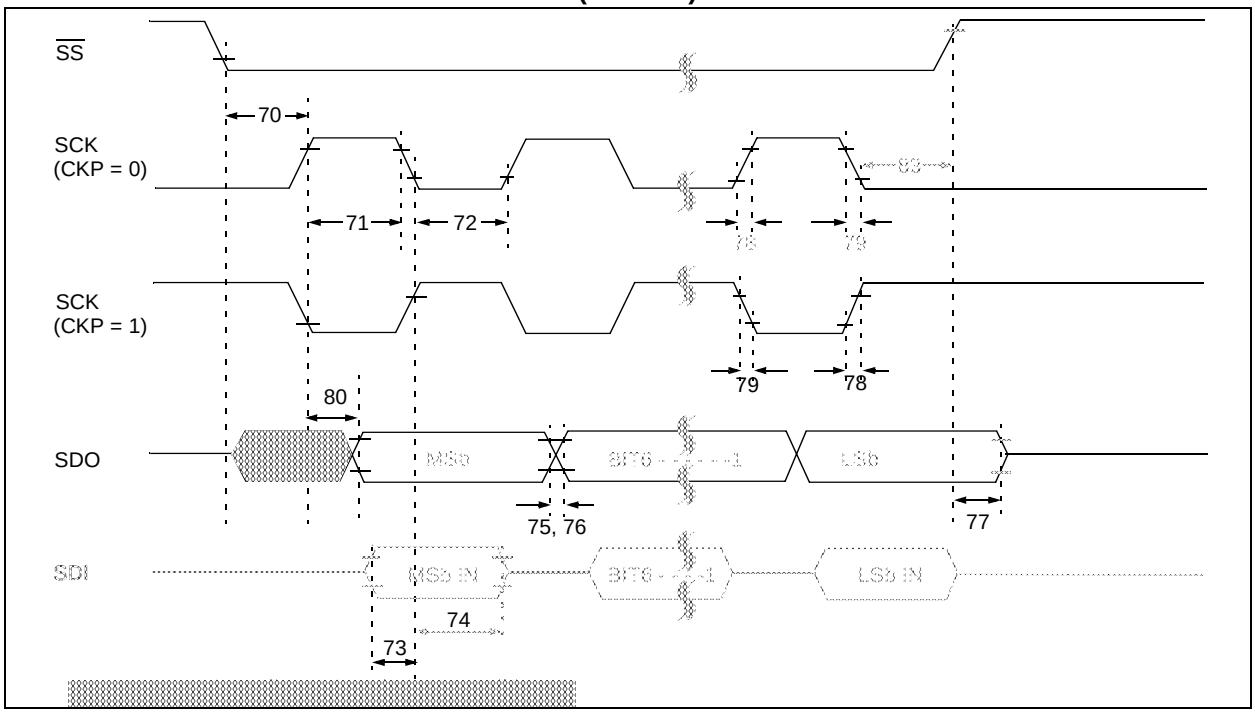


TABLE 15-19: SPI MODE REQUIREMENTS (SLAVE MODE TIMING (CKE = 0)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input		TCY	—	—	ns	
71*	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A*			Single Byte	40	—	—	ns	**Note 1**
72*	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A*			Single Byte	40	—	—	ns	**Note 1**
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A*	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	**Note 1**
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75*	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
76*	TdoF	SDO data output fall time		—	10	25	ns	
77*	TssH2doZ	$\overline{SS}$↑ to SDO output hi-impedance		10	—	50	ns	
78*	TscR	SCK output rise time (Master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX		—	100	ns	
83*	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK edge		1.5TCY + 40	—	—	ns	

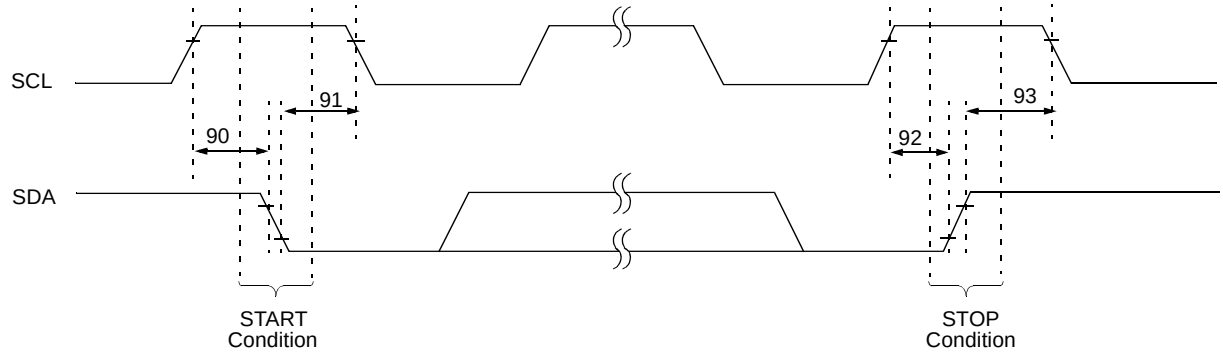
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

15.6 Master SSP I²C Mode Timing Waveforms and Requirements

FIGURE 15-22: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS



Note: Refer to Figure 15-4 for load conditions.

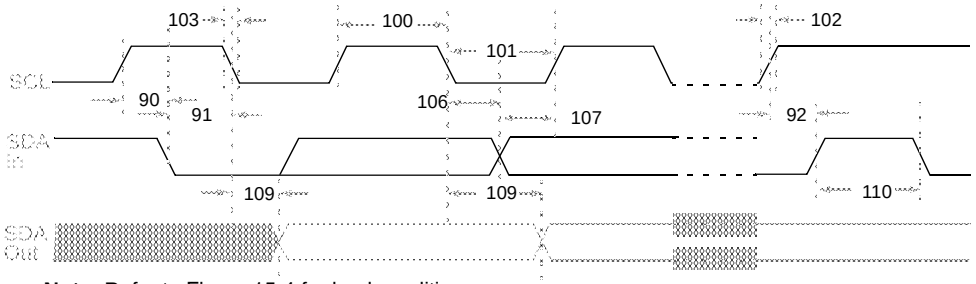
TABLE 15-21: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	Only relevant for a Repeated START condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		
93*	THD:STO	STOP condition Hold time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	—		

* These parameters are characterized but not tested. For the value required by the I²C specification, please refer to the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

Maximum pin capacitance = 10 pF for all I²C pins.

FIGURE 15-23: MASTER SSP I²C BUS DATA TIMING



Note: Refer to Figure 15-4 for load conditions.

FIGURE 16-12: MAXIMUM IDD VS. VDD (INTRC 37 kHZ MODE)

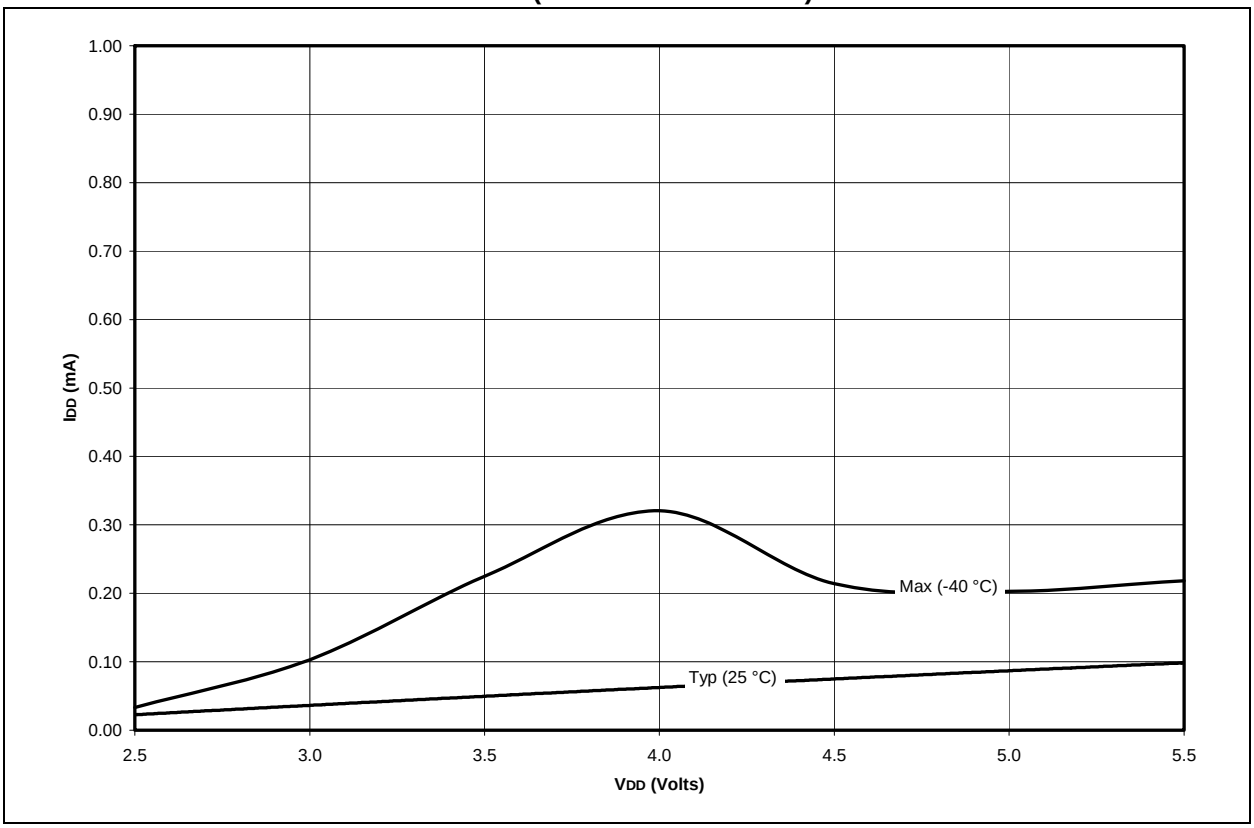
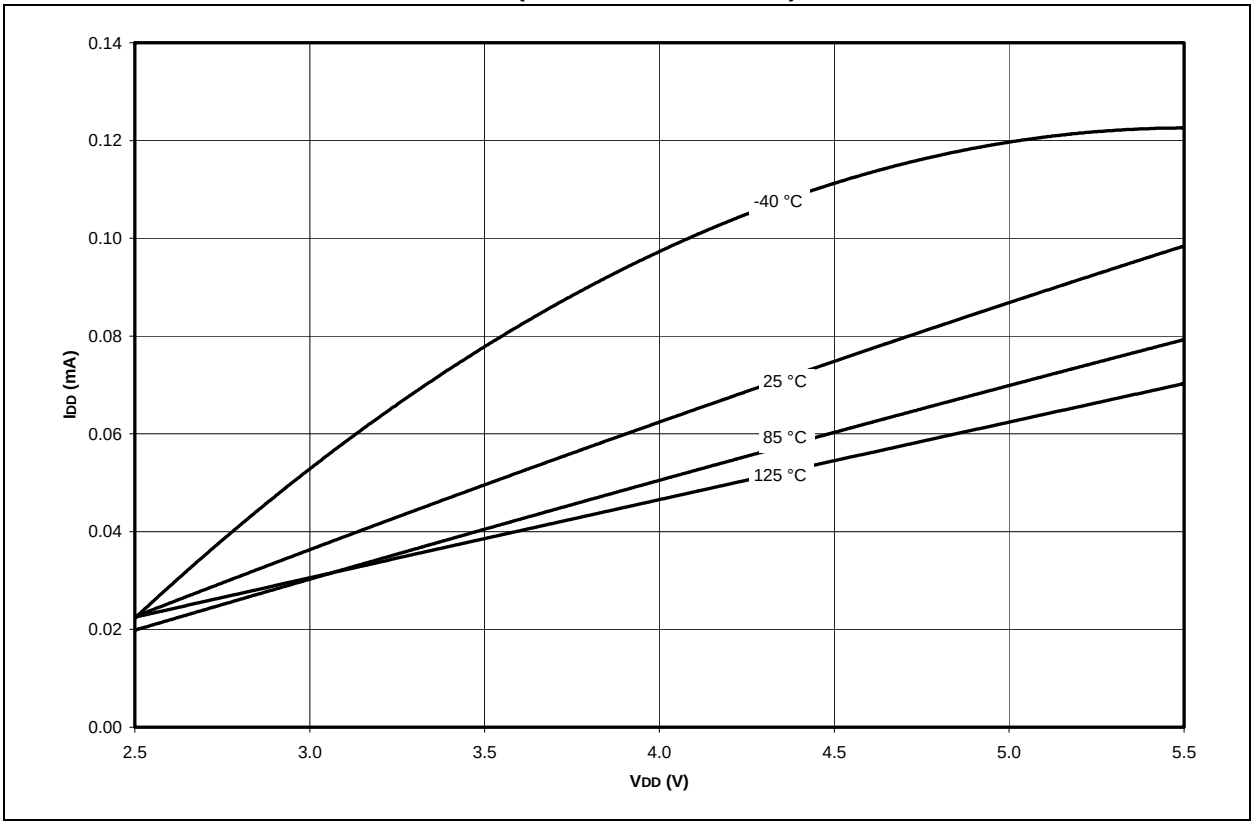


FIGURE 16-13: TYPICAL IDD VS. VDD (INTRC 37 kHZ MODE)



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