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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

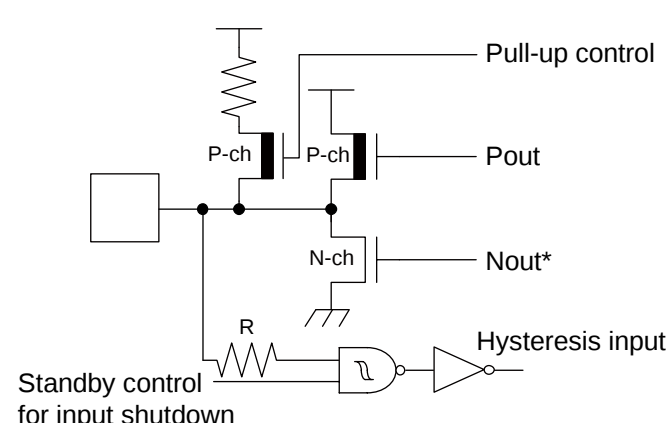
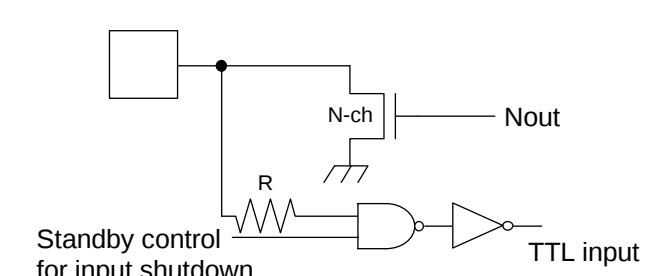
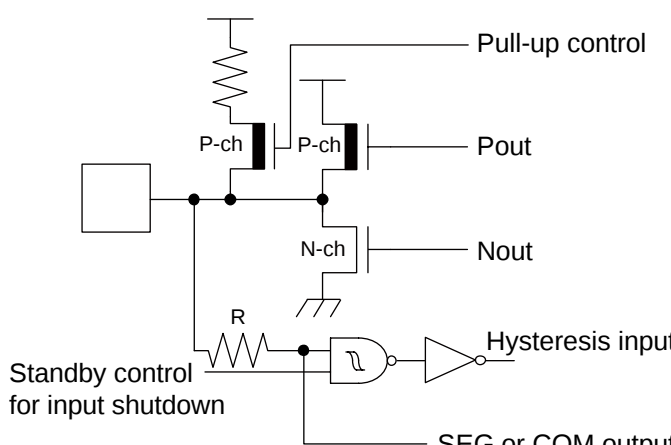
Details

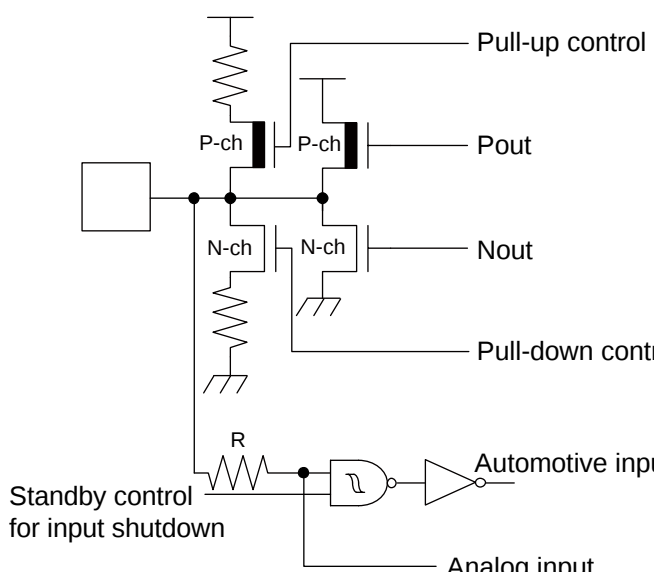
Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f685abpmc-gse1



4. Pin Description

Pin Name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
COMn	LCD	LCD Common driver pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
DVcc	Supply	SMC pins power supply
DVss	Supply	SMC pins power supply
FRCKn	Free-Running Timer	Free-Running Timer n input pin
FRCKn_R	Free-Running Timer	Relocated Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PWMn	SMC	SMC PWM high current output pin
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCLn	I ² C	I ² C interface n clock I/O input/output pin
SDAn	I ² C	I ² C interface n serial data I/O input/output pin
SEGn	LCD	LCD Segment driver pin
SGAn	Sound Generator	Sound Generator amplitude output pin
SGOn	Sound Generator	Sound Generator sound/tone output pin
SINn	USART	USART n serial data input pin
SOTn	USART	USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TINn_R	Reload Timer	Relocated Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TOTn_R	Reload Timer	Relocated Reload Timer n output pin

Type	Circuit	Remarks
N	 The diagram shows a CMOS output stage. A pull-up resistor is connected to the output node. A P-channel MOSFET (P-ch) is connected to the output node and its gate is controlled by a 'Pull-up control' signal. An N-channel MOSFET (N-ch) is connected to the output node and its gate is controlled by a 'Standby control for input shutdown' signal. The output node is also connected to a resistor 'R' which is connected to a 'Hysteresis input' signal. The output node is labeled 'Pout' and the N-channel MOSFET is labeled 'Nout*'. The output node is also connected to a 'Hysteresis input' signal.	• CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I²C spec, irrespective of usage.
O	 The diagram shows an open-drain output stage. An N-channel MOSFET (N-ch) is connected to the output node and its gate is controlled by a 'Standby control for input shutdown' signal. The output node is also connected to a resistor 'R' which is connected to a 'TTL input' signal. The output node is labeled 'Nout'.	• Open-drain I/O • Output 25mA, $V_{CC} = 2.7\text{V}$ • TTL input
P	 The diagram shows a CMOS output stage. A pull-up resistor is connected to the output node. A P-channel MOSFET (P-ch) is connected to the output node and its gate is controlled by a 'Pull-up control' signal. An N-channel MOSFET (N-ch) is connected to the output node and its gate is controlled by a 'Standby control for input shutdown' signal. The output node is also connected to a resistor 'R' which is connected to a 'Hysteresis input' signal. The output node is labeled 'Pout' and the N-channel MOSFET is labeled 'Nout'. The output node is also connected to a 'Hysteresis input' signal. The output node is also connected to a 'SEG or COM output' signal.	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis inputs with input shutdown function • Programmable pull-up resistor • SEG or COM output

Type	Circuit	Remarks
R	 Standby control for input shutdown Pull-up control P-ch Pout N-ch Nout Pull-down control R Automotive input Analog input	• CMOS level output (programmable $I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$ and $I_{OL} = 30\text{mA}$, $I_{OH} = -30\text{mA}$) • Automotive input with input shutdown function • Programmable pull-up / pull-down resistor • Analog input

11. Interrupt Vector Table

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
0	3FC _H	CALLV0	No	-	CALLV instruction
1	3F8 _H	CALLV1	No	-	CALLV instruction
2	3F4 _H	CALLV2	No	-	CALLV instruction
3	3F0 _H	CALLV3	No	-	CALLV instruction
4	3EC _H	CALLV4	No	-	CALLV instruction
5	3E8 _H	CALLV5	No	-	CALLV instruction
6	3E4 _H	CALLV6	No	-	CALLV instruction
7	3E0 _H	CALLV7	No	-	CALLV instruction
8	3DC _H	RESET	No	-	Reset vector
9	3D8 _H	INT9	No	-	INT9 instruction
10	3D4 _H	EXCEPTION	No	-	Undefined instruction execution
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Clock Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	LVDI	No	16	Low Voltage Detector
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	EXTINT1	Yes	18	External Interrupt 1
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	-	-	22	Reserved
23	3A0 _H	EXTINT6	Yes	23	External Interrupt 6
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	-	-	25	Reserved
26	394 _H	-	-	26	Reserved
27	390 _H	-	-	27	Reserved
28	38C _H	-	-	28	Reserved
29	388 _H	-	-	29	Reserved
30	384 _H	-	-	30	Reserved
31	380 _H	-	-	31	Reserved
32	37C _H	-	-	32	Reserved
33	378 _H	CAN0	No	33	CAN Controller 0
34	374 _H	-	-	34	Reserved
35	370 _H	-	-	35	Reserved
36	36C _H	-	-	36	Reserved
37	368 _H	-	-	37	Reserved
38	364 _H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360 _H	PPG1	Yes	39	Programmable Pulse Generator 1

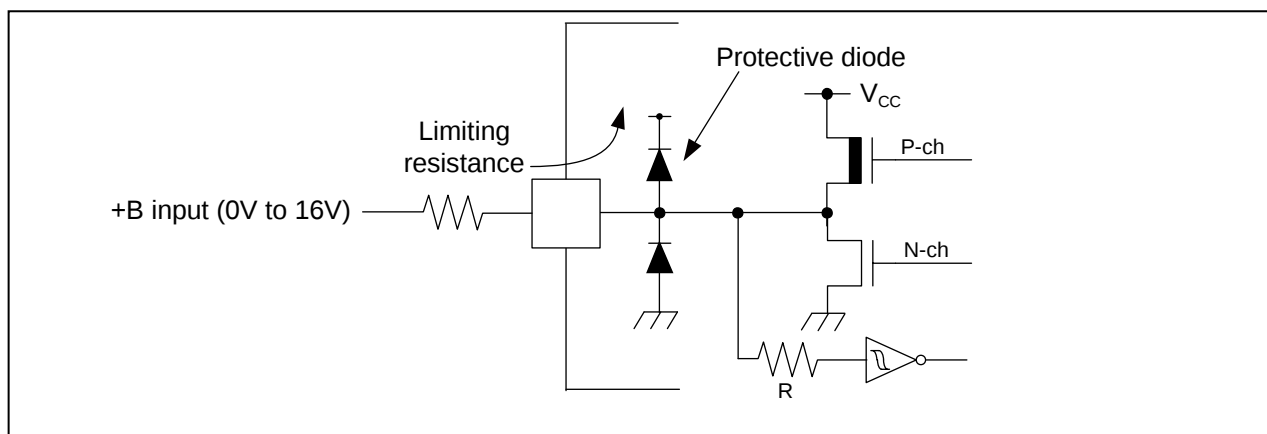
Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
40	35C _H	PPG2	Yes	40	Programmable Pulse Generator 2
41	358 _H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 _H	-	-	42	Reserved
43	350 _H	-	-	43	Reserved
44	34C _H	-	-	44	Reserved
45	348 _H	-	-	45	Reserved
46	344 _H	-	-	46	Reserved
47	340 _H	-	-	47	Reserved
48	33C _H	-	-	48	Reserved
49	338 _H	-	-	49	Reserved
50	334 _H	-	-	50	Reserved
51	330 _H	-	-	51	Reserved
52	32C _H	-	-	52	Reserved
53	328 _H	-	-	53	Reserved
54	324 _H	-	-	54	Reserved
55	320 _H	-	-	55	Reserved
56	31C _H	-	-	56	Reserved
57	318 _H	-	-	57	Reserved
58	314 _H	-	-	58	Reserved
59	310 _H	RLT1	Yes	59	Reload Timer 1
60	30C _H	RLT2	Yes	60	Reload Timer 2
61	308 _H	-	-	61	Reserved
62	304 _H	-	-	62	Reserved
63	300 _H	-	-	63	Reserved
64	2FC _H	RLT6	Yes	64	Reload Timer 6
65	2F8 _H	ICU0	Yes	65	Input Capture Unit 0
66	2F4 _H	ICU1	Yes	66	Input Capture Unit 1
67	2F0 _H	-	-	67	Reserved
68	2EC _H	-	-	68	Reserved
69	2E8 _H	ICU4	Yes	69	Input Capture Unit 4
70	2E4 _H	ICU5	Yes	70	Input Capture Unit 5
71	2E0 _H	-	-	71	Reserved
72	2DC _H	-	-	72	Reserved
73	2D8 _H	-	-	73	Reserved
74	2D4 _H	-	-	74	Reserved
75	2D0 _H	-	-	75	Reserved
76	2CC _H	-	-	76	Reserved
77	2C8 _H	-	-	77	Reserved
78	2C4 _H	-	-	78	Reserved
79	2C0 _H	-	-	79	Reserved
80	2BC _H	-	-	80	Reserved

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	V _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	
Analog power supply voltage*1	AV _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _{CC} = AV _{CC} *2
Analog reference voltage*1	AVRH	-	V _{SS} - 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVRH, AVRH ≥ AV _{SS}
SMC Power supply*1	DV _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _{CC} = AV _{CC} = DV _{CC} *2
LCD power supply voltage*1	V0 to V3	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V0 to V3 must not exceed V _{CC}
Input voltage*1	V _I	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _I ≤ (D)V _{CC} + 0.3V*3
Output voltage*1	V _O	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _O ≤ (D)V _{CC} + 0.3V*3
Maximum Clamp Current	I _{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins *4
Total Maximum Clamp Current	Σ I _{CLAMP}	-	-	21	mA	Applicable to general purpose I/O pins *4
"L" level maximum output current	I _{OL}	-	-	15	mA	Normal port
	I _{OLSMC}	T _A = -40°C	-	52	mA	High current port
		T _A = +25°C	-	39	mA	
		T _A = +85°C	-	32	mA	
		T _A = +105°C	-	30	mA	
"L" level average output current	I _{OLAV}	-	-	4	mA	Normal port
	I _{OLAVSMC}	T _A = -40°C	-	40	mA	High current port
		T _A = +25°C	-	30	mA	
		T _A = +85°C	-	25	mA	
		T _A = +105°C	-	23	mA	
"L" level maximum overall output current	ΣI _{OL}	-	-	46	mA	Normal port
	ΣI _{OLSMC}	-	-	180	mA	High current port
"L" level average overall output current	ΣI _{OLAV}	-	-	23	mA	Normal port
	ΣI _{OLAVSMC}	-	-	90	mA	High current port
"H" level maximum output current	I _{OH}	-	-	-15	mA	Normal port
	I _{OHSMC}	T _A = -40°C	-	-52	mA	High current port
		T _A = +25°C	-	-39	mA	
		T _A = +85°C	-	-32	mA	
		T _A = +105°C	-	-30	mA	
"H" level average output current	I _{OHAV}	-	-	-4	mA	Normal port
	I _{OHAVSMC}	T _A = -40°C	-	-40	mA	High current port
		T _A = +25°C	-	-30	mA	
		T _A = +85°C	-	-25	mA	
		T _A = +105°C	-	-23	mA	
"H" level maximum overall output current	ΣI _{OH}	-	-	-46	mA	Normal port
	ΣI _{OHSMC}	-	-	-180	mA	High current port
"H" level average overall output current	ΣI _{OHAV}	-	-	-23	mA	Normal port
	ΣI _{OHAVSMC}	-	-	-90	mA	High current port
Power consumption*5	P _D	T _A = +105°C	-	317*6	mW	
Operating ambient temperature	T _A	-	-40	+105	°C	
Storage temperature	T _{STG}	-	-55	+150	°C	

- *1: This parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0V$.
- *2: AV_{CC} and V_{CC} and DV_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} , DV_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.
- *3: V_I and V_O should not exceed $V_{CC} + 0.3V$. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the ICLAMP rating supersedes the V_I rating. Input/Output voltages of high current ports depend on DV_{CC} . Input/Output voltages of standard ports depend on V_{CC} .
- *4:
- Applicable to all general purpose I/O pins (Pnn_m).
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
 - The DEBUG I/F pin has only a protective diode against V_{SS} . Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
 - Sample recommended circuits:



- *5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
 The actual power dissipation depends on the customer application and can be calculated as follows:
 $PD = P_{IO} + P_{INT}$
 $P_{IO} = \sum (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
 $P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
 I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
 I_A is the analog current consumption into AV_{CC} .
- *6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

WARNING

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V _{CC} , AV _{CC} , DV _{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C _S	0.5	1.0 to 3.9	4.7	μF	1.0μF (Allowance within ± 50%) 3.9μF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V _{CC} must use the one of a capacity value that is larger than C _S .

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes ^{*1}	I _{CCSPLL}	V _{CC}	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	6.5	-	mA	T _A = +25°C
				-	-	13	mA	T _A = +105°C
	I _{CCSMAIN}		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	0.9	-	mA	T _A = +25°C
				-	-	4	mA	T _A = +105°C
	I _{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.5	-	mA	T _A = +25°C
				-	-	3.5	mA	T _A = +105°C
	I _{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.06	-	mA	T _A = +25°C
				-	-	2.7	mA	T _A = +105°C
	I _{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T _A = +25°C
				-	-	2.5	mA	T _A = +105°C

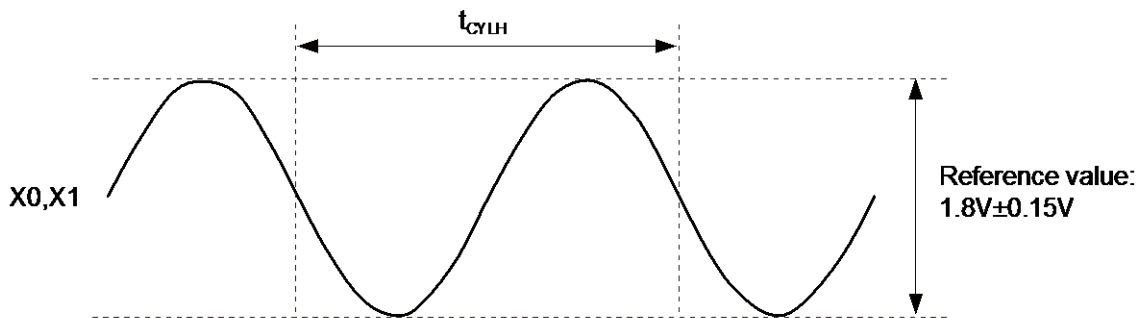
14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^\circ C$ to $+105^\circ C$)

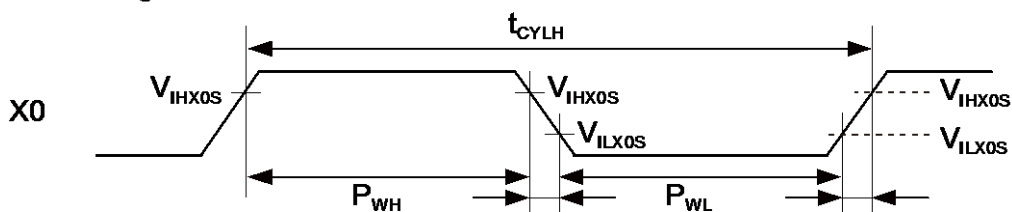
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_c	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	

When using the crystal oscillator



The amplitude changes by resistance, capacity which added outside or the difference of the device.

When using the external clock



14.4.3 Built-in RC Oscillation Characteristics

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	μs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	μs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 Internal Clock Timing

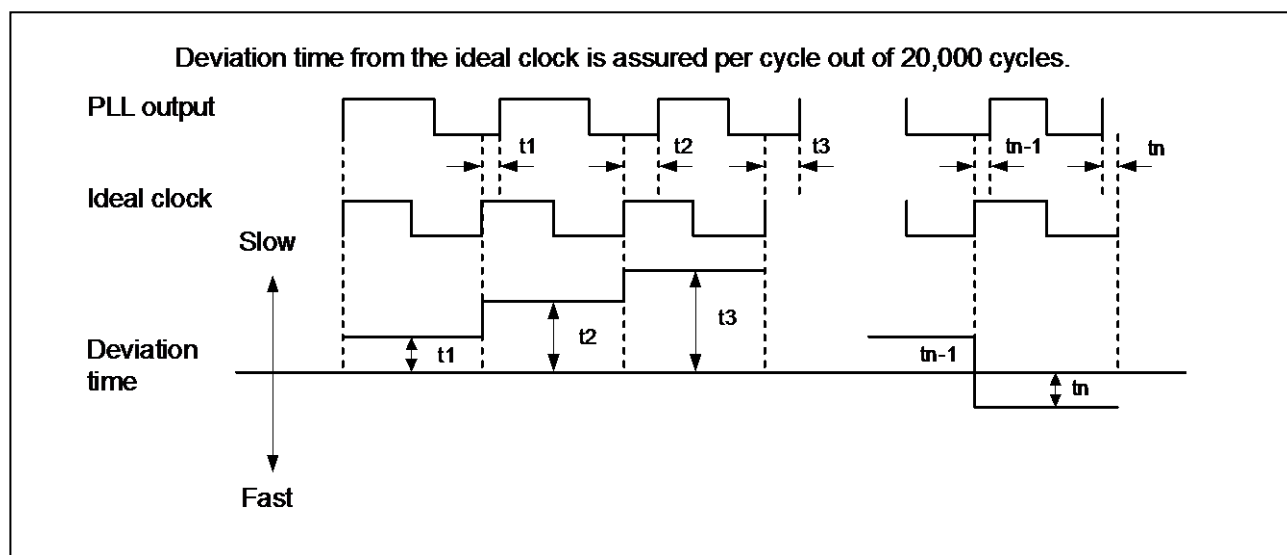
($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.5 Operating Conditions of PLL

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

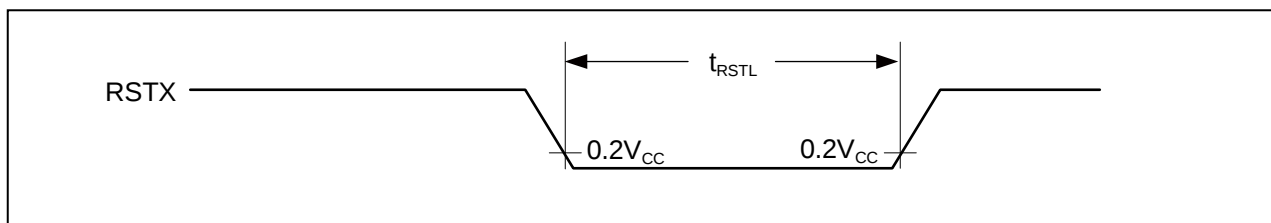
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) $\geq 4MHz$



14.4.6 Reset Input

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

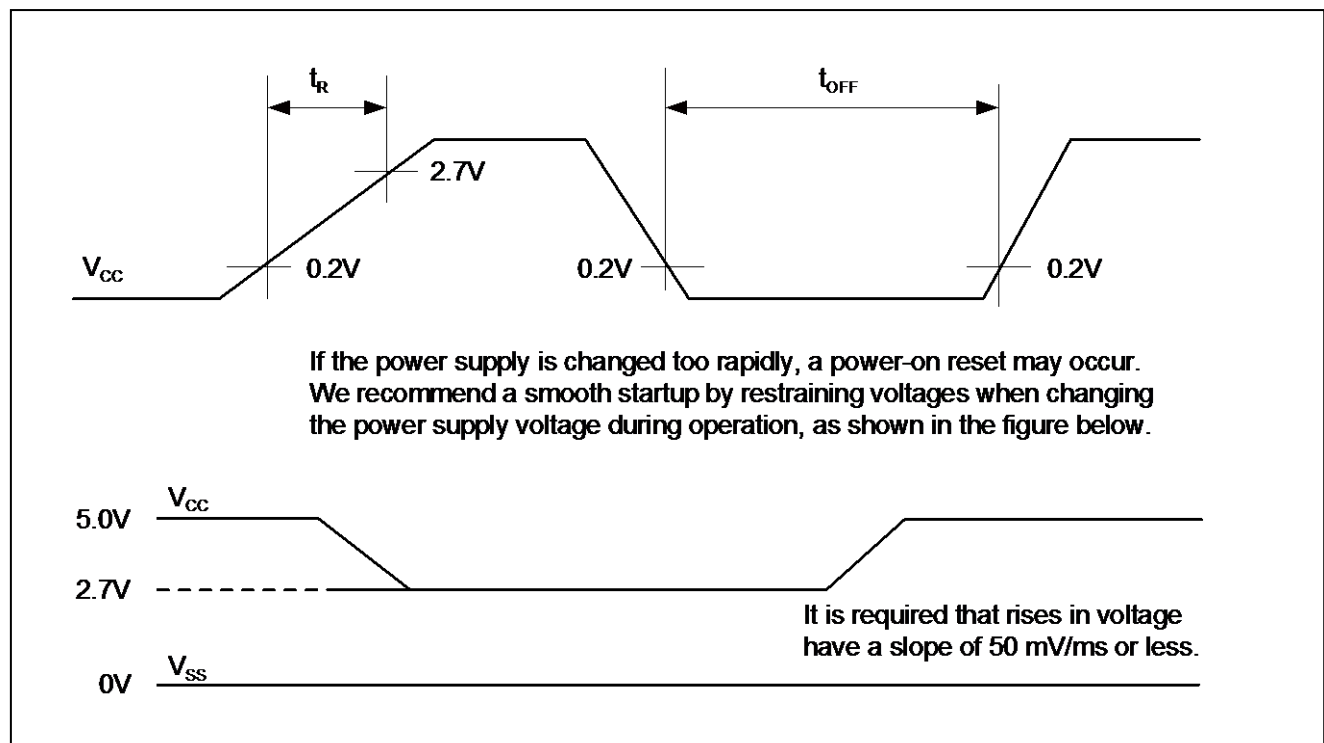
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	μS
Rejection of reset input time			1	-	μS



14.4.7 Power-on Reset Timing

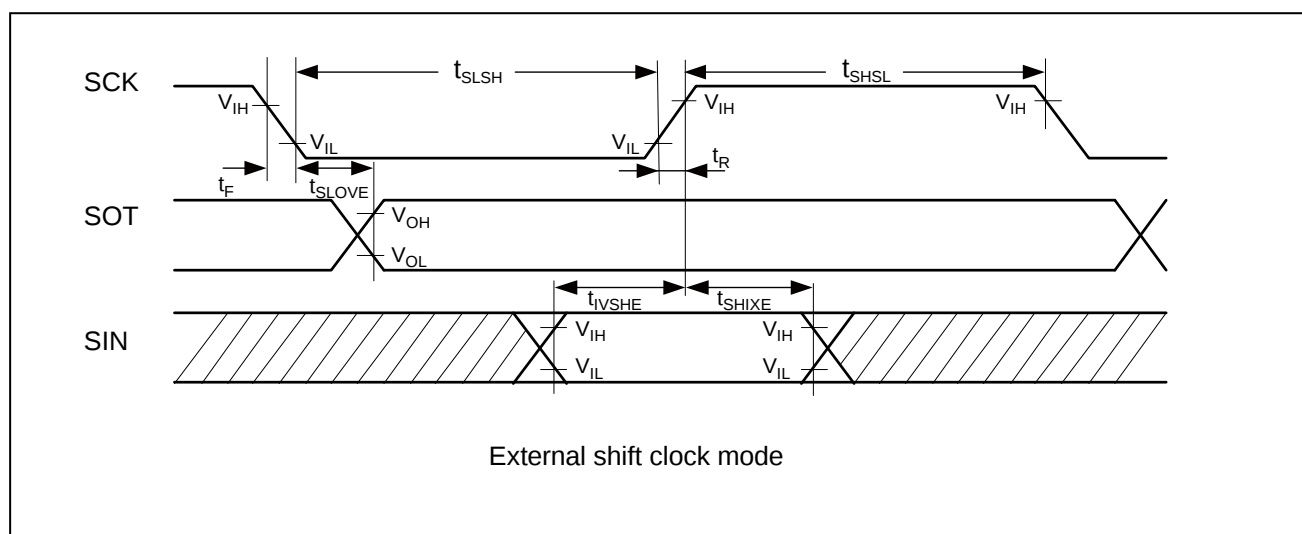
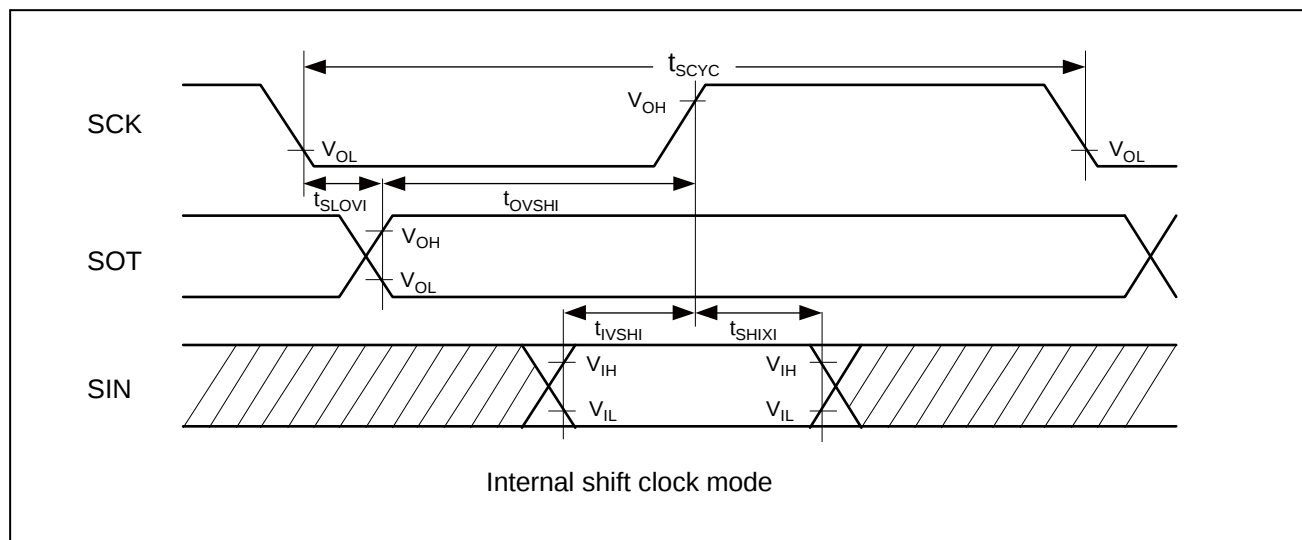
($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	V_{CC}	0.05	-	30	ms
Power off time	t_{OFF}	V_{CC}	1	-	-	ms



Examples:

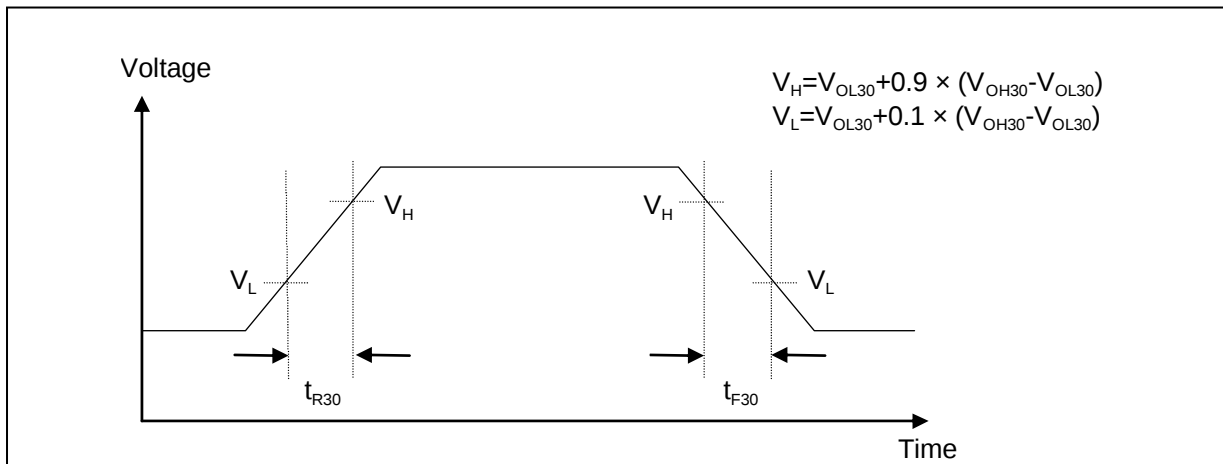
t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}, 6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}, 8 \times t_{CLKP1}$	4
...	...

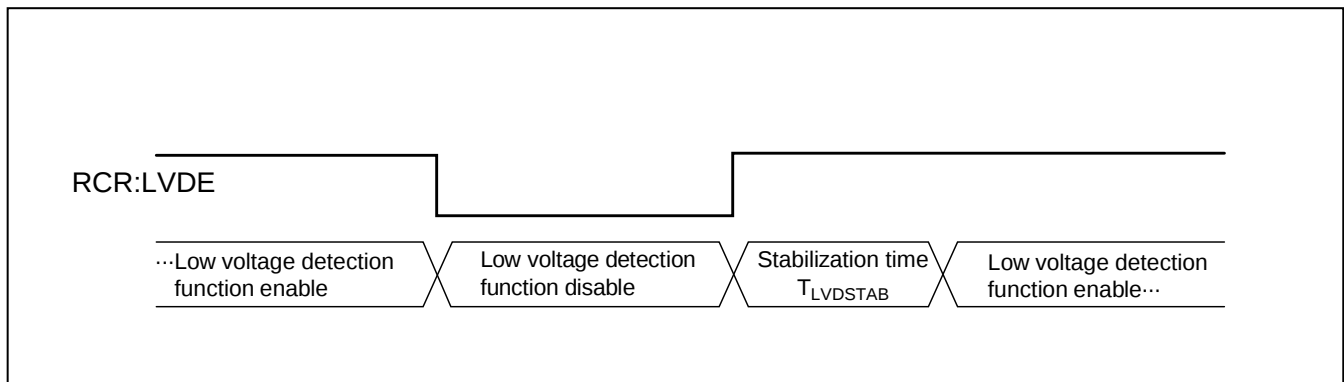
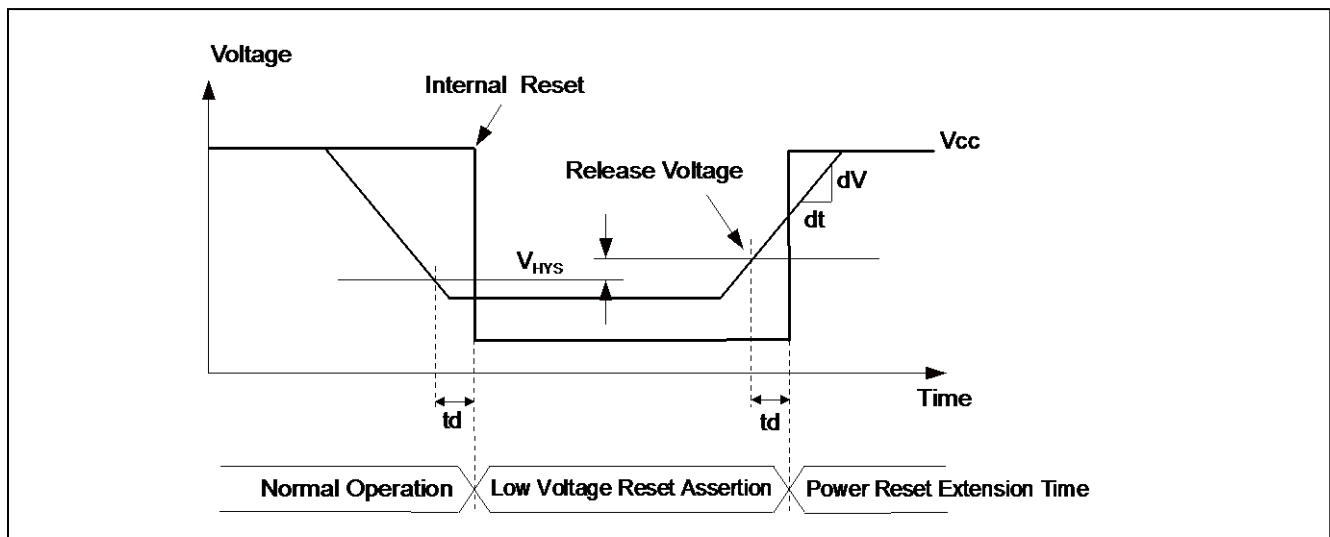
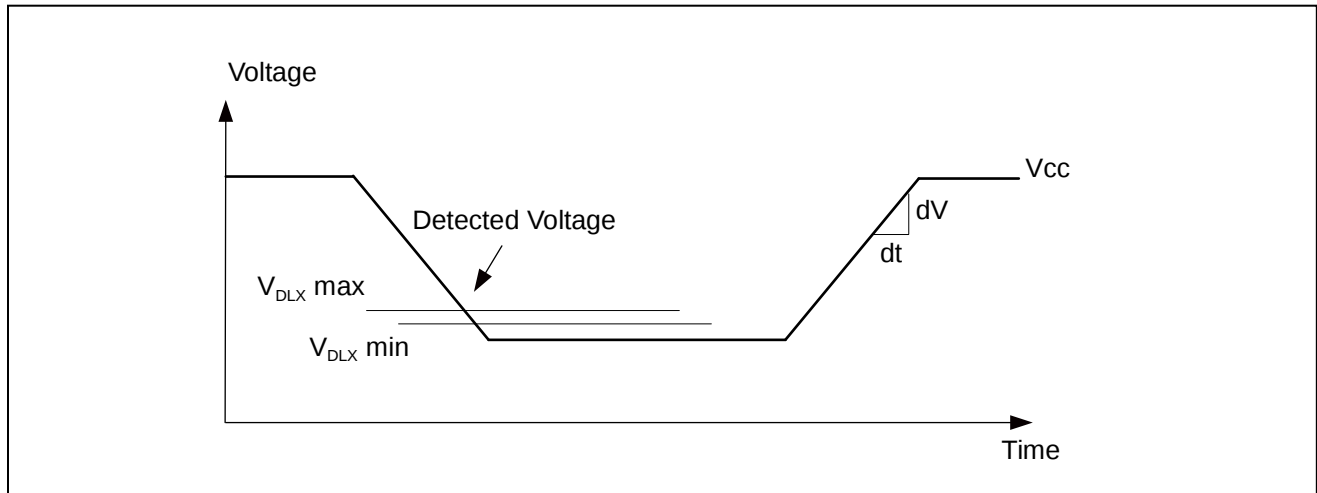


14.6 High Current Output Slew Rate

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise/fall time	t_{R30} , t_{F30}	P08_m	Outputs driving strength set to "30mA"	15	-	75	ns	$C_L=85pF$





14.8 Flash Memory Write/Erase Characteristics

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	-	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time		-	-	25	400	μs	Not including system-level overhead time.
Chip erase time		-	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage ($-0.004V/\mu s$ to $+0.004V/\mu s$) after the external power falls below the detection voltage (V_{DLX})^{*1}.

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 ^{*2}
10,000	10 ^{*2}
100,000	5 ^{*2}

*1: See "14.7 Low Voltage Detection Function Characteristics".

*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^{\circ}C$).

■ Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

18. Major Changes

Spanision Publication Number: MB96680_DS704-00002

Page	Section	Change Results
Revision 2.0		
40	Electrical Characteristics 3. DC Characteristics (1) Current Rating	Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 1880 μ A → 1800 μ A ($T_A = +25^{\circ}\text{C}$)
Revision 2.1		
-	-	Company name and layout design change
Rev.*B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
6, 8, 64, 65	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-80P-M21 → LQH080
64	16. Ordering Information	Revised Marketing Part Numbers as follows: Before) MCU with CAN controller MB96F683RBPMC-GSE1 MB96F683RBPMC-GSE2 MB96F685RBPMC-GSE1 MB96F685RBPMC-GSE2 MCU without CAN controller MB96F683ABPMC-GSE1 MB96F683ABPMC-GSE2 MB96F685ABPMC-GSE1 MB96F685ABPMC-GSE2 After) MCU with CAN controller MB96F683RBPMC-GS-UJE1 MB96F685RBPMC-GS-UJE1 MCU without CAN controller MB96F683ABPMC-GS-UJE1

NOTE: Please see “Document History” about later revised information.