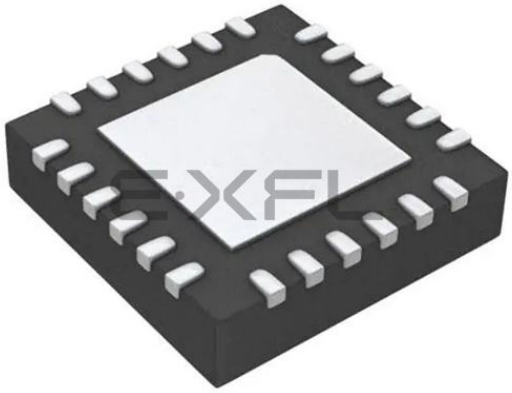

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	21
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f374-a-gm

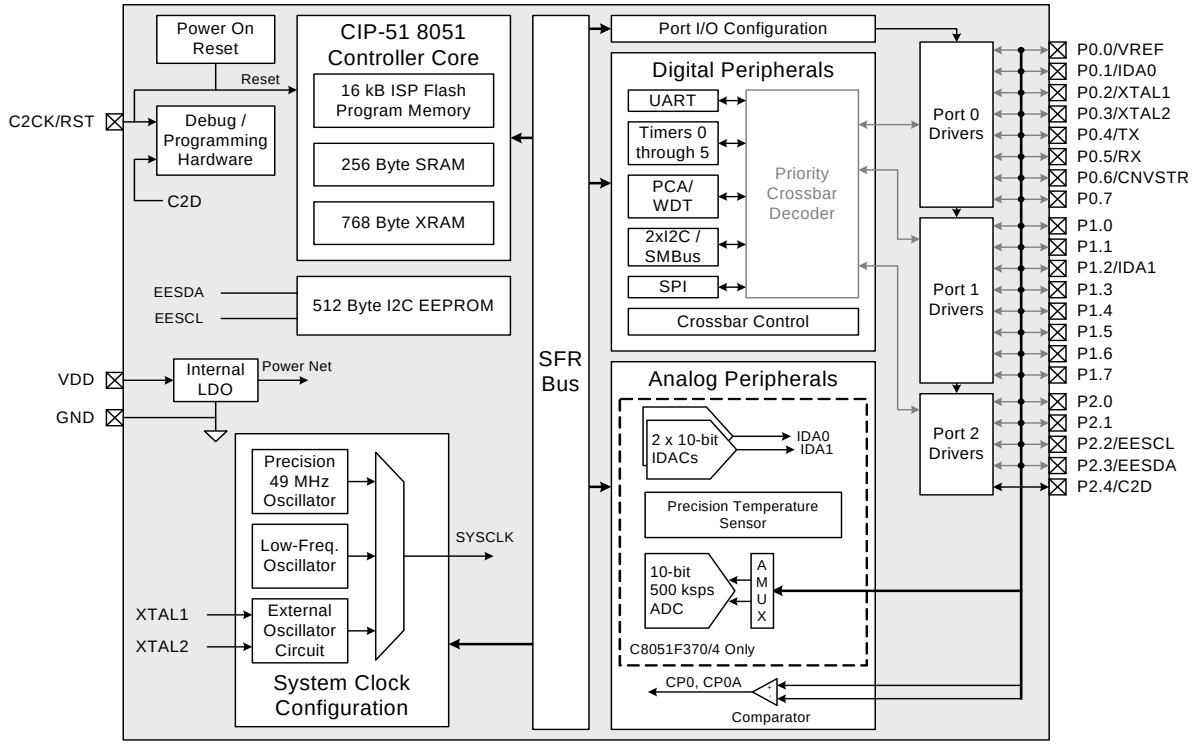


Figure 1.3. C8051F370/1/4/5 Block Diagram

Table 7.7. Internal High-Frequency Oscillator Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +105 °C (C8051F39x), –40 to +85 °C (C8051F37x), using factory-calibrated settings, unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	C8051F390/1/2/3, C8051F370/1	48	49	50	MHz
Oscillator Supply Current (from V_{DD})	C8051F394/5/6/7, C8051F374/5	—	840	880	µA
Power Supply Sensitivity	C8051F398/9	—	0.12	—	%/V
Temperature Sensitivity		—	90	—	ppm/°C

Table 7.8. Internal Low-Frequency Oscillator Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +105 °C (C8051F39x), –40 to +85 °C (C8051F37x), using factory-calibrated settings, unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	C8051F390/1/2/3, C8051F370/1	75	80	85	kHz
Oscillator Supply Current (from V_{DD})	C8051F394/5/6/7, C8051F374/5	—	5.5	12	µA
Power Supply Sensitivity	C8051F398/9	—	0.05	—	%/V
Temperature Sensitivity		—	160	—	ppm/°C

Table 7.9. Internal Low-Power Oscillator Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +105 °C (C8051F39x), –40 to +85 °C (C8051F37x), using factory-calibrated settings, unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	C8051F390/1/2/3, C8051F370/1	18.5	20	21.5	MHz
Power Supply Sensitivity	C8051F394/5/6/7, C8051F374/5	—	0.1	—	%/V
Temperature Sensitivity	C8051F398/9	—	60	—	ppm/°C

SFR Definition 8.1. TS0CN: Temperature Sensor Control

Bit	7	6	5	4	3	2	1	0
Name	TS0STRT	TS0DN				TS0CNVL		
Type	R/W	R	R/W			R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD2; SFR Page = F

Bit	Name	Function
7	TS0STRT	**Temperature Sensor Start.** Firmware must set this bit to 1, then clear this bit to 0 to start a temperature sensor measurement.
6	TS0DN	**Temperature Sensor Finished Flag.** Hardware will set TS0DN to 1 when a temperature sensor measurement is complete. If enabled, a temperature sensor interrupt will be generated. This bit must be cleared to 0 by firmware.
5:3	Reserved	Must Write 000b.
2:0	TS0CNVL	**Temperature Sensor Conversion Length.** This field sets the conversion length of time over which the temperature is calculated. A longer conversion length results in a more accurate measurement. The conversion length in microseconds is derived from the following equation, where TS0CNVL is the 3-bit value held in TS0CNVL[2:0] and F_{TS0} is the precision temperature sensor clock frequency given in Table 7.12. $$\text{Conversion Length in } \mu s = \left(\frac{256}{F_{TS0}} \times 10^6\right) \times (2^{TS0CNVL+1} + 1) + 32$$

14.1. Comparator Multiplexer

C8051F39x/37x devices include an analog input multiplexer to connect Port I/O pins to the comparator inputs. The Comparator0 inputs are selected in the CPT0MX register (SFR Definition 14.3). The CMX0P1–CMX0P0 bits select the Comparator0 positive input; the CMX0N1–CMX0N0 bits select the Comparator0 negative input. **Important Note About Comparator Inputs:** The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “27.6. Special Function Registers for Accessing and Configuring Port I/O” on page 185).

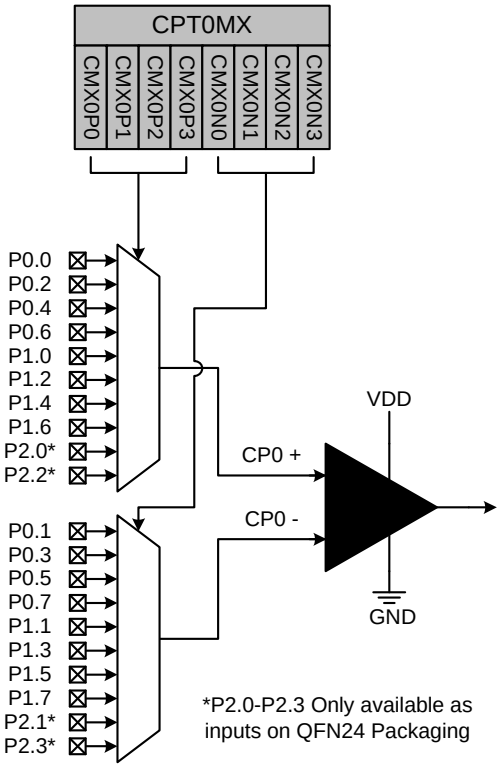


Figure 14.3. Comparator Input Multiplexer Block Diagram

SFR Definition 15.3. SP: Stack Pointer

Bit	7	6	5	4	3	2	1	0
Name	SP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	1	1	1

SFR Address = 0x81; SFR Page = All Pages

Bit	Name	Function
7:0	SP[7:0]	**Stack Pointer.** The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 15.4. ACC: Accumulator

Bit	7	6	5	4	3	2	1	0
Name	ACC[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7:0	ACC[7:0]	**Accumulator.** This register is the accumulator for arithmetic operations.

Table 19.2. Special Function Register (SFR) Memory Map

Address	Page	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
F8		SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	P0MAT	P0MASK	VDM0CN
F0		B	P0MDIN	P1MDIN	P2MDIN	CKCON1		EIP1	PCA0PWM
E8		ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	P1MAT	P1MASK	RSTSRC
E0	0	ACC	XBR0	XBR1	OSCLCN	IT01CF		EIE1	SMB0ADM
	F								SMB1ADM
D8		PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	CRC0AUTO	CRC0CNT	CRC0CN
D0	0	PSW	REF0CN	TS0DATL	TS0DATH	P0SKIP	P1SKIP	P2SKIP	SMB0ADR
	F			TS0CN	SFRSTACK				SMB1ADR
C8		TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	PCA0CLR	SFRPGCN
		TMR5CN		TMR5RLL	TMR5RLH	TMR5L	TMR5H		
C0	0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	SMBTC
	F	SMB1CN	SMB1CF	SMB1DAT					
B8	0	IP	IDA0CN	AMX0N	AMX0P	ADC0CF	ADC0L	ADC0H	EIP2
	F		IDA1CN						
B0			OSCXCN	OSCICN	OSCICL		PFE0CN	FLSCL	FLKEY
A8	0	IE	CLKSEL	EMI0CN	DERIVID	REVISION			EIE2
	F				SN0	SN1	SN2	SN3	
A0		P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	SFRPAGE
98		SCON0	SBUF0	CRC0FLIP	CPT0CN	CRC0IN	CPT0MD	CRC0DAT	CPT0MX
90	0	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	IDA0L	IDA0H
	F		TMR4CN	TMR4RLL	TMR4RLH	TMR4L	TMR4H	IDA1L	IDA1H
88		TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80		P0	SP	DPL	DPH	IPH	EIP1H	EIP2H	PCON
		0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

Notes:

1. SFR Addresses ending in 0x0 or 0x8 are bit-addressable locations and can be used with bitwise instructions.
2. Unless indicated otherwise, SFRs are available on both page 0 and page F.

20.1. MCU Interrupt Sources and Vectors

The C8051F39x/37x MCUs support 18 interrupt sources. Software can simulate an interrupt by setting any interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. MCU interrupt sources, associated vector addresses, priority order and control bits are summarized in Table 20.2. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

20.1.1. Interrupt Priorities

Each interrupt source can be individually programmed to one of four priority levels. This differs from the traditional two priority levels on the 8051 core. However, the implementation of the extra levels is backwards-compatible with legacy 8051 code.

An interrupt service routine can be preempted by any interrupt of higher priority. Interrupts at the highest priority level cannot be preempted. Each interrupt has two associated priority bits which are used to configure the priority level. For backwards compatibility, the bits are spread across two different registers. The LSBs of the priority setting are stored in the IP, EIP1 and EIP2 registers, while the MSBs are store in the IPH, EIP1H and EIP2H registers. Priority levels according to the MSB and LSB are decoded in Table 20.1. The lowest priority setting is the default for all interrupts. If two or more interrupts are recognized simultaneously, the interrupt with the highest priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate, given in Table 20.2. If legacy 8051 operation is desired, the bits of the “High” priority registers (IPH, EIP1H and EIP2H) should all be configured to 0 (this is the reset value of these registers).

Priority MSB (from IPH, EIP1H or EIP2H)	Priority LSB (from IP, EIP1 or EIP2)	Priority Level
0	0	Priority 0 (lowest priority, default)
0	1	Priority 1
1	0	Priority 2
1	1	Priority 3 (highest priority)

Table 20.1. Configurable Interrupt Priority Decoding

20.1.2. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction. If more than one interrupt is pending when the CPU exits an ISR, the CPU will service the next highest priority interrupt that is pending.

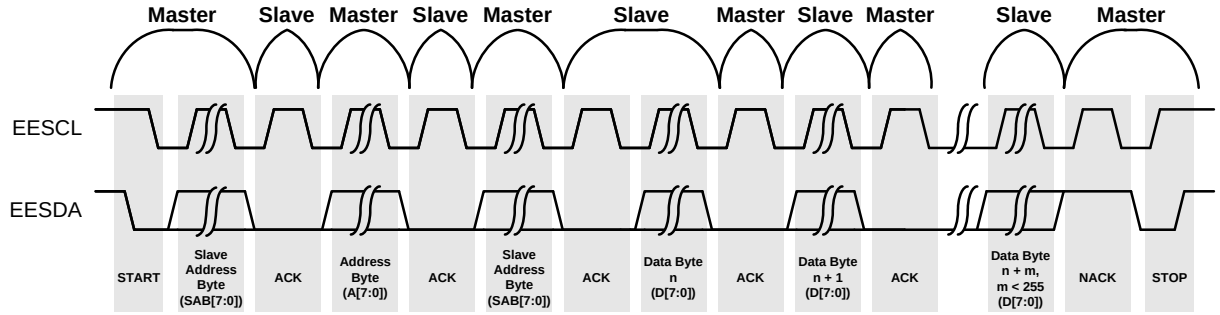


Figure 22.7. Selective Address Read (Multiple Bytes)

27.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to '1'.** Table 27.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

Table 27.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) Used for Assignment
UART0, SPI0, SMBus0, SMBus1, CP0, CP0A, SYSCLK, PCA0 (CEX0-2 and ECI), T0 or T1.	Any Port pin available for assignment by the Crossbar. This includes P0.0 - P2.3 pins which have their PnSKIP bit set to '0'. **Note:** The Crossbar will always assign UART0 pins to P0.4 and P0.5.	XBR0, XBR1
Any pin used for GPIO	P0.0 - P2.4	P0SKIP, P1SKIP, P2SKIP

27.3. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 27.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which is always at pins 4 and 5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P0.0 if VREF is used, P0.3 and/or P0.2 if the external oscillator circuit is enabled, P0.6 if the ADC or IDAC is configured to use the external conversion start signal (CNVSTR), and any selected ADC or Comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin.

Figure 27.3 shows all of the potential peripheral-to-pin assignments available to the crossbar. Note that this does not mean any peripheral can always be assigned to the highlighted pins. The actual pin assignments are determined by the priority of the enabled peripherals.

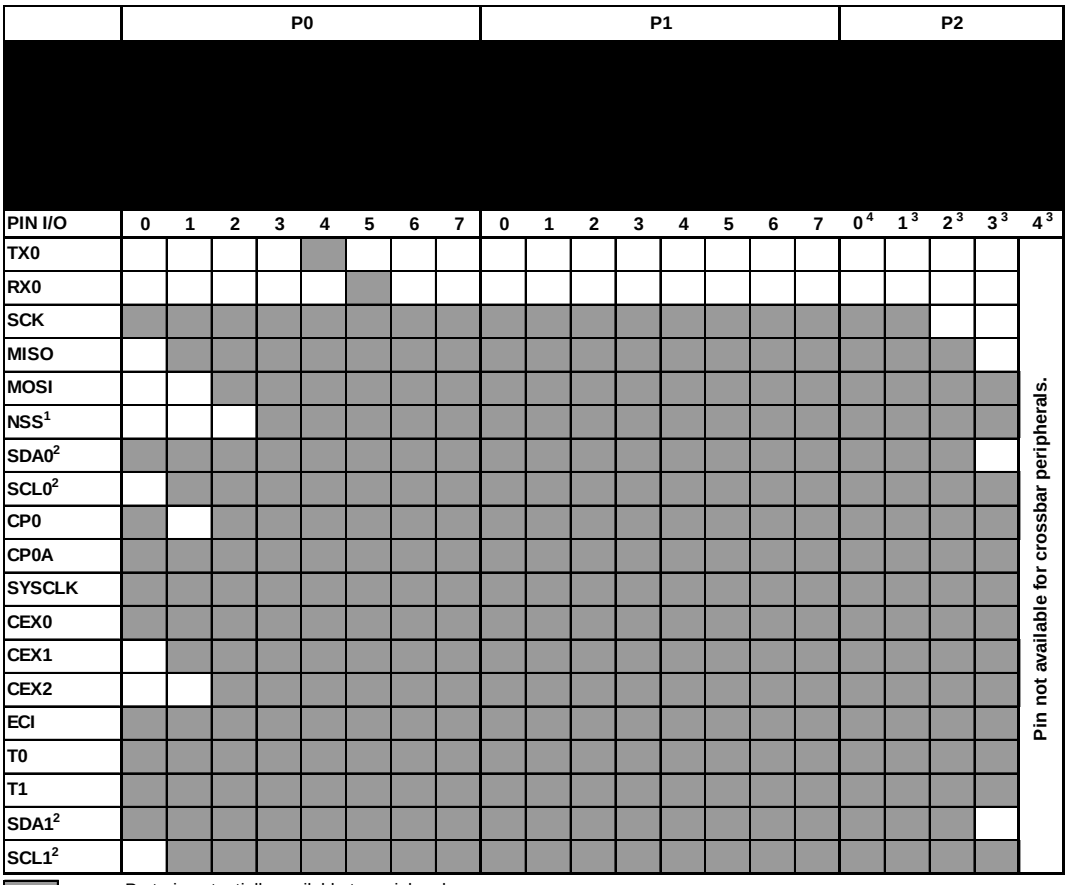


Figure 27.3. Crossbar Priority Decoder - Possible Pin Assignments

27.5. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMATCH registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMATCH registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (P0MATCH & P0MASK) or if (P1 & P1MASK) does not equal (P1MATCH & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode, such as IDLE or SUSPEND. See the Interrupts and Power Options chapters for more details on interrupt and wake-up sources.

SFR Definition 27.3. P0MASK: Port 0 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P0MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFE; SFR Page = All Pages

Bit	Name	Function
7:0	P0MASK[7:0]	**Port 0 Mask Value.** Selects P0 pins to be compared to the corresponding bits in P0MAT. 0: P0.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P0.n pin logic value is compared to P0MAT.n.

SFR Definition 27.7. P0: Port 0

Bit	7	6	5	4	3	2	1	0
Name	P0[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0x80; SFR Page = All Pages; Bit Addressable

Bit	Name	Description	Write	Read
7:0	P0[7:0]	**Port 0 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P0.n Port pin is logic LOW. 1: P0.n Port pin is logic HIGH.

SFR Definition 27.8. P0MDIN: Port 0 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF1; SFR Page = All Pages

Bit	Name	Function
7:0	P0MDIN[7:0]	**Analog Configuration Bits for P0.7–P0.0 (respectively).** Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P0.n pin is configured for analog mode. 1: Corresponding P0.n pin is not configured for analog mode.

28.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

1. The I^2C-Bus and How to Use It (including specifications), Philips Semiconductor.
2. The I^2C-Bus Specification—Version 2.0, Philips Semiconductor.
3. System Management Bus Specification—Version 1.1, SBS Implementers Forum.

28.2. SMBus Configuration

Figure 28.2 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels. However, the maximum voltage on any port pin must conform to Table 7.1. The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pullup resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively.

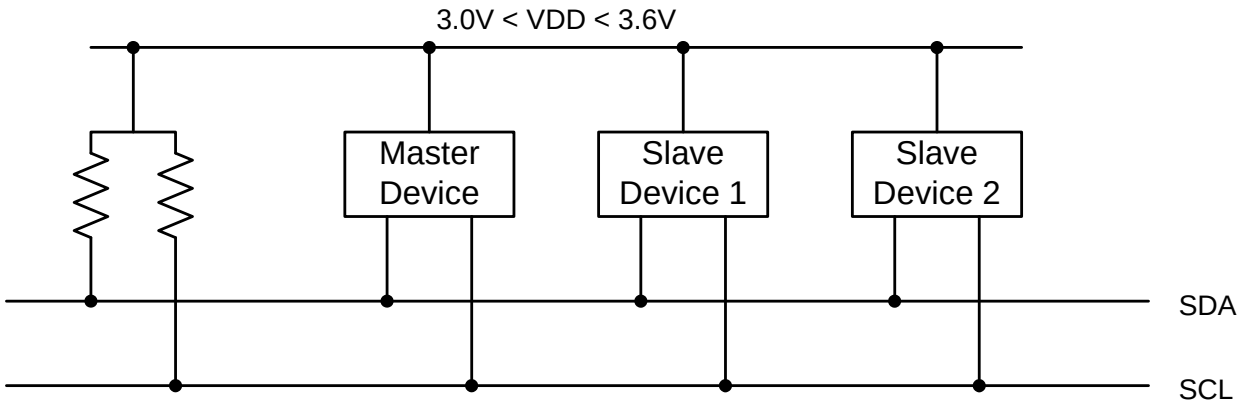


Figure 28.2. Typical SMBus Configuration

28.3. SMBus Operation

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. The SMBus interface may operate as a master or a slave, and multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. It is not necessary to specify one device as the Master in a system; any device who transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Bytes that are received (by a master or slave) are acknowledged (ACK) with a low SDA during a high SCL (see Figure 28.3). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation.

SFR Definition 28.3. SMBTC: SMBus Timing and Pin Control

Bit	7	6	5	4	3	2	1	0
Name	SMB1SWAP	SMB0SWAP			SMB1SDD[1:0]		SMB0SDD[1:0]	
Type	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC7; SFR Page = All Pages

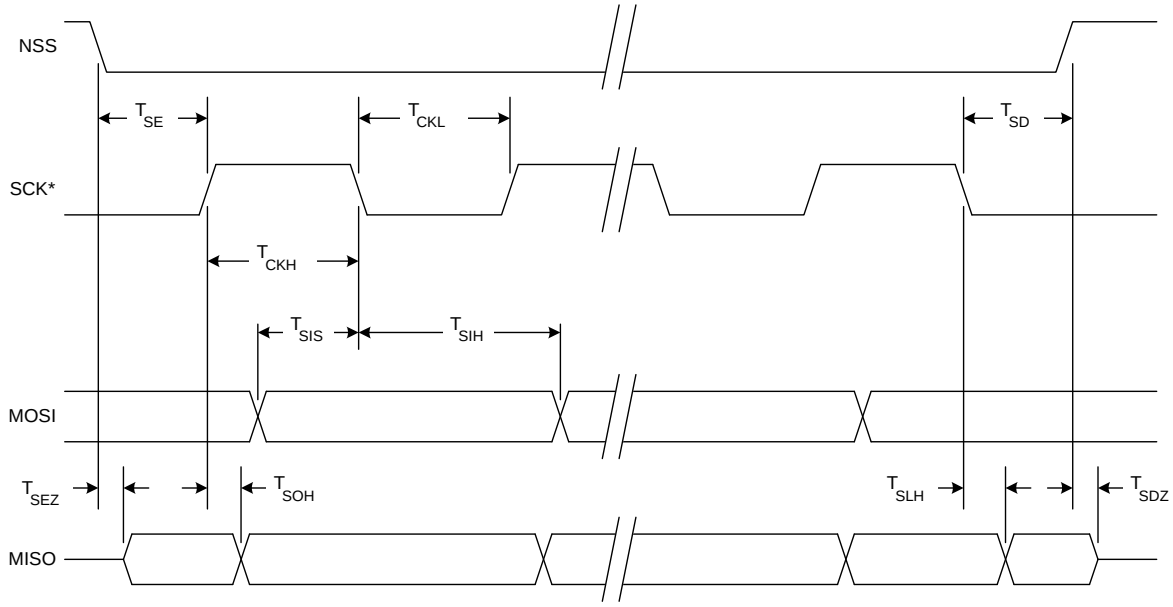
Bit	Name	Function
7	SMB1SWAP	**SMBus1 Swap Pins** This bit swaps the order of the SMBus1 pins on the cross-bar. This should be set to 1 when accessing the EEPROM. 0: SDA1 is mapped to the lower-numbered port pin, and SCL1 is mapped to the higher-numbered port pin. 1: SCL1 is mapped to the lower-numbered port pin, and SDA1 is mapped to the higher-numbered port pin.
6	SMB0SWAP	**SMBus0 Swap Pins** This bit swaps the order of the SMBus1 pins on the cross-bar. This should be set to 1 when accessing the EEPROM. 0: SDA0 is mapped to the lower-numbered port pin, and SCL0 is mapped to the higher-numbered port pin. 1: SCL0 is mapped to the lower-numbered port pin, and SDA0 is mapped to the higher-numbered port pin.
5:4	Reserved	Must Write 00b.
3:2	SMB1SDD[1:0]	**SMBus1 Start Detection Window** These bits increase the hold time requirement between SDA falling and SCL falling for START detection. 00: No additional hold time requirement (0-1 SYSCLK). 01: Increase hold time window to 2-3 SYSCLKs. 10: Increase hold time window to 4-5 SYSCLKs. 11: Increase hold time window to 8-9 SYSCLKs.
1:0	SMB0SDD[1:0]	**SMBus0 Start Detection Window** These bits increase the hold time requirement between SDA falling and SCL falling for START detection. 00: No additional hold time window (0-1 SYSCLK). 01: Increase hold time window to 2-3 SYSCLKs. 10: Increase hold time window to 4-5 SYSCLKs. 11: Increase hold time window to 8-9 SYSCLKs.

SFR Definition 28.4. SMB0CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER0	TXMODE0	STA0	STO0	ACKRQ0	ARBLOST0	ACK0	SI0
Type	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC0; SFR Page = 0; Bit-Addressable

Bit	Name	Description	Read	Write
7	MASTER0	**SMBus0 Master/Slave Indicator.** This read-only bit indicates when the SMBus0 is operating as a master.	0: SMBus0 operating in slave mode. 1: SMBus0 operating in master mode.	N/A
6	TXMODE0	**SMBus0 Transmit Mode Indicator.** This read-only bit indicates when the SMBus0 is operating as a transmitter.	0: SMBus0 in Receiver Mode. 1: SMBus0 in Transmitter Mode.	N/A
5	STA0	**SMBus0 Start Flag.**	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO0	**SMBus0 Stop Flag.**	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmitted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ0	**SMBus0 Acknowledge Request.**	0: No ACK requested 1: ACK requested	N/A
2	ARBLOST0	**SMBus0 Arbitration Lost Indicator.**	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK0	**SMBus0 Acknowledge.**	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SI0	**SMBus0 Interrupt Flag.** This bit is set by hardware under the conditions listed in Table 28.3. SI0 must be cleared by software. While SI0 is set, SCL0 is held low and the SMBus0 is stalled.	0: No interrupt pending 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event. 1: Force interrupt.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 30.11. SPI Slave Timing (CKPHA = 1)

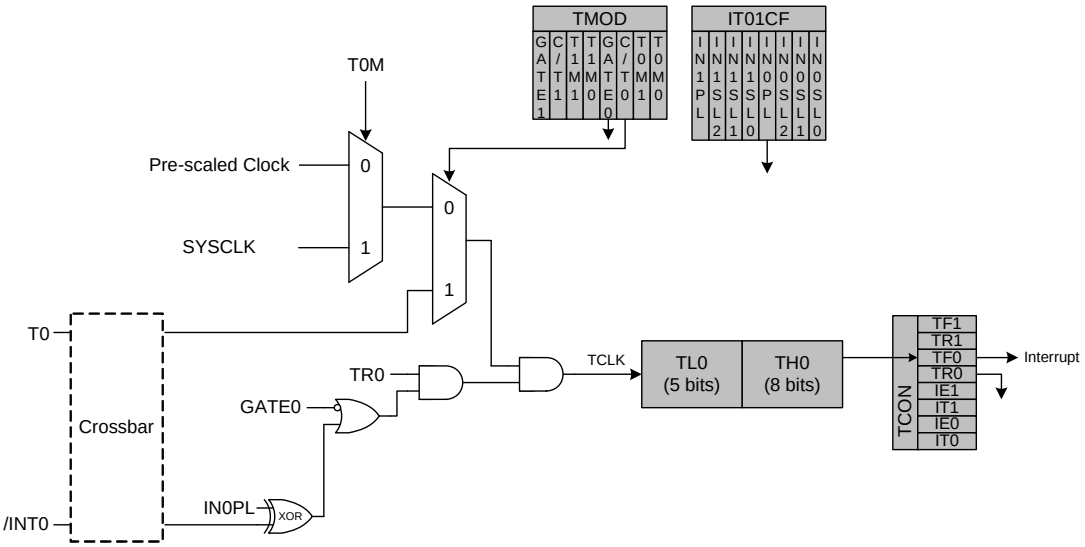


Figure 31.1. T0 Mode 0 Block Diagram

31.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

SFR Definition 31.5. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8A; SFR Page = All Pages

Bit	Name	Function
7:0	TL0[7:0]	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 31.6. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8B; SFR Page = All Pages

Bit	Name	Function
7:0	TL1[7:0]	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

32.5. Comparator Clear Function

In 8/9/10/11/16-bit PWM modes, the comparator clear function utilizes the Comparator0 output synchronized to the system clock to clear CEXn to logic low for the current PWM cycle. This comparator clear function can be enabled for each PWM channel by setting the CPCEn bits to 1 in the PCA0CLR SFR (see SFR Definition 32.4). When the comparator clear function is disabled, CEXn is unaffected. See Figure 32.12.

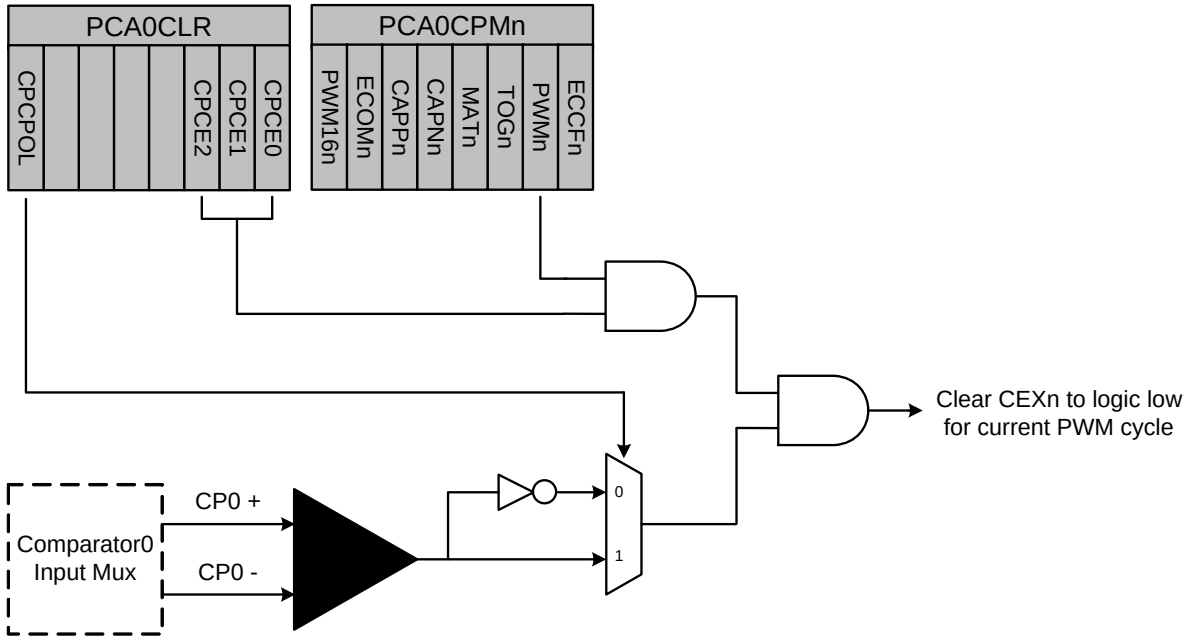


Figure 32.12. Comparator Clear Function Diagram

The asynchronous Comparator0 output is logic high when the voltage of CP0+ is greater than CP0- and logic low when the voltage of CP0+ is less than CP0-. The polarity of the Comparator0 output is used to clear CEXn as follows: when CPCPOL = 0, CEXn is forced to logic low on the falling edge of the Comparator0 output (see Figure 32.13); when CPCPOL = 0, CEXn is forced logic low on the rising edge of the Compartor0 output (see Figure 32.14).

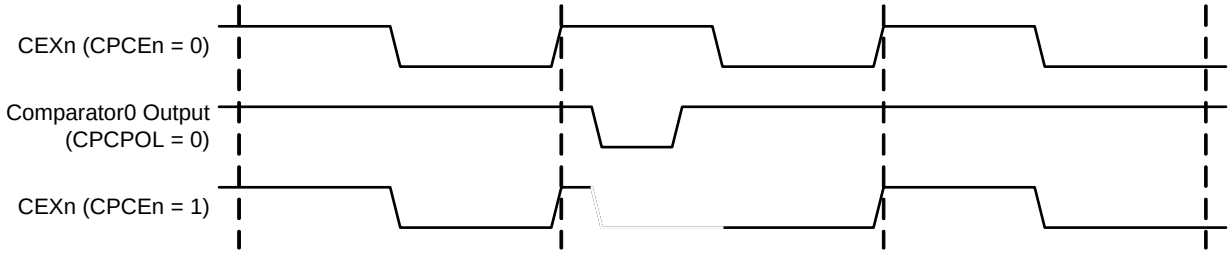


Figure 32.13. CEXn with CPCEn = 1, CPCPOL = 0