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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f390-a-gmr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 6.2. QFN-24 Recommended PCB Land Pattern

Table 6.2. QFN-24 PCB Land Pattern D	imensions
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Dimension	Min	Мах	Dimension	Min	Max
C1	3.90	4.00	X2	2.70	2.80
C2	3.90	4.00	Y1	0.65	0.75
E	0.50 BSC		Y2	2.70	2.80
X1	0.20	0.30			

Notes:

General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

- **4.** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 5. The stencil thickness should be 0.125 mm (5 mils).
- 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
- **7.** A 2 x 2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch should be used for the center pad.

Card Assembly

- 8. A No-Clean, Type-3 solder paste is recommended.
- **9.** The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



7.2. Electrical Characteristics

Table 7.2. Global Electrical Characteristics

-40 to +105 °C (C8051F39x), -40 to +85 °C (C8051F37x), 50 MHz system clock, unless otherwise specified.

Parameter	Test Condition	Min	Тур	Max	Unit
Supply Voltage (V _{DD})	Normal Operation	V _{RST} ¹	3.0	3.6	V
	Writing or Erasing Flash Memory	1.8	3.0	3.6	V
Digital Supply RAM Data Retention Voltage			1.5		V
SYSCLK (System Clock) ²		0		50	MHz
T _{SYSH} (SYSCLK High Time)		9.5			ns
T _{SYSL} (SYSCLK Low Time)		9.5			ns
Specified Operating	C8051F39x	-40	<u> </u>	+105	°C
Temperature Range	C8051F37x	-40	'	+85	°C
Digital Supply Current—CPU	Active (Normal Mode, Fetching Instru	ictions f	rom Fla	sh)	
I _{DD} ^{3, 4}	V _{DD} = 3.6 V, F = 50 MHz	<u> </u>	7.1	7.8	mA
	$V_{DD} = 3.0 V, F = 50 MHz$	-	7.0	7.7	mA
	$V_{DD} = 3.6 V, F = 25 MHz$	-	4.6	5.2	mA
	V _{DD} = 3.0 V, F = 25 MHz	-	4.5	5.1	mA
	V _{DD} = 3.6 V, F = 1 MHz	-	0.35	—	mA
	V _{DD} = 3.0 V, F = 1 MHz	-	0.35	—	mA
	V _{DD} = 3.0 V, F = 80 kHz		0.25		mA

Notes:

1. Given in Table 7.4 on page 36.

2. SYSCLK must be at least 32 kHz to enable debugging.

3. Based on device characterization data; Not production tested.

4. Digital Supply Current depends on the particular code being executed. The values in this table are obtained with the CPU executing an "sjmp \$" loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the Flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of Flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 64-byte Flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 64-byte boundary.





7.3. Typical Performance Curves









SFR Definition 15.3. SP: Stack Pointer

Bit	7	6	5	4	3	2	1	0
Name				SP[7:0]			
Туре	R/W							
Reset	0	0	0	0	0	1	1	1

SFR Address = 0x81; SFR Page = All Pages

Bit	Name	Function
7:0	SP[7:0]	Stack Pointer.
		The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 15.4. ACC: Accumulator

Bit	7	6	5	4	3	2	1	0
Name	ACC[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7:0	ACC[7:0]	Accumulator.
		This register is the accumulator for arithmetic operations.



SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	SFR Page	Description	Page
EMIOCN	0xAA	All Pages	External Memory Interface Control	96
FLKEY	0xB7	All Pages	Flash Lock and Key	138
FLSCL	0xB6	All Pages	Flash Scale	139
IDA0CN	0xB9	0	Current Mode DAC0 Control	69
IDA0H	0x97	0	Current Mode DAC0 High	70
IDA0L	0x96	0	Current Mode DAC0 Low	70
IDA1CN	0xB9	F	Current Mode DAC1 Control	71
IDA1H	0x97	F	Current Mode DAC1 High	72
IDA1L	0x96	F	Current Mode DAC1 Low	72
IE	0xA8	All Pages	Interrupt Enable	120
IP	0xB8	All Pages	Interrupt Priority	121
IPH	0x84	All Pages	Interrupt Priority High	122
IT01CF	0xE4	All Pages	INT0/INT1 Configuration	129
OSCICL	0xB3	All Pages	Internal Oscillator Calibration	166
OSCICN	0xB2	All Pages	Internal Oscillator Control	167
OSCLCN	0xE3	All Pages	Low-Frequency Oscillator Control	168
OSCXCN	0xB1	All Pages	External Oscillator Control	172
P0	0x80	All Pages	Port 0 Latch	186
POMASK	0xFE	All Pages	Port 0 Mask Configuration	183
P0MAT	0xFD	All Pages	Port 0 Match Configuration	184
POMDIN	0xF1	All Pages	Port 0 Input Mode Configuration	186
P0MDOUT	0xA4	All Pages	Port 0 Output Mode Configuration	187
P0SKIP	0xD4	All Pages	Port 0 Skip	187
P1	0x90	All Pages	Port 1 Latch	188
P1MASK	0xEE	All Pages	Port 1Mask Configuration	184
P1MAT	0xED	All Pages	Port 1 Match Configuration	185
P1MDIN	0xF2	All Pages	Port 1 Input Mode Configuration	188
P1MDOUT	0xA5	All Pages	Port 1 Output Mode Configuration	189
P1SKIP	0xD5	All Pages	Port 1 Skip	189
P2	0xA0	All Pages	Port 2 Latch	190
P2MDIN	0xF3	All Pages	Port 2 Input Mode Configuration	190
P2MDOUT	0xA6	All Pages	Port 2 Output Mode Configuration	191
P2SKIP	0xD6	All Pages	Port 2 Skip	191
PCA0CLR	0xCE	All Pages	PCA Comparator Clear Control	293



SFR Definition 20.6. EIP1H: Extended Interrupt Priority 1 High

Bit	7	6	5	4	3	2	1	0
Name	PHT3		PHCP0	PHPCA0	PHADC0	PHWADC0	PHMAT	PHSMB0
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x85; SFR Page = All Pages

Bit	Name	Function
7	PHT3	Timer 3 Interrupt Priority Control MSB.
		This bit sets the MSB of the priority field for the Timer 3 interrupt.
6	Reserved	Reserved. Must Write 0.
5	PHCP0	Comparator0 (CP0) Interrupt Priority Control MSB.
		This bit sets the MSB of the priority field for the CP0 interrupt.
4	PHPCA0	Programmable Counter Array (PCA0) Interrupt Priority Control MSB.
		This bit sets the MSB of the priority field for the PCA0 interrupt.
3	PHADC0	ADC0 Conversion Complete Interrupt Priority Control MSB.
		This bit sets the MSB of the priority field for the ADC0 Conversion Complete interrupt.
2	PHWADC0	ADC0 Window Comparator Interrupt Priority Control MSB.
		This bit sets the MSB of the priority field for the ADC0 Window interrupt.
1	PHMAT	Port Match Interrupt Priority Control MSB.
		This bit sets the MSB of the priority field for the Port Match Event interrupt.
0	PHSMB0	SMBus (SMB0) Interrupt Priority Control MSB.
		This bit sets the MSB of the priority field for the SMB0 interrupt.



SFR Definition 20.10. IT01CF: INT0/INT1 Configuration

Bit	7	6	5	4	3	2	1	0
Name	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]		
Туре	R/W	R/W			R/W		R/W	
Reset	0	0	0	0	0	0	0	1

SFR Address = 0xE4; SFR Page = All Pages



SFR Definition 21.2. FLKEY: Flash Lock and Key

Bit	7	6	5	4	3	2	1	0
Name	FLKEY[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB7; SFR Page = All Pages

Bit	Name	Function
7:0	FLKEY[7:0]	Flash Lock and Key Register.
7:0	FLKEY[7:0]	Flash Lock and Key Register. Write: This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is com- plete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these opera- tions are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software. Read: When read, bits 1–0 indicate the current Flash lock state.
		00: Flash is write/erase locked.
		10: Flash is unlocked (writes/erases allowed).
		11: Flash writes/erases disabled until the next reset.



23. Cyclic Redundancy Check Unit (CRC0)

C8051F39x/37x devices include a cyclic redundancy check unit (CRC0) that can perform a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data written to the CRC0IN register. CRC0 posts the 16-bit result to an internal register. The internal result register may be accessed indirectly using the CRC0PNT bits and CRC0DAT register, as shown in Figure 23.1. CRC0 also has a bit reverse register for quick data manipulation.



Figure 23.1. CRC0 Block Diagram

23.1. CRC Algorithm

The C8051F39x/37x CRC unit generates a CRC result equivalent to the following algorithm:

- XOR the input with the most-significant bits of the current CRC result. If this is the first iteration of the CRC unit, the current CRC result will be the set initial value (0x00000000 or 0xFFFFFFF).
- 2a. If the MSB of the CRC result is set, shift the CRC result and XOR the result with the selected polynomial.
- 2b. If the MSB of the CRC result is not set, shift the CRC result.

Repeat Steps 2a/2b for the number of input bits (8). The algorithm is also described in the following example.



24.1. Power-On Reset

During power-up, the device is held in a reset state and the \overline{RST} pin is driven low until V_{DD} settles above V_{RST}. A delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 24.2. plots the power-on and V_{DD} monitor reset timing. The maximum V_{DD} ramp time is 1 ms; slower ramp times may cause the device to be released from reset before V_{DD} reaches the V_{RST} level. For ramp times less than 1 ms, the power-on reset delay (T_{PORDelay}) is typically less than 0.3 ms.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.



Figure 24.2. Power-On and V_{DD} Monitor Reset Timing



24.3. External Reset

The external RST pin provides a means for external circuitry to force the device into a reset state. Asserting an active-low signal on the RST pin generates a reset; an external pullup and/or decoupling of the RST pin may be necessary to avoid erroneous noise-induced resets. See Section "7. Electrical Characteristics" on page 32 for complete RST pin specifications. The PINRSF flag (RSTSRC.0) is set on exit from an external reset.

24.4. Missing Clock Detector Reset

The Missing Clock Detector (MCD) is a one-shot circuit that is triggered by the system clock. If the system clock remains high or low for more than 100 μ s, the one-shot will time out and generate a reset. After a MCD reset, the MCDRSF flag (RSTSRC.2) will read '1', signifying the MCD as the reset source; otherwise, this bit reads '0'. Writing a '1' to the MCDRSF bit enables the Missing Clock Detector; writing a '0' disables it. The state of the RST pin is unaffected by this reset.

24.5. Comparator0 Reset

Comparator0 can be configured as a reset source by writing a '1' to the CORSEF flag (RSTSRC.5). Comparator0 should be enabled and allowed to settle prior to writing to CORSEF to prevent any turn-on chatter on the output from generating an unwanted reset. The Comparator0 reset is active-low: if the non-inverting input voltage (on CP0+) is less than the inverting input voltage (on CP0-), the device is put into the reset state. After a Comparator0 reset, the CORSEF flag (RSTSRC.5) will read '1' signifying Comparator0 as the reset source; otherwise, this bit reads '0'. The state of the RST pin is unaffected by this reset.

24.6. PCA Watchdog Timer Reset

The programmable Watchdog Timer (WDT) function of the Programmable Counter Array (PCA) can be used to prevent software from running out of control during a system malfunction. The PCA WDT function can be enabled or disabled by software as described in Section "32.4. Watchdog Timer Mode" on page 286; the WDT is enabled and clocked by SYSCLK / 12 following any reset. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit (RSTSRC.5) is set to '1'. The state of the RST pin is unaffected by this reset.

24.7. Flash Error Reset

If a Flash read/write/erase or program read targets an illegal address, a system reset is generated. This may occur due to any of the following:

- A Flash write or erase is attempted above user code space. This occurs when PSWE is set to '1' and a MOVX write operation targets an address above address 0x3DFF.
- A Flash read is attempted above user code space. This occurs when a MOVC operation targets an address above address 0x3DFF.
- A Program read is attempted above user code space. This occurs when user code attempts to branch to an address above 0x3DFF.
- A Flash read, write or erase attempt is restricted due to a Flash security setting (see Section "21.3. Security Options" on page 133).

The FERROR bit (RSTSRC.6) is set following a Flash error reset. The state of the \overline{RST} pin is unaffected by this reset.

24.8. Software Reset

Software may force a reset by writing a '1' to the SWRSF bit (RSTSRC.4). The SWRSF bit will read '1' following a software forced reset. The state of the RST pin is unaffected by this reset.



25. Power Management Modes

The C8051F39x/37x devices have three software programmable power management modes: idle, stop, and Suspend. Idle mode and stop mode are part of the standard 8051 architecture, while suspend mode is an enhanced power-saving mode implemented by the high-speed oscillator.

Idle mode halts the CPU while leaving the peripherals and clocks active. In stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the internal oscillator is stopped (analog peripherals remain in their selected states; the external oscillator is not affected). Suspend mode is similar to Stop mode in that the internal oscillator and CPU are halted, but the device can wake on events such as a Port Mismatch, Comparator low output, or a Timer 3 overflow. Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode and suspend mode consume the least power because the majority of the device is shut down with no clocks active. SFR Definition 25.1 describes the Power Control Register (PCON) used to control the C8051F39x/37x's Stop and Idle power management modes. Suspend mode is controlled by the SUSPEND bit in the OSCICN register (SFR Definition 26.3).

Although the C8051F39x/37x has idle, stop, and suspend modes available, more control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers or serial buses, draw little power when they are not in use. Turning off oscillators lowers power consumption considerably, at the expense of reduced functionality.

25.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the hardware to halt the CPU and enter idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Therefore, instructions that set the IDLE bit should be followed by an instruction that has two or more opcode bytes, for example:

<pre>// in `C': PCON = 0x01; PCON = PCON;</pre>	// set IDLE bit // followed by a 3-cycle dummy instruction
; in assembly: ORL PCON, #01h MOV PCON, PCON	; set IDLE bit ; followed by a 3-cycle dummy instruction

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to Section "24.6. PCA Watchdog Timer Reset" on page 159 for more information on the use and configuration of the WDT.



27.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital func-tions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to '1'**. Table 27.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

Digital Function	Potentially Assignable Port Pins	SFR(s) Used for Assignment
UART0, SPI0, SMBus0, SMBus1, CP0, CP0A, SYSCLK, PCA0 (CEX0-2 and ECI), T0 or T1.	Any Port pin available for assignment by the Crossbar. This includes P0.0 - P2.3 pins which have their PnSKIP bit set to '0'. Note: The Crossbar will always assign UART0 pins to P0.4 and P0.5.	XBR0, XBR1
Any pin used for GPIO	P0.0 - P2.4	P0SKIP, P1SKIP, P2SKIP



27.3. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 27.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which is always at pins 4 and 5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P0.0 if VREF is used, P0.3 and/or P0.2 if the external oscillator circuit is enabled, P0.6 if the ADC or IDAC is configured to use the external conversion start signal (CNVSTR), and any selected ADC or Comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin.

Figure 27.3 shows all of the potential peripheral-to-pin assignments available to the crossbar. Note that this does not mean any peripheral can always be assigned to the highlighted pins. The actual pin assignments are determined by the priority of the enabled peripherals.



5. C8051F37x only

Figure 27.3. Crossbar Priority Decoder - Possible Pin Assignments



SFR Definition 28.4. SMB0CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER0	TXMODE0	STA0	STO0	ACKRQ0	ARBLOST0	ACK0	SI0
Туре	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC0; SFR Page = 0; Bit-Addressable

Bit	Name	Description	Read	Write
7	MASTER0	SMBus0 Master/Slave Indicator. This read-only bit indicates when the SMBus0 is operating as a master.	0: SMBus0 operating in slave mode. 1: SMBus0 operating in master mode.	N/A
6	TXMODE0	SMBus0 Transmit Mode Indicator. This read-only bit indicates when the SMBus0 is operating as a transmitter.	0: SMBus0 in Receiver Mode. 1: SMBus0 in Transmitter Mode.	N/A
5	STA0	SMBus0 Start Flag.	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO0	SMBus0 Stop Flag.	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmit- ted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ0	SMBus0 Acknowledge Request.	0: No ACK requested 1: ACK requested	N/A
2	ARBLOST0	SMBus0 Arbitration Lost Indicator.	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK0	SMBus0 Acknowledge.	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SIO	SMBus0 Interrupt Flag. This bit is set by hardware under the conditions listed in Table 28.3. SI0 must be cleared by software. While SI0 is set, SCL0 is held low and the SMBus0 is stalled.	0: No interrupt pending 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event.1: Force interrupt.



30.1. Signal Descriptions

The four signals used by SPI0 (MOSI, MISO, SCK, NSS) are described below.

30.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI0 is operating as a master and an input when SPI0 is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

30.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI0 is operating as a master and an output when SPI0 is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

30.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. SPI0 generates this signal when operating as a master. The SCK signal is ignored by a SPI slave when the slave is not selected (NSS = 1) in 4-wire slave mode.

30.1.4. Slave Select (NSS)

The function of the slave-select (NSS) signal is dependent on the setting of the NSSMD1 and NSSMD0 bits in the SPI0CN register. There are three possible modes that can be selected with these bits:

- 1. NSSMD[1:0] = 00: 3-Wire Master or 3-Wire Slave Mode: SPI0 operates in 3-wire mode, and NSS is disabled. When operating as a slave device, SPI0 is always selected in 3-wire mode. Since no select signal is present, SPI0 must be the only slave on the bus in 3-wire mode. This is intended for point-to-point communication between a master and one slave.
- NSSMD[1:0] = 01: 4-Wire Slave or Multi-Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an input. When operating as a slave, NSS selects the SPI0 device. When operating as a master, a 1-to-0 transition of the NSS signal disables the master function of SPI0 so that multiple master devices can be used on the same SPI bus.
- 3. NSSMD[1:0] = 1x: 4-Wire Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an output. The setting of NSSMD0 determines what logic level the NSS pin will output. This configuration should only be used when operating SPI0 as a master device.

See Figure 30.2, Figure 30.3, and Figure 30.4 for typical connection diagrams of the various operational modes. **Note that the setting of NSSMD bits affects the pinout of the device.** When in 3-wire master or 3-wire slave mode, the NSS pin will not be mapped by the crossbar. In all other modes, the NSS signal will be mapped to a pin on the device. See Section "27. Port Input/Output" on page 173 for general purpose port I/O and crossbar information.



SFR Definition 30.4. SPI0DAT: SPI0 Data

Bit	7	6	5	4	3	2	1	0
Name	SPI0DAT[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA3; SFR Page = All Pages

Bit	Name	Function
7:0	SPI0DAT[7:0]	SPI0 Transmit and Receive Data.
		The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 30.8. SPI Master Timing (CKPHA = 0)



SFR Definition 31.10. TMR2RLL: Timer 2 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLL[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCA; SFR Page = 0

Bit	Name	Function
7:0	TMR2RLL[7:0]	Timer 2 Reload Register Low Byte.
		TMR2RLL holds the low byte of the reload value for Timer 2.

SFR Definition 31.11. TMR2RLH: Timer 2 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLH[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCB; SFR Page = 0

Bit	Name	Function		
7:0	TMR2RLH[7:0]	Timer 2 Reload Register High Byte.		
		TMR2RLH holds the high byte of the reload value for Timer 2.		

SFR Definition 31.12. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCC; SFR Page = 0

Bit	Name	Function
7:0	TMR2L[7:0]	Timer 2 Low Byte.
		In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.



31.3. Timer 3

Timer 3 is a 16-bit timer formed by two 8-bit SFRs: TMR3L (low byte) and TMR3H (high byte). Timer 3 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T3SPLIT bit (TMR3CN.3) defines the Timer 3 operation mode.

Timer 3 may be clocked by the system clock, the system clock divided by 12, the external oscillator source divided by 8, or the internal low-frequency oscillator divided by 8. The external clock mode is ideal for realtime clock (RTC) functionality, where the internal high-frequency oscillator drives the system clock while Timer 3 is clocked by an external oscillator source. Note that the external oscillator source divided by 8 and the LFO source divided by 8 are synchronized with the system clock when in all operating modes except suspend. When the internal oscillator is placed in suspend mode, The external clock/8 signal or the LFO/8 output can directly drive the timer. This allows the use of an external clock or the LFO to wake up the device from suspend mode. The timer will continue to run in suspend mode and count up. When the timer overflow occurs, the device will wake from suspend mode, and begin executing code again. The timer value may be set prior to entering suspend, to overflow in the desired amount of time (number of clocks) to wake the device. If a wake-up source other than the timer wakes the device from suspend mode, it may take up to three timer clocks before the timer registers can be read or written. During this time, the STSYNC bit in register OSCICN will be set to 1, to indicate that it is not safe to read or write the timer registers.

Important Note: In internal LFO/8 mode, the divider for the internal LFO must be set to 1 for proper functionality. The timer will not operate if the LFO divider is not set to 1.

31.3.1. 16-bit Timer with Auto-Reload

When T3SPLIT (TMR3CN.3) is zero, Timer 3 operates as a 16-bit timer with auto-reload. Timer 3 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 3 reload registers (TMR3RLH and TMR3RLL) is loaded into the Timer 3 register as shown in Figure 31.7, and the Timer 3 High Byte Overflow Flag (TMR3CN.7) is set. If Timer 3 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 3 overflow. Additionally, if Timer 3 interrupts are enabled and the TF3LEN bit is set (TMR3CN.5), an interrupt will be generated each time the lower 8 bits (TMR3L) overflow from 0xFF to 0x00.



Figure 31.7. Timer 3 16-Bit Mode Block Diagram



32.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/ timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.



Figure 32.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

