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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f393-a-gm

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Name	Pin 'F392/3/6/ 7/8/9	Pin 'F390/1/ 4/5	Pin 'F370/1/ 4/5	Type	Description
P2.2	—	8	—	D I/O or A In	Port 2.2.
P2.2 EESCL	-	—	8	D I/O or A In D I/O	Port 2.2. EEPROM SCL Connection.
P2.3	—	7	—	D I/O or A In	Port 2.3.
P2.3 EESDA	-	—	7	D I/O or A In D I/O	Port 2.3. EEPROM SDA Connection.
P2.4	—	6	6	D I/O	Port 2.4. (Also C2D on 24-pin Packaging)

Table 7.11. ADC Temperature Sensor Electrical Characteristics

$V_{DD} = 3.0\text{ V}$, -40 to $+105\text{ }^{\circ}\text{C}$ (C8051F39x), -40 to $+85\text{ }^{\circ}\text{C}$ (C8051F37x), unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Linearity		—	0.75	—	$^{\circ}\text{C}$
Slope		—	2.92	—	$\text{mV}/^{\circ}\text{C}$
Slope Error*		—	70	—	$\mu\text{V}/^{\circ}\text{C}$
Offset	Temp = $0\text{ }^{\circ}\text{C}$	—	785	—	mV
Offset Error*	Temp = $0\text{ }^{\circ}\text{C}$	—	13	—	mV
Supply Current		—	90	120	μA
Note: Represents one standard deviation from the mean.					

Table 7.12. Precision Temperature Sensor Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V , -40 to $+105\text{ }^{\circ}\text{C}$ (C8051F39x), -40 to $+85\text{ }^{\circ}\text{C}$ (C8051F37x), unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Range		-40	—	105	$^{\circ}\text{C}$
Absolute Error		-2	0.2	+2	$^{\circ}\text{C}$
Integral Nonlinearity		—	0	± 0.4	$^{\circ}\text{C}$
Resolution		0.0078125			$^{\circ}\text{C}$
Power Supply Rejection		—	0.05	0.2	$^{\circ}\text{C}/\text{V}$
Supply Current		—	230	280	μA
Clock Frequency (F_{TS0})		320	520	730	kHz

C8051F39x/37x

Table 7.16. Comparator Electrical Characteristics

$V_{DD} = 3.0\text{ V}$, -40 to $+105\text{ }^{\circ}\text{C}$ (C8051F39x), -40 to $+85\text{ }^{\circ}\text{C}$ (C8051F37x), unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Response Time Mode 0, $V_{cm}^* = 1.5\text{ V}$	CP0+ – CP0– = 100 mV	—	370	—	ns
	CP0+ – CP0– = –100 mV	—	135	—	ns
Response Time Mode 3, $V_{cm}^* = 1.5\text{ V}$	CP0+ – CP0– = 100 mV	—	1575	—	ns
	CP0+ – CP0– = –100 mV	—	3705	—	ns
Common-Mode Rejection Ratio		—	0.6	5	mV/V
Positive Hysteresis Mode 0 (CPMD = 00)	CP0HYP1–0 = 00	—	0.5	—	mV
	CP0HYP1–0 = 01	—	8	—	mV
	CP0HYP1–0 = 10	—	16	—	mV
	CP0HYP1–0 = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	CP0HYN1–0 = 00	—	0.5	—	mV
	CP0HYN1–0 = 01	—	–8	—	mV
	CP0HYN1–0 = 10	—	–16	—	mV
	CP0HYN1–0 = 11	—	–32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	CP0HYP1–0 = 00	—	0.5	—	mV
	CP0HYP1–0 = 01	—	6	—	mV
	CP0HYP1–0 = 10	—	12	—	mV
	CP0HYP1–0 = 11	—	24.5	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	CP0HYN1–0 = 00	—	0.5	—	mV
	CP0HYN1–0 = 01	—	–6	—	mV
	CP0HYN1–0 = 10	—	–12	—	mV
	CP0HYN1–0 = 11	—	–24.5	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	CP0HYP1–0 = 00	—	0.7	—	mV
	CP0HYP1–0 = 01	—	4.5	—	mV
	CP0HYP1–0 = 10	—	10	—	mV
	CP0HYP1–0 = 11	—	19	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	CP0HYN1–0 = 00	—	0.7	—	mV
	CP0HYN1–0 = 01	—	–4.5	—	mV
	CP0HYN1–0 = 10	—	–10	—	mV
	CP0HYN1–0 = 11	—	–19	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	CP0HYP1–0 = 00	—	1.6	2.3	mV
	CP0HYP1–0 = 01	2	4	6	mV
	CP0HYP1–0 = 10	4.8	8	11	mV
	CP0HYP1–0 = 11	10	15.5	21	mV

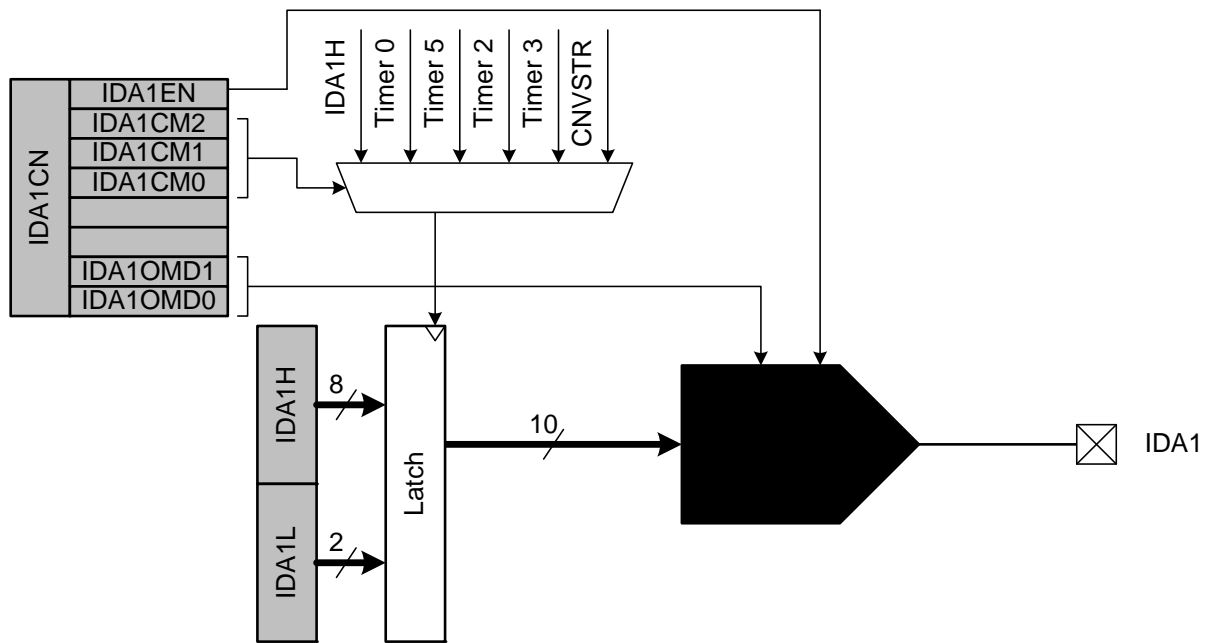


Figure 11.2. IDA1 Functional Block Diagram

15. CIP-51 Microcontroller

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. The CIP-51 also includes on-chip debug hardware (see description in Section 33), and interfaces directly with the analog and digital subsystems providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 15.1 for a block diagram). The CIP-51 includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 50 MIPS Peak Throughput with 49 MHz Clock
- 0 to 49 MHz Clock Frequency
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- On-chip Debug Logic
- Program and Data Memory Security

Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

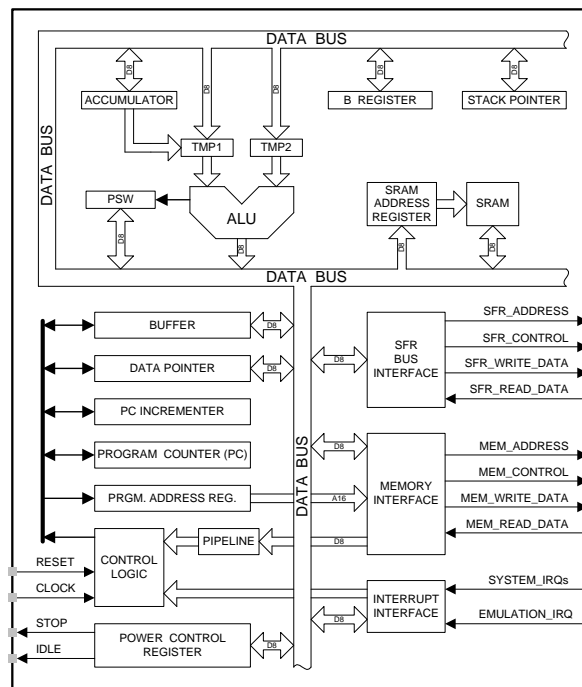


Figure 15.1. CIP-51 Block Diagram

SFR Definition 26.5. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	XCLKVLD	XOSCMD[2:0]				XFCN[2:0]		
Type	R	R/W			R	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB1; SFR Page = All Pages

Bit	Name	Function																																				
7	XCLKVLD	External Oscillator Valid Flag. Provides External Oscillator status and is valid at all times for all modes of operation except External CMOS Clock Mode and External CMOS Clock Mode with divide by 2. In these modes, XCLKVLD always returns 0. 0: External Oscillator is unused or not yet stable. 1: External Oscillator is running and stable.																																				
6:4	XOSCMD[2:0]	External Oscillator Mode Select. 00x: External Oscillator circuit off. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide-by-2 stage. 100: RC Oscillator Mode with divide-by-2 stage. 101: Capacitor Oscillator Mode with divide-by-2 stage. 110: Crystal Oscillator Mode. 111: Crystal Oscillator Mode with divide-by-2 stage.																																				
3	Unused	Read = 0; Write = don't care																																				
2:0	XFCN[2:0]	External Oscillator Frequency Control Bits. Set according to the desired frequency for RC mode. Set according to the desired K Factor for C mode. <table><tr><th>XFCN</th><th>Crystal Mode</th><th>RC Mode</th><th>C Mode</th></tr><tr><td>000</td><td>f ≤ 20 kHz</td><td>f ≤ 25 kHz</td><td>K Factor = 0.87</td></tr><tr><td>001</td><td>20 kHz < f ≤ 58 kHz</td><td>25 kHz < f ≤ 50 kHz</td><td>K Factor = 2.6</td></tr><tr><td>010</td><td>58 kHz < f ≤ 155 kHz</td><td>50 kHz < f ≤ 100 kHz</td><td>K Factor = 7.8</td></tr><tr><td>011</td><td>155 kHz < f ≤ 415 kHz</td><td>100 kHz < f ≤ 200 kHz</td><td>K Factor = 22</td></tr><tr><td>100</td><td>415 kHz < f ≤ 1.1 MHz</td><td>200 kHz < f ≤ 400 kHz</td><td>K Factor = 66</td></tr><tr><td>101</td><td>1.1 MHz < f ≤ 3.1 MHz</td><td>400 kHz < f ≤ 800 kHz</td><td>K Factor = 189</td></tr><tr><td>110</td><td>3.1 MHz < f ≤ 8.2 MHz</td><td>800 kHz < f ≤ 1.6 MHz</td><td>K Factor = 741</td></tr><tr><td>111</td><td>8.2 MHz < f ≤ 25 MHz</td><td>1.6 MHz < f ≤ 3.2 MHz</td><td>K Factor = 2222</td></tr></table>	XFCN	Crystal Mode	RC Mode	C Mode	000	f ≤ 20 kHz	f ≤ 25 kHz	K Factor = 0.87	001	20 kHz < f ≤ 58 kHz	25 kHz < f ≤ 50 kHz	K Factor = 2.6	010	58 kHz < f ≤ 155 kHz	50 kHz < f ≤ 100 kHz	K Factor = 7.8	011	155 kHz < f ≤ 415 kHz	100 kHz < f ≤ 200 kHz	K Factor = 22	100	415 kHz < f ≤ 1.1 MHz	200 kHz < f ≤ 400 kHz	K Factor = 66	101	1.1 MHz < f ≤ 3.1 MHz	400 kHz < f ≤ 800 kHz	K Factor = 189	110	3.1 MHz < f ≤ 8.2 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 741	111	8.2 MHz < f ≤ 25 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 2222
XFCN	Crystal Mode	RC Mode	C Mode																																			
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011	155 kHz < f ≤ 415 kHz	100 kHz < f ≤ 200 kHz	K Factor = 22																																			
100	415 kHz < f ≤ 1.1 MHz	200 kHz < f ≤ 400 kHz	K Factor = 66																																			
101	1.1 MHz < f ≤ 3.1 MHz	400 kHz < f ≤ 800 kHz	K Factor = 189																																			
110	3.1 MHz < f ≤ 8.2 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 741																																			
111	8.2 MHz < f ≤ 25 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 2222																																			

SFR Definition 27.1. XBR0: Port I/O Crossbar Register 0

Bit	7	6	5	4	3	2	1	0
Name	EEPUE	SMB1E	CP0AE	CP0E	SYSCKE	SMB0E	SPI0E	URT0E
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE1; SFR Page = All Pages

Bit	Name	Function
7	EEPUE	EEPROM Pullup Enable. 0: On-chip strong pullups not active. 1: On-chip strong pullups active on pins P2.2 and P2.3.
6	SMB1E	SMBus1 I/O Enable. 0: SMBus1 I/O unavailable at Port pins. 1: SMBus1 I/O routed to Port pins.
5	CP0AE	Comparator0 Asynchronous Output Enable. 0: Asynchronous CP0 unavailable at Port pin. 1: Asynchronous CP0 routed to Port pin.
4	CP0E	Comparator0 Output Enable. 0: CP0 unavailable at Port pin. 1: CP0 routed to Port pin.
3	SYSCKE	/SYSCLK Output Enable. 0: /SYSCLK unavailable at Port pin. 1: /SYSCLK output routed to Port pin.
2	SMB0E	SMBus0 I/O Enable. 0: SMBus0 I/O unavailable at Port pins. 1: SMBus0 I/O routed to Port pins.
1	SPI0E	SPI I/O Enable. 0: SPI I/O unavailable at Port pins. 1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO pins.
0	URT0E	UART I/O Output Enable. 0: UART I/O unavailable at Port pin. 1: UART TX0, RX0 routed to Port pins P0.4 and P0.5.

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SFR Definition 27.4. P0MAT: Port 0 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P0MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xFD; SFR Page = All Pages

Bit	Name	Function
7:0	P0MAT[7:0]	Port 0 Match Value. Match comparison value used on Port 0 for bits in P0MASK which are set to '1'. 0: P0.n pin logic value is compared with logic LOW. 1: P0.n pin logic value is compared with logic HIGH.

SFR Definition 27.5. P1MASK: Port 1 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P1MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xEE; SFR Page = All Pages

Bit	Name	Function
7:0	P1MASK[7:0]	Port 1 Mask Value. Selects P1 pins to be compared to the corresponding bits in P1MAT. 0: P1.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P1.n pin logic value is compared to P1MAT.n.

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SFR Definition 27.11. P1: Port 1

Bit	7	6	5	4	3	2	1	0
Name	P1[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0x90; SFR Page = All Pages; Bit Addressable

Bit	Name	Description	Write	Read
7:0	P1[7:0]	Port 1 Data. Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P1.n Port pin is logic LOW. 1: P1.n Port pin is logic HIGH.

SFR Definition 27.12. P1MDIN: Port 1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF2; SFR Page = All Pages

Bit	Name	Function
7:0	P1MDIN[7:0]	Analog Configuration Bits for P1.7–P1.0 (respectively). Port pins configured for analog mode have their weak pul-lup, digital driver, and digital receiver disabled. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.

All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data a byte at a time waiting for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 28.3 illustrates a typical SMBus transaction.

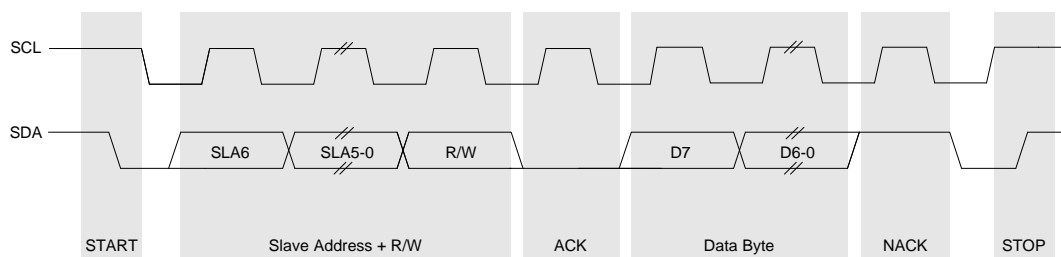


Figure 28.3. SMBus Transaction

28.3.1. Transmitter vs. Receiver

On the SMBus communications interface, a device is the “transmitter” when it is sending an address or data byte to another device on the bus. A device is a “receiver” when an address or data byte is being sent to it from another device on the bus. The transmitter controls the SDA line during the address or data byte. After each byte of address or data information is sent by the transmitter, the receiver sends an ACK or NACK bit during the ACK phase of the transfer, during which time the receiver controls the SDA line.

28.3.2. Arbitration

A master may start a transfer only if the bus is free. The bus is free after a STOP condition or after the SCL and SDA lines remain high for a specified time (see Section “28.3.5. SCL High (SMBus Free) Timeout” on page 195). In the event that two or more devices attempt to begin a transfer at the same time, an arbitration scheme is employed to force one master to give up the bus. The master devices continue transmitting until one attempts a HIGH while the other transmits a LOW. Since the bus is open-drain, the bus will be pulled LOW. The master attempting the HIGH will detect a LOW SDA and lose the arbitration. The winning master continues its transmission without interruption; the losing master becomes a slave and receives the rest of the transfer if addressed. This arbitration scheme is non-destructive: one device always wins, and no data is lost.

28.3.3. Clock Low Extension

SMBus provides a clock synchronization mechanism, similar to I2C, which allows devices with different speed capabilities to coexist on the bus. A clock-low extension is used during a transfer in order to allow slower slave devices to communicate with faster masters. The slave may temporarily hold the SCL line LOW to extend the clock low period, effectively decreasing the serial clock frequency.

28.3.4. SCL Low Timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a “timeout” condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.

For the SMBus0 interface, Timer 3 is used to implement SCL low timeouts. Timer 4 is used on the SMBus1 interface for SCL low timeouts. The SCL low timeout feature is enabled by setting the SMBnTOE bit in SMBnCF. The associated timer is forced to reload when SCL is high, and allowed to count when SCL is

imum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is above 10 MHz.

Table 28.2. Minimum SDA Setup and Hold Times

EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time
0	$T_{low} - 4$ system clocks or 1 system clock + s/w delay*	3 system clocks
1	11 system clocks	12 system clocks
Note: Setup Time for ACK bit transmissions and the MSB of all data transfers. When using software acknowledgement, the s/w delay occurs between the time SMB0DAT or ACK is written and when SI is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.		

With the SMBnTOE bit set, Timer 3 (SMBus0) and Timer 5 (SMBus1) should be configured to overflow after 25 ms in order to detect SCL low timeouts (see Section “28.3.4. SCL Low Timeout” on page 194). The SMBus interface will force the associated timer to reload while SCL is high, and allow the timer to count when SCL is low. The timer interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBnFTE bit. When this bit is set, the bus will be considered free if SDA and SCL remain high for more than 10 SMBus clock source periods (see Figure 28.4).

28.4.2. SMBus Pin Swap

The SMBus peripherals are assigned to pins using the priority crossbar decoder. By default, the SMBus signals are assigned to port pins starting with SDA on the lower-numbered pin, and SCL on the next available pin. The SMBnSWAP bits in the SMBTC register can be set to 1 to reverse the order in which the SMBus signals are assigned.

28.4.3. SMBus Timing Control

The SMBnSDD field in the SMBTC register are used to restrict the detection of a START condition under certain circumstances. In some systems where there is significant mis-match between the impedance or the capacitance on the SDA and SCL lines, it may be possible for SCL to fall after SDA during an address or data transfer. Such an event can cause a false START detection on the bus. These kind of events are not expected in a standard SMBus or I2C-compliant system. **In most systems this parameter should not be adjusted, and it is recommended that it be left at its default value.**

By default, if the SCL falling edge is detected after the falling edge of SDA (i.e. one SYSCLK cycle or more), the device will detect this as a START condition. The SMBnSDD field is used to increase the amount of hold time that is required between SDA and SCL falling before a START is recognized. An additional 2, 4, or 8 SYSCLKs can be added to prevent false START detection in systems where the bus conditions warrant this.

SFR Definition 30.1. SPI0CFG: SPI0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Address = 0xA1; SFR Page = All Pages

Bit	Name	Function
7	SPIBSY	SPI Busy. This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	Master Mode Enable. 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	SPI0 Clock Phase. 0: Data centered on first edge of SCK period.* 1: Data centered on second edge of SCK period.*
4	CKPOL	SPI0 Clock Polarity. 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	Slave Selected Flag. This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	NSS Instantaneous Pin Input. This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	Shift Register Empty (valid in slave mode only). This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. SRMT = 1 when in Master Mode.
0	RXBMT	Receive Buffer Empty (valid in slave mode only). This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. RXBMT = 1 when in Master Mode.
Note: In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 30.1 for timing parameters.		

31.3. Timer 3

Timer 3 is a 16-bit timer formed by two 8-bit SFRs: TMR3L (low byte) and TMR3H (high byte). Timer 3 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T3SPLIT bit (TMR3CN.3) defines the Timer 3 operation mode.

Timer 3 may be clocked by the system clock, the system clock divided by 12, the external oscillator source divided by 8, or the internal low-frequency oscillator divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal high-frequency oscillator drives the system clock while Timer 3 is clocked by an external oscillator source. Note that the external oscillator source divided by 8 and the LFO source divided by 8 are synchronized with the system clock when in all operating modes except suspend. When the internal oscillator is placed in suspend mode, the external clock/8 signal or the LFO/8 output can directly drive the timer. This allows the use of an external clock or the LFO to wake up the device from suspend mode. The timer will continue to run in suspend mode and count up. When the timer overflow occurs, the device will wake from suspend mode, and begin executing code again. The timer value may be set prior to entering suspend, to overflow in the desired amount of time (number of clocks) to wake the device. If a wake-up source other than the timer wakes the device from suspend mode, it may take up to three timer clocks before the timer registers can be read or written. During this time, the STSYNC bit in register OSCICN will be set to 1, to indicate that it is not safe to read or write the timer registers.

Important Note: In internal LFO/8 mode, the divider for the internal LFO must be set to 1 for proper functionality. The timer will not operate if the LFO divider is not set to 1.

31.3.1. 16-bit Timer with Auto-Reload

When T3SPLIT (TMR3CN.3) is zero, Timer 3 operates as a 16-bit timer with auto-reload. Timer 3 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 3 reload registers (TMR3RLH and TMR3RLL) is loaded into the Timer 3 register as shown in Figure 31.7, and the Timer 3 High Byte Overflow Flag (TMR3CN.7) is set. If Timer 3 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 3 overflow. Additionally, if Timer 3 interrupts are enabled and the TF3LEN bit is set (TMR3CN.5), an interrupt will be generated each time the lower 8 bits (TMR3L) overflow from 0xFF to 0x00.

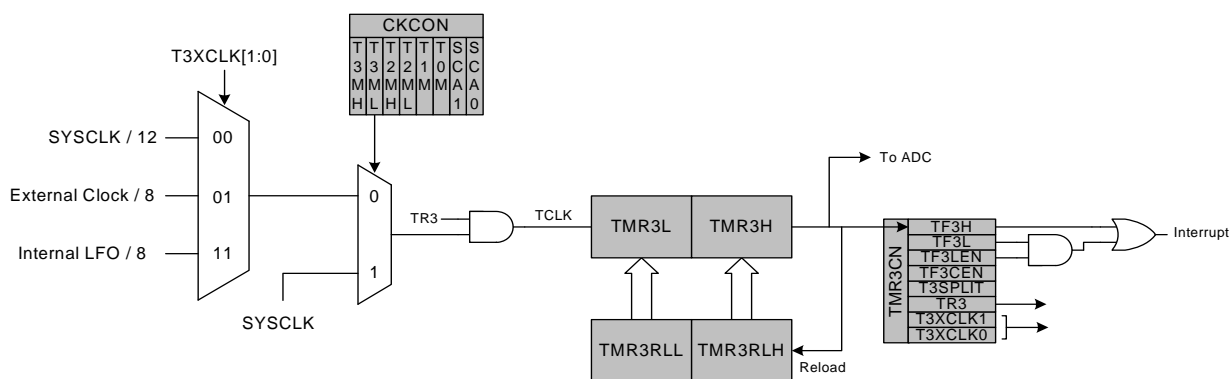


Figure 31.7. Timer 3 16-Bit Mode Block Diagram

31.3.3. Low-Frequency Oscillator (LFO) Capture Mode

The Low-Frequency Oscillator Capture Mode allows the LFO clock to be measured against the system clock or an external oscillator source. Timer 3 can be clocked from the system clock, the system clock divided by 12, or the external oscillator divided by 8, depending on the T3ML (CKCON.6), and T3XCLK[1:0] settings.

Setting TF3CEN to 1 enables the LFO Capture Mode for Timer 3. In this mode, T3SPLIT should be set to 0, as the full 16-bit timer is used. Upon a falling edge of the low-frequency oscillator, the contents of Timer 3 (TMR3H:TMR3L) are loaded into the Timer 3 reload registers (TMR3RLH:TMR3RLL) and the TF3H flag is set. By recording the difference between two successive timer capture values, the LFO clock frequency can be determined with respect to the Timer 3 clock. The Timer 3 clock should be much faster than the LFO to achieve an accurate reading. This means that the LFO/8 should not be selected as the timer clock source in this mode.

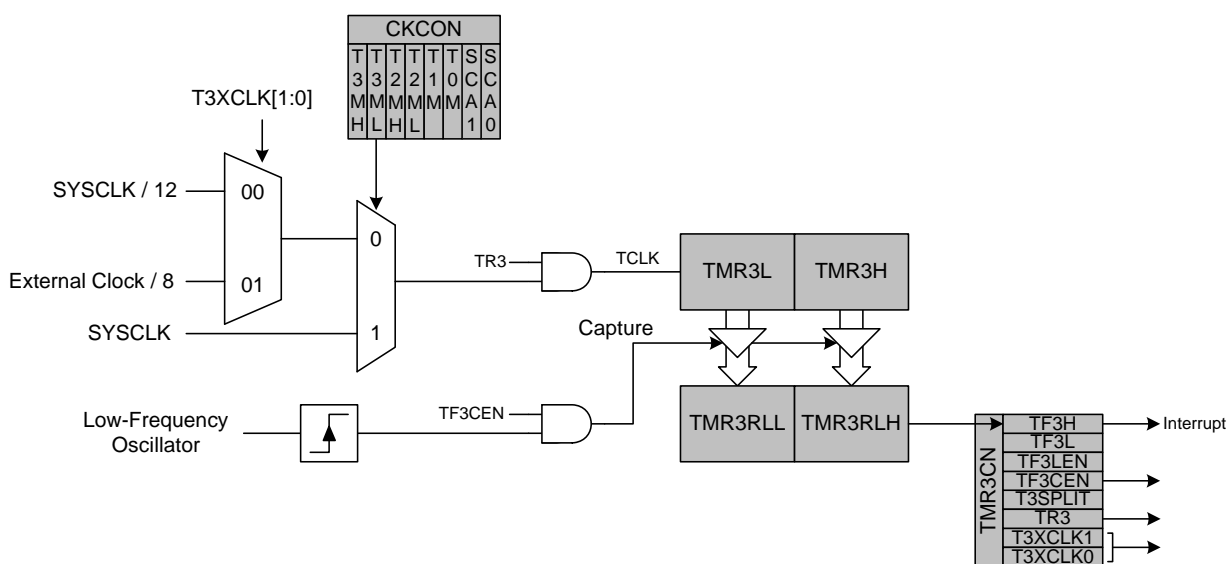


Figure 31.9. Timer 3 Low-Frequency Oscillation Capture Mode Block Diagram

C8051F39x/37x

SFR Definition 31.20. TMR4RLL: Timer 4 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR4RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x92; SFR Page = F

Bit	Name	Function
7:0	TMR4RLL[7:0]	Timer 4 Reload Register Low Byte. TMR4RLL holds the low byte of the reload value for Timer 4.

SFR Definition 31.21. TMR4RLH: Timer 4 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR4RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x93; SFR Page = F

Bit	Name	Function
7:0	TMR4RLH[7:0]	Timer 4 Reload Register High Byte. TMR4RLH holds the high byte of the reload value for Timer 4.

SFR Definition 31.22. TMR4L: Timer 4 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR4L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x94; SFR Page = F

Bit	Name	Function
7:0	TMR4L[7:0]	Timer 4 Low Byte. In 16-bit mode, the TMR4L register contains the low byte of the 16-bit Timer 4. In 8-bit mode, TMR4L contains the 8-bit low byte timer value.

31.5. Timer 5

Timer 5 is a 16-bit timer formed by two 8-bit SFRs: TMR5L (low byte) and TMR5H (high byte). Timer 5 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T5SPLIT bit (TMR5CN.3) defines

Timer 5 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. Note that the external oscillator source divided by 8 is synchronized with the system clock.

31.5.1. 16-bit Timer with Auto-Reload

When T5SPLIT (TMR5CN.3) is zero, Timer 5 operates as a 16-bit timer with auto-reload. Timer 5 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 5 reload registers (TMR5RLH and TMR5RLL) is loaded into the Timer 5 register as shown in Figure 31.12, and the Timer 5 High Byte Overflow Flag (TMR5CN.7) is set. If Timer 5 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 5 overflow. Additionally, if Timer 5 interrupts are enabled and the TF5LEN bit is set (TMR5CN.5), an interrupt will be generated each time the lower 8 bits (TMR5L) overflow from 0xFF to 0x00.

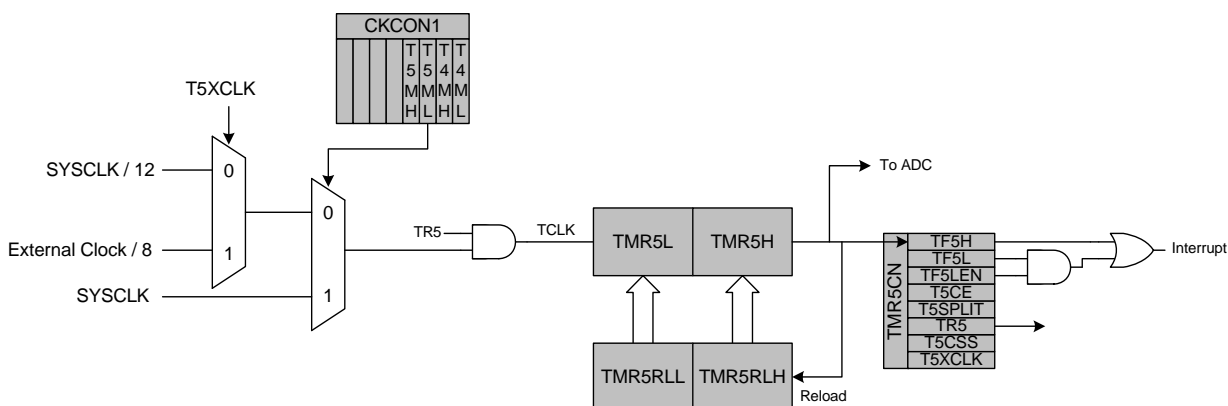


Figure 31.12. Timer 5 16-Bit Mode Block Diagram

31.5.2. 8-bit Timers with Auto-Reload

When T5SPLIT is 1 and T5CE = 0, Timer 5 operates as two 8-bit timers (TMR5H and TMR5L). Both 8-bit timers operate in auto-reload mode as shown in Figure 31.13. TMR5RLL holds the reload value for TMR5L; TMR5RLH holds the reload value for TMR5H. The TR5 bit in TMR5CN handles the run control for TMR5H. TMR5L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCCLK, SYSCCLK divided by 12, or the external oscillator clock source divided by 8. The Timer 5 Clock Select bits (T5MH and T5ML in CKCON1) select either SYSCCLK or the clock defined by the Timer 5 External Clock Select bit (T5XCLK in TMR5CN), as follows:

T5MH	T5XCLK	TMR5H Clock Source
0	0	SYSCCLK/12
0	1	External Clock/8
1	X	SYSCCLK

T5ML	T5XCLK	TMR5L Clock Source
0	0	SYSCCLK/12
0	1	External Clock/8
1	X	SYSCCLK

The TF5H bit is set when TMR5H overflows from 0xFF to 0x00; the TF5L bit is set when TMR5L overflows from 0xFF to 0x00. When Timer 5 interrupts are enabled, an interrupt is generated each time TMR5H overflows. If Timer 5 interrupts are enabled and TF5LEN (TMR5CN.5) is set, an interrupt is generated each time either TMR5L or TMR5H overflows. When TF5LEN is enabled, software must check the TF5H and TF5L flags to determine the source of the Timer 5 interrupt. The TF5H and TF5L interrupt flags are not cleared by hardware and must be manually cleared by software.

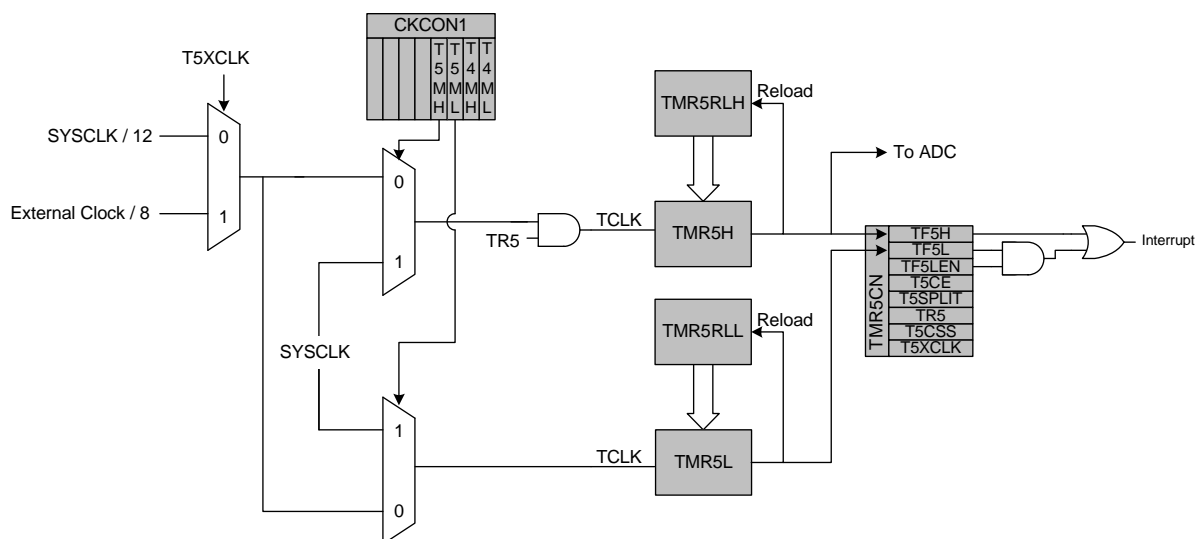


Figure 31.13. Timer 5 8-Bit Mode Block Diagram

SFR Definition 32.6. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF9; SFR Page = All Pages

Bit	Name	Function
7:0	PCA0[7:0]	PCA Counter/Timer Low Byte. The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.
Note: When the WDTE bit is set to 1, the PCA0L register cannot be modified by software. To change the contents of the PCA0L register, the Watchdog Timer must first be disabled.		

SFR Definition 32.7. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFA; SFR Page = All Pages

Bit	Name	Function
7:0	PCA0[15:8]	PCA Counter/Timer High Byte. The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a “snapshot” register, whose contents are updated only when the contents of PCA0L are read (see Section 32.1).
Note: When the WDTE bit is set to 1, the PCA0H register cannot be modified by software. To change the contents of the PCA0H register, the Watchdog Timer must first be disabled.		

33. C2 Interface

C8051F39x/37x devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

33.1. C2 Interface Registers

The following describes the C2 registers necessary to perform Flash programming through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 33.1. C2ADD: C2 Address

Bit	7	6	5	4	3	2	1	0
Name	C2ADD[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function	
7:0	C2ADD[7:0]	C2 Address. The C2ADD register is accessed via the C2 interface to select the target Data register for C2 Data Read and Data Write commands.	
		Address	Description
		0x00	Selects the Device ID register for Data Read instructions
		0x01	Selects the Revision ID register for Data Read instructions
		0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions
		0xB4	Selects the C2 Flash Programming Data register for Data Read/Write instructions