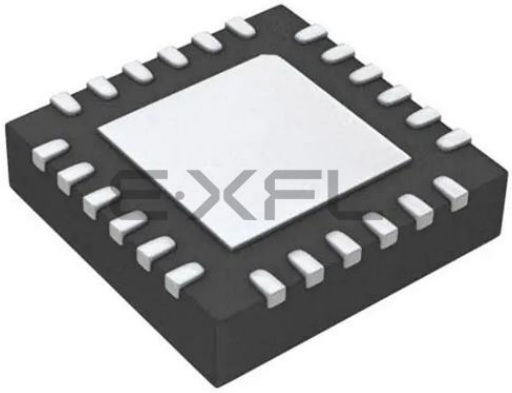

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	21
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f394-a-gm

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4. Pin Definitions

Table 4.1. Pin Definitions for the C8051F39x/37x

Name	Pin 'F392/3/6/7/8/9	Pin 'F390/1/4/5	Pin 'F370/1/4/5	Type	Description
V_{DD}	3	4	4		Power Supply Voltage.
GND	2	3	3		Ground. This ground connection is required. The center pad may optionally be connected to ground also.
$\overline{RST}$/ C2CK	4	5	5	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 10 µs. Clock signal for the C2 Debug Interface.
C2D	5	6	6	D I/O	Bi-directional data signal for the C2 Debug Interface. Shared with P2.0 on 20-pin packaging and P2.4 on 24-pin packaging.
P0.0/ VREF	1	2	2	D I/O or A In A In	Port 0.0. External VREF input.
P0.1 IDA0	20	1	1	D I/O or A In A Out	Port 0.1. IDA0 Output.
P0.2/ XTAL1	19	24	24	D I/O or A In A In	Port 0.2. External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/ XTAL2	18	23	23	D I/O or A In A I/O or D In	Port 0.3. External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	17	22	22	D I/O or A In	Port 0.4.
P0.5	16	21	21	D I/O or A In	Port 0.5.

Table 4.1. Pin Definitions for the C8051F39x/37x (Continued)

Name	Pin ‘F392/3/6/7/8/9	Pin ’F390/1/4/5	Pin ’F370/1/4/5	Type	Description
P0.6/ CNVSTR	15	20	20	D I/O or A In D In	Port 0.6. ADC0 External Convert Start or IDA0 Update Source Input.
P0.7	14	19	19	D I/O or A In	Port 0.7.
P1.0 IDA1	13	—	—	D I/O or A In A Out	Port 1.0. IDA1 Output.
P1.0		18	18	D I/O or A In	Port 1.0.
P1.1	12	17	17	D I/O or A In	Port 1.1.
P1.2 IDA1	-	16	16	D I/O or A In A Out	Port 1.2. IDA1 Output.
P1.2	11	—	—	D I/O or A In	Port 1.2.
P1.3	10	15	15	D I/O or A In	Port 1.3.
P1.4	9	14	14	D I/O or A In	Port 1.4.
P1.5	8	13	13	D I/O or A In	Port 1.5.
P1.6	7	12	12	D I/O or A In	Port 1.6.
P1.7	6	11	11	D I/O or A In	Port 1.7.
P2.0	5	10	10	D I/O or A In	Port 2.0. (Also C2D on 20-pin Packaging)
P2.1	—	9	9	D I/O or A In	Port 2.1.

Table 7.13. Voltage Reference Electrical Characteristics

V_{DD} = 3.0 V, –40 to +105 °C (C8051F39x), –40 to +85 °C (C8051F37x), unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Internal Reference (REFBE = 1)					
Output Voltage	2.4 V Setting	2.37	2.4	2.43	V
	1.2 V Setting	1.18	1.2	1.22	V
VREF Short-Circuit Current		—	—	8	mA
VREF Temperature Coefficient		—	33	—	ppm/°C
Load Regulation	Load = 0 to 200 µA to AGND	—	6	—	µV/µA
VREF Turn-on Time 1	4.7 µF tantalum, 0.1 µF ceramic bypass	—	1.5	—	ms
VREF Turn-on Time 2	0.1 µF ceramic bypass	—	110	—	µs
Power Supply Rejection	2.4 V Setting	—	3.5	—	mV/V
	1.2 V Setting	—	1.1	—	mV/V
External Reference (REFBE = 0)					
Input Voltage Range		1.0	—	V_{DD}	V
Input Current	Sample Rate = 200 ksps; VREF = 3.0 V	—	3	—	µA
Power Specifications					
Supply Current	REFBE = “1” or TEMPE = “1”	—	70	100	µA

Table 7.14. Voltage Regulator Electrical Characteristics

V_{DD} = 3.0 V, –40 to +105 °C (C8051F39x), –40 to +85 °C (C8051F37x), unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Output Voltage		1.73	1.78	1.83	V
Power Supply Sensitivity	Constant Temperature	—	0.5	—	%/V
Temperature Sensitivity	Constant Supply	—	55	—	ppm/°C

SFR Definition 14.2. CPT0MD: Comparator0 Mode Selection

Bit	7	6	5	4	3	2	1	0
Name			CP0RIE	CP0FIE			CP0MD[1:0]	
Type	R	R	R/W	R/W	R	R	R/W	
Reset	0	0	0	0	0	0	1	0

SFR Address = 0x9D; SFR Page = All Pages

Bit	Name	Function
7:6	Unused	Unused. Read = 00b, Write = Don't Care.
5	CP0RIE	**Comparator0 Rising-Edge Interrupt Enable.** 0: Comparator0 Rising-edge interrupt disabled. 1: Comparator0 Rising-edge interrupt enabled.
4	CP0FIE	**Comparator0 Falling-Edge Interrupt Enable.** 0: Comparator0 Falling-edge interrupt disabled. 1: Comparator0 Falling-edge interrupt enabled.
3:2	Unused	Unused. Read = 00b, Write = don't care.
1:0	CP0MD[1:0]	**Comparator0 Mode Select.** These bits affect the response time and power consumption for Comparator0. 00: Mode 0 (Fastest Response Time, Highest Power Consumption) 01: Mode 1 10: Mode 2 11: Mode 3 (Slowest Response Time, Lowest Power Consumption)

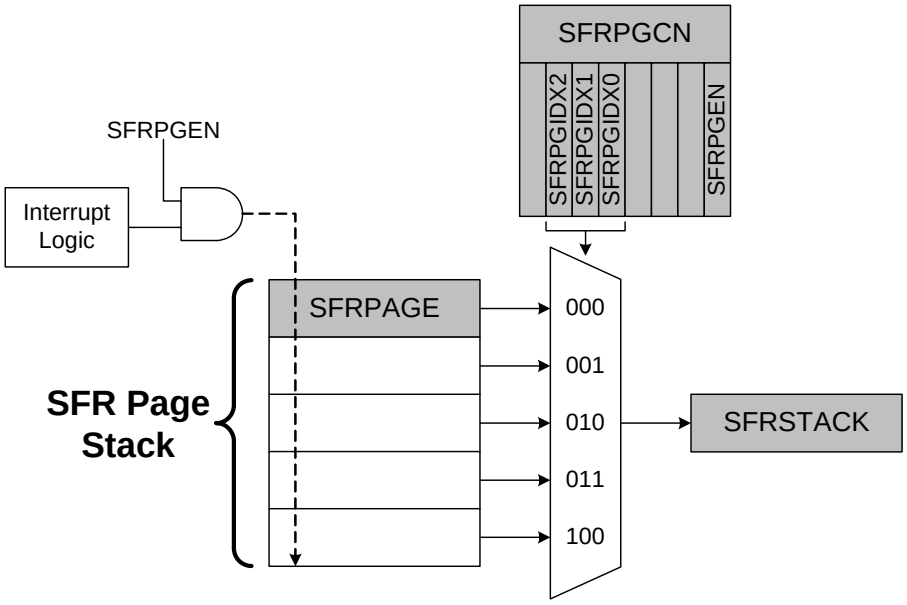

Figure 19.1. SFR Page Stack

Upon an interrupt, hardware performs the five following operations:

1. The value (if any) in the SFRPGIDX = 011b location is pushed to the SFRPAGE = 100b location.
2. The value (if any) in the SFRPGIDX = 010b location is pushed to the SFRPAGE = 011b location.
3. The value (if any) in the SFRPGIDX = 001b location is pushed to the SFRPAGE = 010b location.
4. The current SFRPAGE value is pushed to the SFRPGIDX = 001b location in the stack.
5. SFRPAGE is set to the page corresponding to the flag which generated the interrupt.

On a return from interrupt, hardware performs the four following operations:

1. The SFR page stack is popped resulting in the value in the SFRPGIDX = 001b location returning to the SFRPAGE register, thereby restoring the SFR page context without software intervention.
2. The value in the SFRPGIDX = 010b location of the stack is placed in the SFRPGIDX = 001b location.
3. The value in the SFRPGIDX = 011b location of the stack is placed in the SFRPGIDX = 010b location.
4. The value in the SFRPGIDX = 100b location of the stack is placed in the SFRPGIDX = 011b location.

Automatic switching of the SFR page by hardware upon interrupt entries and exits may be enabled or disabled using the SFR Automatic Page Control Enable Bit (SFRPGEN) located in SFRPGCN. The automatic SFR page switching is enabled after a reset until disabled by firmware.

Table 19.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	SFR Page	Description	Page
ACC	0xE0	All Pages	Accumulator	89
ADC0CF	0xBC	All Pages	ADC0 Configuration	55
ADC0CN	0xE8	All Pages	ADC0 Control	57
ADC0GTH	0xC4	All Pages	ADC0 Greater-Than Compare High	58
ADC0GTL	0xC3	All Pages	ADC0 Greater-Than Compare Low	58
ADC0H	0xBE	All Pages	ADC0 High	56
ADC0L	0xBD	All Pages	ADC0 Low	56
ADC0LTH	0xC6	All Pages	ADC0 Less-Than Compare Word High	59
ADC0LTL	0xC5	All Pages	ADC0 Less-Than Compare Word Low	59
AMX0N	0xBA	All Pages	AMUX0 Negative Channel Select	63
AMX0P	0xBB	All Pages	AMUX0 Positive Channel Select	62
B	0xF0	All Pages	B Register	90
CKCON	0x8E	All Pages	Clock Control	243
CKCON1	0xF4	All Pages	Clock Control 1	244
CLKSEL	0xA9	All Pages	Clock Select	165
CPT0CN	0x9B	All Pages	Comparator0 Control	78
CPT0MD	0x9D	All Pages	Comparator0 Mode Selection	79
CPT0MX	0x9F	All Pages	Comparator0 MUX Selection	81
CRC0AUTO	0xDD	All Pages	CRC0 Automatic Control	152
CRC0CN	0xDF	All Pages	CRC0 Control	150
CRC0CNT	0xDE	All Pages	CRC0 Automatic Flash Sector Count	153
CRC0DAT	0x9E	All Pages	CRC0 Data Output	151
CRC0FLIP	0x9A	All Pages	CRC0 Bit Flip	154
CRC0IN	0x9C	All Pages	CRC0 Data Input	151
DERIVID	0xAB	0	Device Derivative ID	97
DPH	0x83	All Pages	Data Pointer High	88
DPL	0x82	All Pages	Data Pointer Low	88
EIE1	0xE6	All Pages	Extended Interrupt Enable 1	123
EIE2	0xAF	All Pages	Extended Interrupt Enable 2	126
EIP1	0xF6	All Pages	Extended Interrupt Priority 1	124
EIP1H	0x85	All Pages	Extended Interrupt Priority 1 High	125
EIP2	0xBF	All Pages	Extended Interrupt Priority 2	127
EIP2H	0x86	All Pages	Extended Interrupt Priority 2 High	127

22.3. Read Operation

There are two operations to read the EEPROM: current address read and selective address read. Both read operations can read up to 256 bytes within a single read operation.

22.3.1. Current Address Read

A current address read accesses the data at the EEPROM internal address counter's current location.

The address counter in the EEPROM maintains the address of the last byte accessed, incremented by one. For example, if the previous operation was a read or write operation addressed to address location n, the internal address counter automatically increments to address n+1.

To perform a current address read operation:

1. The master sends the START condition and the slave address byte with the R/W bit set to 1.
2. The EEPROM generates an ACK and transmits the byte of data (D[7:0]) stored at the address specified by the address counter. This address will be the address from the last read or write operation incremented by one.
3. The EEPROM increments the internal address counter by one.
4. (Optional) To read additional bytes:
    a. The master generates an ACK.
    b. The EEPROM transmits the byte of data stored at the address specified by the address counter.
    c. The EEPROM increments the internal address counter by one.
    d. Repeat Step 4a through 4c until the master is done reading bytes.
5. The master generates a NACK.
6. The master generates a STOP condition.
7. The EEPROM terminates the transmission.

Note: If the previous operation targeted the last byte of the EEPROM, the EEPROM will transmit the data from address location 0x00 for a current address read operation.

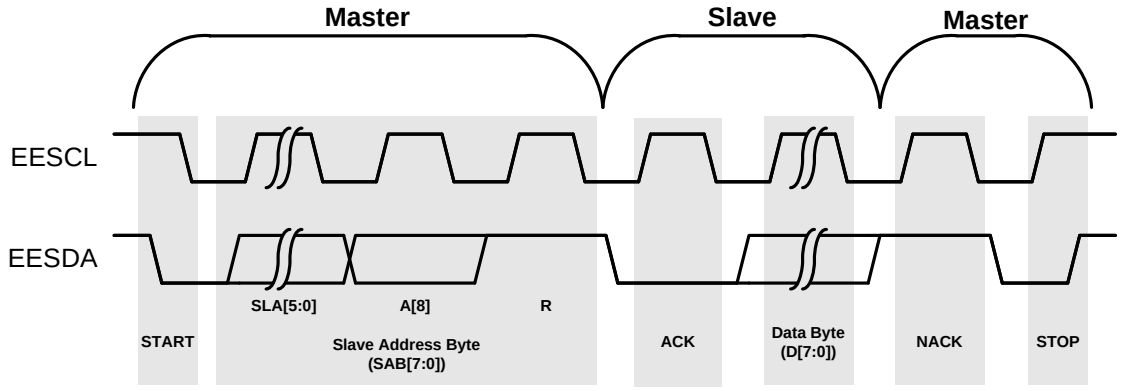

Figure 22.4. Current Address Read Operation (Single Byte)

SFR Definition 25.1. PCON: Power Control

Bit	7	6	5	4	3	2	1	0
Name	GF[5:0]						STOP	IDLE
Type	R/W						R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x87; SFR Page = All Pages

Bit	Name	Function
7:2	GF[5:0]	**General Purpose Flags 5–0.** These are general purpose flags for use under software control.
1	STOP	**Stop Mode Select.** Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0. 1: CPU goes into Stop mode (internal oscillator stopped).
0	IDLE	**IDLE: Idle Mode Select.** Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0. 1: CPU goes into Idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)

SFR Definition 26.5. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	XCLKVLD	XOSCMD[2:0]				XFCN[2:0]		
Type	R	R/W			R	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB1; SFR Page = All Pages

Bit	Name	Function
7	XCLKVLD	**External Oscillator Valid Flag.** Provides External Oscillator status and is valid at all times for all modes of operation except External CMOS Clock Mode and External CMOS Clock Mode with divide by 2. In these modes, XCLKVLD always returns 0. 0: External Oscillator is unused or not yet stable. 1: External Oscillator is running and stable.
6:4	XOSCMD[2:0]	**External Oscillator Mode Select.** 00x: External Oscillator circuit off. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide-by-2 stage. 100: RC Oscillator Mode with divide-by-2 stage. 101: Capacitor Oscillator Mode with divide-by-2 stage. 110: Crystal Oscillator Mode. 111: Crystal Oscillator Mode with divide-by-2 stage.
3	Unused	Read = 0; Write = don't care
2:0	XFCN[2:0]	**External Oscillator Frequency Control Bits.** Set according to the desired frequency for RC mode. Set according to the desired K Factor for C mode.

XFCN	Crystal Mode	RC Mode	C Mode
000	f ≤ 20 kHz	f ≤ 25 kHz	K Factor = 0.87
001	20 kHz < f ≤ 58 kHz	25 kHz < f ≤ 50 kHz	K Factor = 2.6
010	58 kHz < f ≤ 155 kHz	50 kHz < f ≤ 100 kHz	K Factor = 7.8
011	155 kHz < f ≤ 415 kHz	100 kHz < f ≤ 200 kHz	K Factor = 22
100	415 kHz < f ≤ 1.1 MHz	200 kHz < f ≤ 400 kHz	K Factor = 66
101	1.1 MHz < f ≤ 3.1 MHz	400 kHz < f ≤ 800 kHz	K Factor = 189
110	3.1 MHz < f ≤ 8.2 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 741
111	8.2 MHz < f ≤ 25 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 2222

27.5. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMATCH registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMATCH registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (P0MATCH & P0MASK) or if (P1 & P1MASK) does not equal (P1MATCH & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode, such as IDLE or SUSPEND. See the Interrupts and Power Options chapters for more details on interrupt and wake-up sources.

SFR Definition 27.3. P0MASK: Port 0 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P0MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFE; SFR Page = All Pages

Bit	Name	Function
7:0	P0MASK[7:0]	**Port 0 Mask Value.** Selects P0 pins to be compared to the corresponding bits in P0MAT. 0: P0.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P0.n pin logic value is compared to P0MAT.n.

SFR Definition 27.17. P2MDOUT: Port 2 Output Mode

Bit	7	6	5	4	3	2	1	0
Name				P2MDOUT[4:0]				
Type	R	R	R	R/W				
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA6; SFR Page = All Pages

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care
4:0	P2MDOUT[4:0]	**Output Configuration Bits for P2.4–P2.0 (respectively).** These bits are ignored if the corresponding bit in register P2MDIN is logic 0. 0: Corresponding P2.n Output is open-drain. 1: Corresponding P2.n Output is push-pull.
Note: P2.0 is not available for analog input in the QFN20-packaged devices, and P2.1-P2.4 are only available in the QFN24-packaged devices.		

SFR Definition 27.18. P2SKIP: Port 2 Skip

Bit	7	6	5	4	3	2	1	0
Name					P2SKIP[7:0]			
Type	R	R	R	R	R/W			
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD6; SFR Page = All Pages

Bit	Name	Function
7:4	Unused	Read = 0000b; Write = Don't Care
3:0	P2SKIP[3:0]	**Port 2 Crossbar Skip Enable Bits.** These bits select Port 2 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P2.n pin is not skipped by the Crossbar. 1: Corresponding P2.n pin is skipped by the Crossbar.
Note: P2.0 is not available for crossbar peripherals in the QFN20-packaged devices, and P2.1-P2.4 are only available in the QFN24-packaged devices.		

low. With the associated timer enabled and configured to overflow after 25 ms (and SMBnTOE set), the timer interrupt service routine can be used to reset (disable and re-enable) the SMBus in the event of an SCL low timeout.

28.3.5. SCL High (SMBus Free) Timeout

The SMBus specification stipulates that if the SCL and SDA lines remain high for more that 50 µs, the bus is designated as free. When the SMBnFTE bit in SMBnCF is set, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods (as defined by the timer configured for the SMBus clock source). If the SMBus is waiting to generate a Master START, the START will be generated following this timeout. A clock source is required for free timeout detection, even in a slave-only implementation.

28.4. Using the SMBus

The SMBus can operate in both Master and Slave modes. The interface provides timing and shifting control for serial transfers; higher level protocol is determined by user software. The SMBus interface provides the following application-independent features:

- Byte-wise serial data transfers
- Clock signal generation on SCL (Master Mode only) and SDA data synchronization
- Timeout/bus error recognition, as defined by the SMB0CF configuration register
- START/STOP timing, detection, and generation
- Bus arbitration
- Interrupt generation
- Status information
- Optional hardware recognition of slave address and automatic acknowledgement of address/data

SMBus interrupts are generated for each data byte or slave address that is transferred. When hardware acknowledgment is disabled, the point at which the interrupt is generated depends on whether the hardware is acting as a data transmitter or receiver. When a transmitter (i.e., sending address/data, receiving an ACK), this interrupt is generated after the ACK cycle so that software may read the received ACK value; when receiving data (i.e., receiving address/data, sending an ACK), this interrupt is generated before the ACK cycle so that software may define the outgoing ACK value. If hardware acknowledgment is enabled, these interrupts are always generated after the ACK cycle. See Section 28.5 for more details on transmission sequences.

Interrupts are also generated to indicate the beginning of a transfer when a master (START generated), or the end of a transfer when a slave (STOP detected). Software should read the SMBnCN (SMBus Control register) to find the cause of the SMBus interrupt. The SMBnCN register is described in Section 28.4.4; Table 28.5 provides a quick SMBnCN decoding reference.

28.4.1. SMBus Configuration Register

The SMBus Configuration register (SMBnCF) is used to enable the SMBus Master and/or Slave modes, select the SMBus clock source, and select the SMBus timing and timeout options. When the ENSMB bit is set, the SMBus is enabled for all master and slave events. Slave events may be disabled by setting the INH bit. With slave events inhibited, the SMBus interface will still monitor the SCL and SDA pins; however, the interface will NACK all received addresses and will not generate any slave interrupts. When the INH bit is set, all slave events will be inhibited following the next START (interrupts will continue for the duration of the current transfer).

Table 29.1. Timer Settings for Standard Baud Rates Using The Internal 49 MHz Oscillator

	Frequency: 49 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)[1]	T1M[1]	Timer 1 Reload Value (hex)
SYSCLK from Internal Osc.	230400	–0.32%	212	SYSCLK	XX[2]	1	0x96
	115200	0.15%	426	SYSCLK	XX	1	0x2B
	57600	–0.32%	848	SYSCLK/4	01	0	0x96
	28800	0.15%	1704	SYSCLK/12	00	0	0xB9
	9600	–0.32%	5088	SYSCLK/48	00	0	0xCB
	2400	0.15%	20448	SYSCLK/48	10	0	0x2B

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 31.1.
2. X = Don't care.

Table 29.2. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator

	Frequency: 22.1184 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)[1]	T1M[1]	Timer 1 Reload Value (hex)
SYSCLK from External Osc.	230400	0.00%	96	SYSCLK	XX[2]	1	0xD0
	115200	0.00%	192	SYSCLK	XX	1	0xA0
	57600	0.00%	384	SYSCLK	XX	1	0x40
	28800	0.00%	768	SYSCLK / 12	00	0	0xE0
	14400	0.00%	1536	SYSCLK / 12	00	0	0xC0
	9600	0.00%	2304	SYSCLK / 12	00	0	0xA0
	2400	0.00%	9216	SYSCLK / 48	10	0	0xA0
	1200	0.00%	18432	SYSCLK / 48	10	0	0x40
SYSCLK from Internal Osc.	230400	0.00%	96	EXTCLK / 8	11	0	0xFA
	115200	0.00%	192	EXTCLK / 8	11	0	0xF4
	57600	0.00%	384	EXTCLK / 8	11	0	0xE8
	28800	0.00%	768	EXTCLK / 8	11	0	0xD0
	14400	0.00%	1536	EXTCLK / 8	11	0	0xA0
	9600	0.00%	2304	EXTCLK / 8	11	0	0x70

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 31.1.
2. X = Don't care.

SFR Definition 30.3. SPI0CKR: SPI0 Clock Rate

Bit	7	6	5	4	3	2	1	0
Name	SCR[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA2; SFR Page = All Pages

Bit	Name	Function
7:0	SCR[7:0]	**SPI0 Clock Rate.** These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register. $f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR[7:0] + 1)}$ for 0 <= SPI0CKR <= 255 Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04, $f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$ $f_{SCK} = 200kHz$

SFR Definition 31.2. CKCON1: Clock Control 1

Bit	7	6	5	4	3	2	1	0
Name					T5MH	T5ML	T4MH	T4ML
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF4; SFR Page = All Pages

Bit	Name	Function
7:4	Unused	Read = 0000b; Write = don't care
3	T5MH	**Timer 5 High Byte Clock Select.** Selects the clock supplied to the Timer 5 high byte (split 8-bit timer mode only). 0: Timer 5 high byte uses the clock defined by the T5XCLK bit in TMR5CN. 1: Timer 5 high byte uses the system clock.
2	T5ML	**Timer 5 Low Byte Clock Select.** Selects the clock supplied to Timer 5. Selects the clock supplied to the lower 8-bit timer in split 8-bit timer mode. 0: Timer 5 low byte uses the clock defined by the T5XCLK bit in TMR5CN. 1: Timer 5 low byte uses the system clock.
1	T4MH	**Timer 4 High Byte Clock Select.** Selects the clock supplied to the Timer 4 high byte (split 8-bit timer mode only). 0: Timer 4 high byte uses the clock defined by the T4XCLK bit in TMR4CN. 1: Timer 4 high byte uses the system clock.
0	T4ML	**Timer 4 Low Byte Clock Select.** Selects the clock supplied to Timer 4. If Timer 4 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer. 0: Timer 4 low byte uses the clock defined by the T4XCLK bit in TMR4CN. 1: Timer 4 low byte uses the system clock.

SFR Definition 31.5. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8A; SFR Page = All Pages

Bit	Name	Function
7:0	TL0[7:0]	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 31.6. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8B; SFR Page = All Pages

Bit	Name	Function
7:0	TL1[7:0]	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

31.4. Timer 4

Timer 4 is a 16-bit timer formed by two 8-bit SFRs: TMR4L (low byte) and TMR4H (high byte). Timer 4 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T4SPLIT bit (TMR4CN.3) defines

Timer 4 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. Note that the external oscillator source divided by 8 is synchronized with the system clock.

31.4.1. 16-bit Timer with Auto-Reload

When T4SPLIT (TMR4CN.3) is zero, Timer 4 operates as a 16-bit timer with auto-reload. Timer 4 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 4 reload registers (TMR4RLH and TMR4RLL) is loaded into the Timer 4 register as shown in Figure 31.10, and the Timer 4 High Byte Overflow Flag (TMR4CN.7) is set. If Timer 4 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 4 overflow. Additionally, if Timer 4 interrupts are enabled and the TF4LEN bit is set (TMR4CN.5), an interrupt will be generated each time the lower 8 bits (TMR4L) overflow from 0xFF to 0x00.

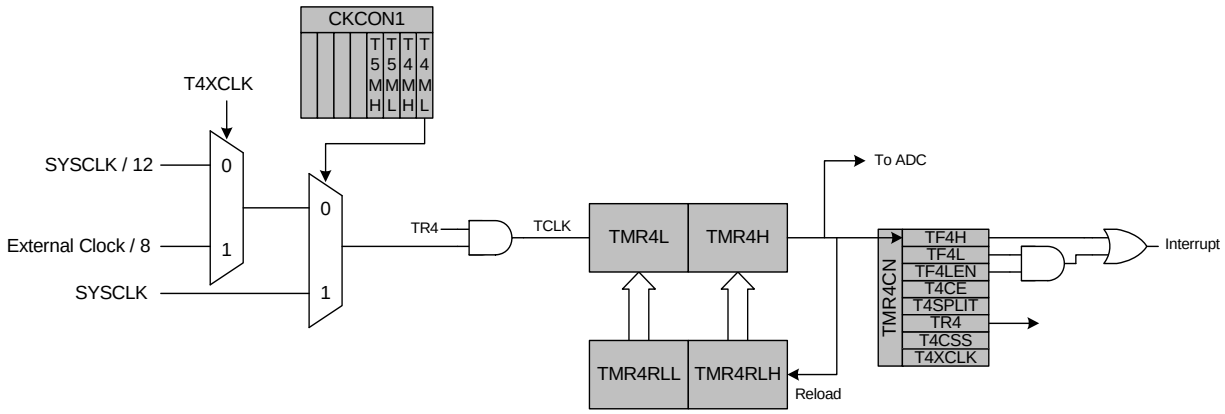

Figure 31.10. Timer 4 16-Bit Mode Block Diagram

SFR Definition 31.23. TMR4H Timer 4 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR4H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x95; SFR Page = F

Bit	Name	Function
7:0	TMR4H[7:0]	**Timer 4 High Byte.** In 16-bit mode, the TMR4H register contains the high byte of the 16-bit Timer 4. In 8-bit mode, TMR4H contains the 8-bit high byte timer value.