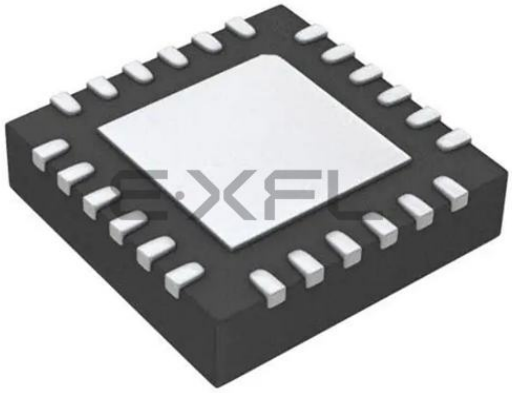

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	21
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f394-a-gmr

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Table 7.10. ADC0 Electrical Characteristics

V_{DD} = 3.0 V, VREF = 2.40 V (REFSL = 0), –40 to +105 °C (C8051F39x), –40 to +85 °C (C8051F37x), unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
DC Accuracy					
Resolution	C8051F394/5/6/7, C8051F374/5		10		bits
Integral Nonlinearity	C8051F398/9	—	<±0.5	±2.0	LSB
Differential Nonlinearity		—	<±0.5	±1	LSB
Offset Error		–2	0	2	LSB
Full Scale Error		–5	–2	1	LSB
Offset Temperature Coefficient		—	0.005	—	LSB/°C
Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, 500 ksps)					
Signal-to-Noise Plus Distortion		55	58	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	–73	—	dB
Spurious-Free Dynamic Range		—	68	—	dB
Conversion Rate					
SAR Conversion Clock		—	—	8.33	MHz
Conversion Time in SAR Clocks		13	—	—	clocks
Track/Hold Acquisition Time		300	—	—	ns
Throughput Rate		—	—	500	ksps
Analog Inputs					
ADC Input Voltage Range	Single Ended (AIN+ – GND) Differential (AIN+ – AIN–)	0 –VREF	— —	VREF VREF	V V
Absolute Pin Voltage with respect to GND	Single Ended or Differential	0	—	V_{DD}	V
Sampling Capacitance (C_{SAMPLE})		—	5	—	pF
Input Multiplexer Impedance (R_{MUX})		—	1.6	—	kΩ
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC0)	Operating Mode, 500 ksps	—	860	1010	µA
Power Supply Rejection	Single Ended (AIN+ – GND) Differential (AIN+ – AIN–)	— —	1.15 2.45	— —	mV/V mV/V

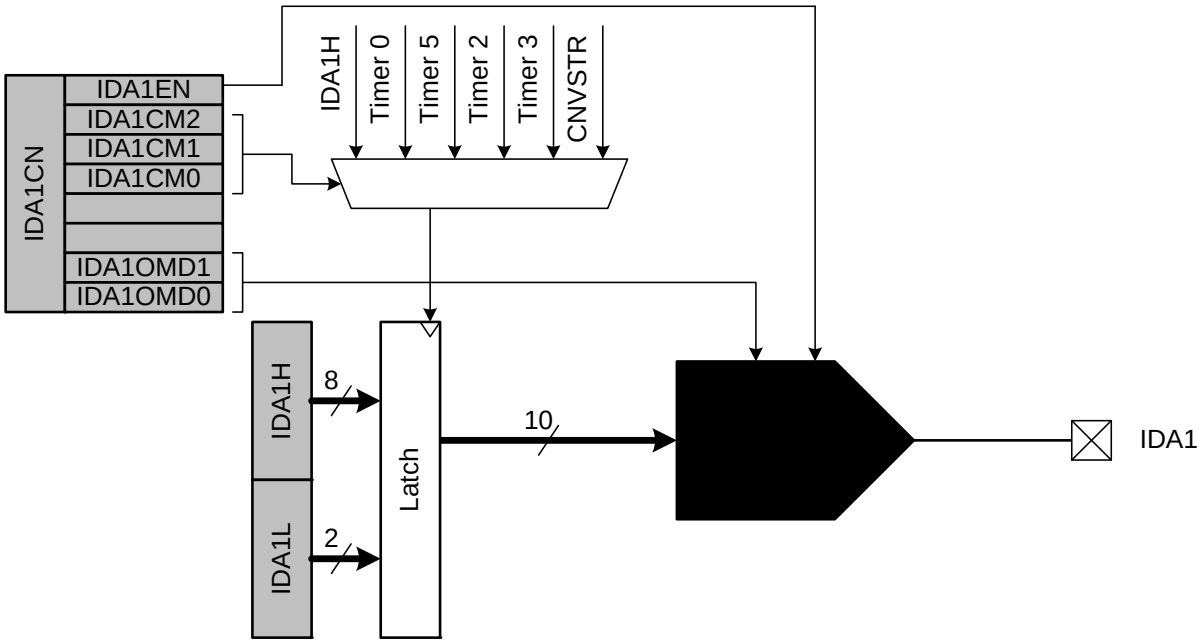

Figure 11.2. IDA1 Functional Block Diagram

SFR Definition 11.5. IDA1H: IDA1 Data Word MSB

Bit	7	6	5	4	3	2	1	0
Name	IDA1[9:2]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x97; SFR Page = F

Bit	Name	Function
7:0	IDA1[9:2]	**IDA1 Data Word High-Order Bits.** Upper 8 bits of the 10-bit IDA1 Data Word.

SFR Definition 11.6. IDA1L: IDA1 Data Word LSB

Bit	7	6	5	4	3	2	1	0
Name	IDA1[1:0]							
Type	R/W		R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x96; SFR Page = F

Bit	Name	Function
7:6	IDA1[1:0]	**IDA1 Data Word Low-Order Bits.** Lower 2 bits of the 10-bit IDA1 Data Word.
5:0	Unused	Unused. Read = 000000b. Write = Don’t care.

SFR Definition 15.3. SP: Stack Pointer

Bit	7	6	5	4	3	2	1	0
Name	SP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	1	1	1

SFR Address = 0x81; SFR Page = All Pages

Bit	Name	Function
7:0	SP[7:0]	**Stack Pointer.** The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 15.4. ACC: Accumulator

Bit	7	6	5	4	3	2	1	0
Name	ACC[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7:0	ACC[7:0]	**Accumulator.** This register is the accumulator for arithmetic operations.

SFR Definition 17.1. EMI0CN: External Memory Interface Control

Bit	7	6	5	4	3	2	1	0
Name							PGSEL	
Type	R	R	R	R	R	R	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAA; SFR Page = All Pages

Bit	Name	Function
7:2	Unused	Read = 000000b; Write = Don't Care
1:0	PGSEL	**XRAM Page Select.** The PGSEL field provides the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM. Since the upper (unused) bits of the register are always zero, the PGSEL determines which page of XRAM is accessed. For Example: If PGSEL = 0x01, addresses 0x0100 through 0x01FF will be accessed.

19.3. SFR Page Stack Example

In this example, the SFR Control register is left in the default enabled state (SFRPGEN set to 1), and the core is executing in-line code that is writing values to Temperature Sensor Control Register (TS0CN). The device is also using the SPI peripheral (SPI0) and the Programmable Counter Array (PCA0) peripheral to generate a PWM output. The PCA is timing a critical control function in its interrupt service routine, therefore, its associated ISR is set to high priority. At this point, the SFR page is set to 0x0F to access the TS0CN SFR. See Figure 19.2.

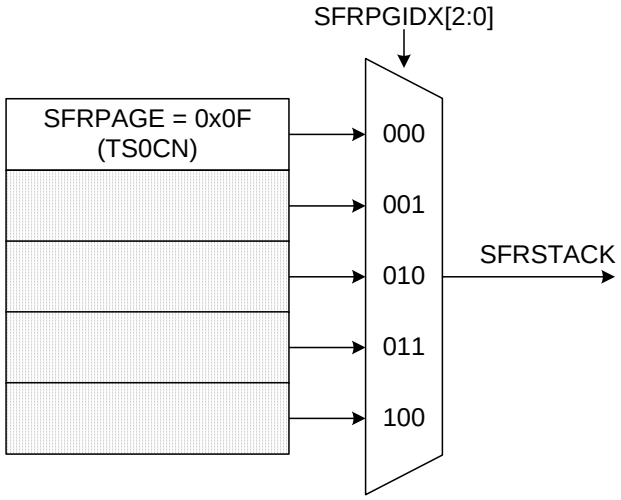

Figure 19.2. SFR Page Stack While Using SFR Page 0x0F To Access TS0CN

On the execution of the RETI instruction in the SPI0 ISR, the value in SFRPAGE register is overwritten with the contents at the SFRPGIDX = 001b location. The CIP-51 may now access the TS0CN register as it did prior to the interrupts occurring. See Figure 19.6.

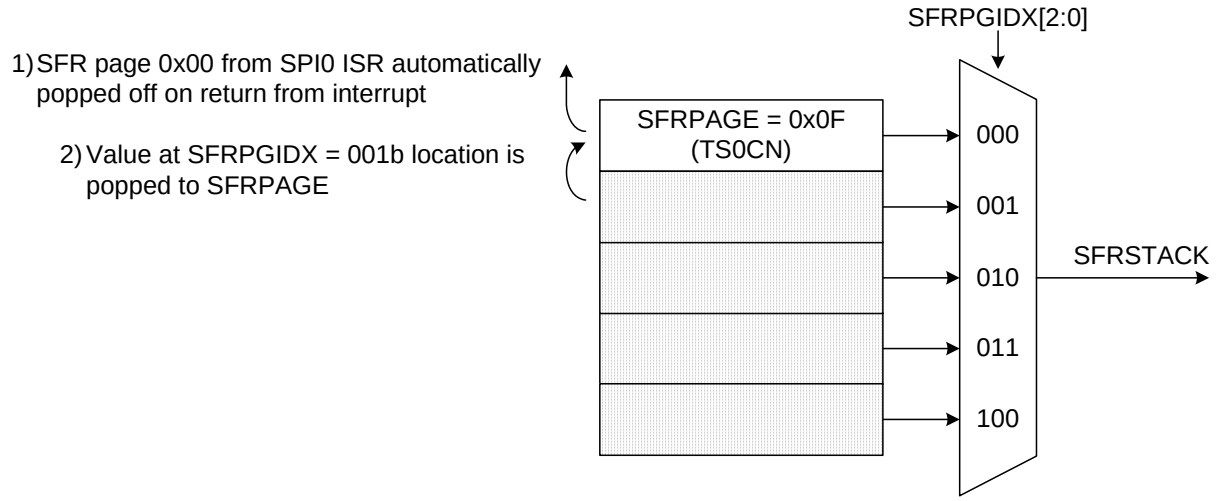

Figure 19.6. SFR Page Stack Upon Return From SPI0 Interrupt

Push operations on the SFR page stack only occur on interrupt service, and pop operations only occur on interrupt exit (execution on the RETI instruction). The automatic switching of the SFRPAGE and operation of the SFR page stack as described above can be disabled in software by clearing the SFR Automatic Page Enable Bit (SFRPGEN) in the SFR Page Control Register (SFRPGCN).

25.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the controller core to enter Stop mode as soon as the instruction that sets the bit completes execution. Before entering stop mode, the system clock must be sourced by the internal high-frequency oscillator. In stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering stop mode. Stop mode can only be terminated by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout.

By default, when in stop mode the internal regulator is still active. However, the regulator can be configured to shut down while in stop mode to save power. To shut down the regulator in stop mode, the STOPCF bit in register REG01CN should be set to 1 prior to setting the STOP bit (see SFR Definition 25.1). If the regulator is shut down using the STOPCF bit, only the $\overline{\text{RST}}$ pin or a full power cycle are capable of resetting the device.

25.3. Suspend Mode

Setting the SUSPEND bit (OSCICN.5) causes the hardware to halt the CPU and the high-frequency internal oscillator, and go into suspend mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. Most digital peripherals are not active in suspend mode. The exception to this is the Port Match feature and Timer 3, when it is run from an external oscillator source or the internal low-frequency oscillator.

Suspend mode can be terminated by four types of events, a port match (described in Section “27.5. Port Match” on page 183), a Timer 3 overflow (described in Section “31.3. Timer 3” on page 259), a Comparator low output (if enabled), or a device reset event. Note that in order to run Timer 3 in suspend mode, the timer must be configured to clock from either the external clock source or the internal low-frequency oscillator source. When suspend mode is terminated, the device will continue execution on the instruction following the one that set the SUSPEND bit. If the wake event (port match or Timer 3 overflow) was configured to generate an interrupt, the interrupt will be serviced upon waking the device. If suspend mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

SFR Definition 27.7. P0: Port 0

Bit	7	6	5	4	3	2	1	0
Name	P0[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0x80; SFR Page = All Pages; Bit Addressable

Bit	Name	Description	Write	Read
7:0	P0[7:0]	**Port 0 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P0.n Port pin is logic LOW. 1: P0.n Port pin is logic HIGH.

SFR Definition 27.8. P0MDIN: Port 0 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF1; SFR Page = All Pages

Bit	Name	Function
7:0	P0MDIN[7:0]	**Analog Configuration Bits for P0.7–P0.0 (respectively).** Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P0.n pin is configured for analog mode. 1: Corresponding P0.n pin is not configured for analog mode.

Table 28.1. SMBus Clock Source Selection

SMBnCS1	SMBnCS0	SMBus0 Clock Source	SMBus1 Clock Source
0	0	Timer 0 Overflow	Timer 0 Overflow
0	1	Timer 1 Overflow	Timer 5 Overflow
1	0	Timer 2 High Byte Overflow	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow	Timer 2 Low Byte Overflow

The SMBnCS1–0 bits select the SMBus clock source, which is used only when operating as a master or when the Free Timeout detection is enabled. When operating as a master, overflows from the selected source determine the absolute minimum SCL low and high times as defined in Equation 28.1.The selected clock source may be shared by other peripherals so long as the timer is left running at all times. For example, Timer 1 overflows may generate the SMBus0 and SMBus1 clock rates simultaneously. Timer configuration is covered in Section “31. Timers” on page 242.

$$T_{HighMin} = T_{LowMin} = \frac{1}{f_{ClockSourceOverflow}}$$

Equation 28.1. Minimum SCL High and Low Times

The selected clock source should be configured to establish the minimum SCL High and Low times as per Equation 28.1. When the interface is operating as a master (and SCL is not driven or extended by any other devices on the bus), the typical SMBus bit rate is approximated by Equation 28.2.

$$BitRate = \frac{f_{ClockSourceOverflow}}{3}$$

Equation 28.2. Typical SMBus Bit Rate

Figure 28.4 shows the typical SCL generation described by Equation 28.2. Notice that T_{HIGH} is typically twice as large as T_{LOW}. The actual SCL output may vary due to other devices on the bus (SCL may be extended low by slower slave devices, or driven low by contending master devices). The bit rate when operating as a master will never exceed the limits defined by equation Equation 28.1.

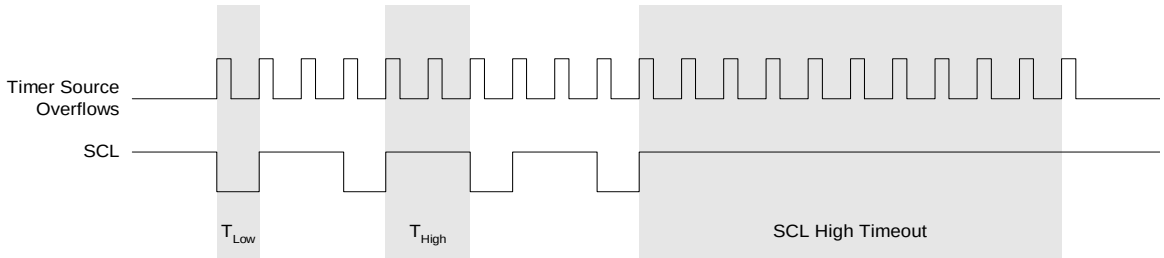

Figure 28.4. Typical SMBus SCL Generation

Setting the EXTHOLD bit extends the minimum setup and hold times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time that the current SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 28.2 shows the min-

SFR Definition 28.5. SMB1CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER1	TXMODE1	STA1	STO1	ACKRQ1	ARBLOST1	ACK1	SI1
Type	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC0; SFR Page = F; Bit-Addressable

Bit	Name	Description	Read	Write
7	MASTER1	**SMBus1 Master/Slave Indicator.** This read-only bit indicates when the SMBus1 is operating as a master.	0: SMBus1 operating in slave mode. 1: SMBus1 operating in master mode.	N/A
6	TXMODE1	**SMBus1 Transmit Mode Indicator.** This read-only bit indicates when the SMBus1 is operating as a transmitter.	0: SMBus1 in Receiver Mode. 1: SMBus1 in Transmitter Mode.	N/A
5	STA1	**SMBus1 Start Flag.**	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO1	**SMBus1 Stop Flag.**	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmitted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ1	**SMBus1 Acknowledge Request.**	0: No ACK requested 1: ACK requested	N/A
2	ARBLOST1	**SMBus1 Arbitration Lost Indicator.**	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK1	**SMBus1 Acknowledge.**	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SI1	**SMBus1 Interrupt Flag.** This bit is set by hardware under the conditions listed in Table 28.3. SI1 must be cleared by software. While SI1 is set, SCL1 is held low and the SMBus1 is stalled.	0: No interrupt pending 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event. 1: Force interrupt.

Table 29.1. Timer Settings for Standard Baud Rates Using The Internal 49 MHz Oscillator

	Frequency: 49 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)[1]	T1M[1]	Timer 1 Reload Value (hex)
SYSCLK from Internal Osc.	230400	–0.32%	212	SYSCLK	XX[2]	1	0x96
	115200	0.15%	426	SYSCLK	XX	1	0x2B
	57600	–0.32%	848	SYSCLK/4	01	0	0x96
	28800	0.15%	1704	SYSCLK/12	00	0	0xB9
	9600	–0.32%	5088	SYSCLK/48	00	0	0xCB
	2400	0.15%	20448	SYSCLK/48	10	0	0x2B

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 31.1.
2. X = Don't care.

Table 29.2. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator

	Frequency: 22.1184 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)[1]	T1M[1]	Timer 1 Reload Value (hex)
SYSCLK from External Osc.	230400	0.00%	96	SYSCLK	XX[2]	1	0xD0
	115200	0.00%	192	SYSCLK	XX	1	0xA0
	57600	0.00%	384	SYSCLK	XX	1	0x40
	28800	0.00%	768	SYSCLK / 12	00	0	0xE0
	14400	0.00%	1536	SYSCLK / 12	00	0	0xC0
	9600	0.00%	2304	SYSCLK / 12	00	0	0xA0
	2400	0.00%	9216	SYSCLK / 48	10	0	0xA0
	1200	0.00%	18432	SYSCLK / 48	10	0	0x40
SYSCLK from Internal Osc.	230400	0.00%	96	EXTCLK / 8	11	0	0xFA
	115200	0.00%	192	EXTCLK / 8	11	0	0xF4
	57600	0.00%	384	EXTCLK / 8	11	0	0xE8
	28800	0.00%	768	EXTCLK / 8	11	0	0xD0
	14400	0.00%	1536	EXTCLK / 8	11	0	0xA0
	9600	0.00%	2304	EXTCLK / 8	11	0	0x70

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 31.1.
2. X = Don't care.

31.5. Timer 5

Timer 5 is a 16-bit timer formed by two 8-bit SFRs: TMR5L (low byte) and TMR5H (high byte). Timer 5 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T5SPLIT bit (TMR5CN.3) defines

Timer 5 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. Note that the external oscillator source divided by 8 is synchronized with the system clock.

31.5.1. 16-bit Timer with Auto-Reload

When T5SPLIT (TMR5CN.3) is zero, Timer 5 operates as a 16-bit timer with auto-reload. Timer 5 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 5 reload registers (TMR5RLH and TMR5RLL) is loaded into the Timer 5 register as shown in Figure 31.12, and the Timer 5 High Byte Overflow Flag (TMR5CN.7) is set. If Timer 5 interrupts are enabled (if EIE1.7 is set), an interrupt will be generated on each Timer 5 overflow. Additionally, if Timer 5 interrupts are enabled and the TF5LEN bit is set (TMR5CN.5), an interrupt will be generated each time the lower 8 bits (TMR5L) overflow from 0xFF to 0x00.

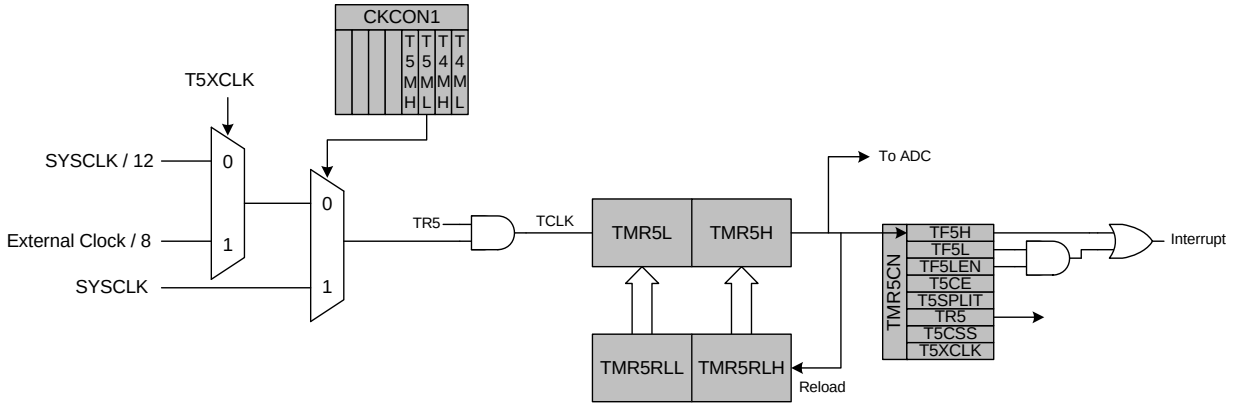

Figure 31.12. Timer 5 16-Bit Mode Block Diagram

32.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

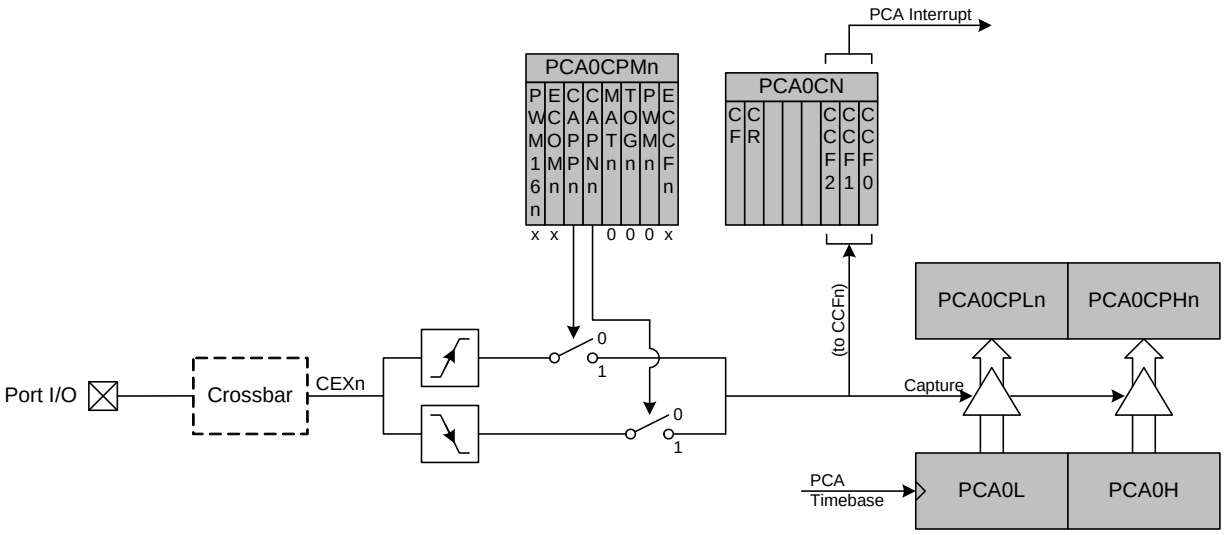

Figure 32.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

SFR Definition 32.4. PCA0CLR: PCA Comparator Clear Control

Bit	7	6	5	4	3	2	1	0
Name	CPCPOL					CPCE2	CPCE1	CPCE0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCE; SFR Page = All Pages

Bit	Name	Function
7	CPCPOL	**Comparator Clear Polarity.** Selects the polarity of the comparator result that will clear the PCA channel(s). 0: PCA channel(s) will be cleared when comparator result goes logic low 1: PCA channel(s) will be cleared when comparator result goes logic high
6:3	Reserved	Must write 0000b.
2	CPCE2	**Comparator Clear Enable for CEX2.** Enables the comparator clear function on PCA channel 2.
1	CPCE1	**Comparator Clear Enable for CEX1.** Enables the comparator clear function on PCA channel 1.
0	CPCE0	**Comparator Clear Enable for CEX0.** Enables the comparator clear function on PCA channel 0.