Rohm Semiconductor - ML620Q504H-NNNTBWBX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	nX-U16/100
Core Size	16-Bit
Speed	16.8MHz
Connectivity	I²C, SSP, UART/USART
Peripherals	Melody Driver, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 16
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml620q504h-nnntbwbx

- Successive approximation type A/D converter (SA-ADC)
  - Input × 12 channels
  - 12-bit A/D converter
  - Starting by trigger of Timer/FTM function.
  - Capacitive touch sense function

- Analog Comparator (CMP)
  - Input × 2ch
  - Common mode input voltage: 0.2V to V_{DD}−0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection are selectable

- Voltage Level Supervisor (VLS)
  - Threshold voltages: selectable from 13 levels
  - interrupt or reset generate are selectable

- Low Level Detector(LLD)
  - Judgement Voltage: 1.8V±0.2V
  - Usable as low level detection reset

- Reset
  - Reset by the RESET_N pin
  - Reset by power-on detection
  - Reset by overflow of watchdog timer (WDT)
  - Reset by Voltage Leve Supervisor(VLS)
  - Reset by Low Level Detector(LLD)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
    - Crystal oscillation (32.768 kHz)
    - External clock input (30kHz to 36kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - Crystal/Ceramic oscillation (16 MHz)
    - External clock input (300kHz to 16 MHz)
    - Built-in RC oscillation (16MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states.
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTB, etc.) can keep in operating states.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

BLOCK DIAGRAM

Block Diagram of ML620Q503H/Q504H

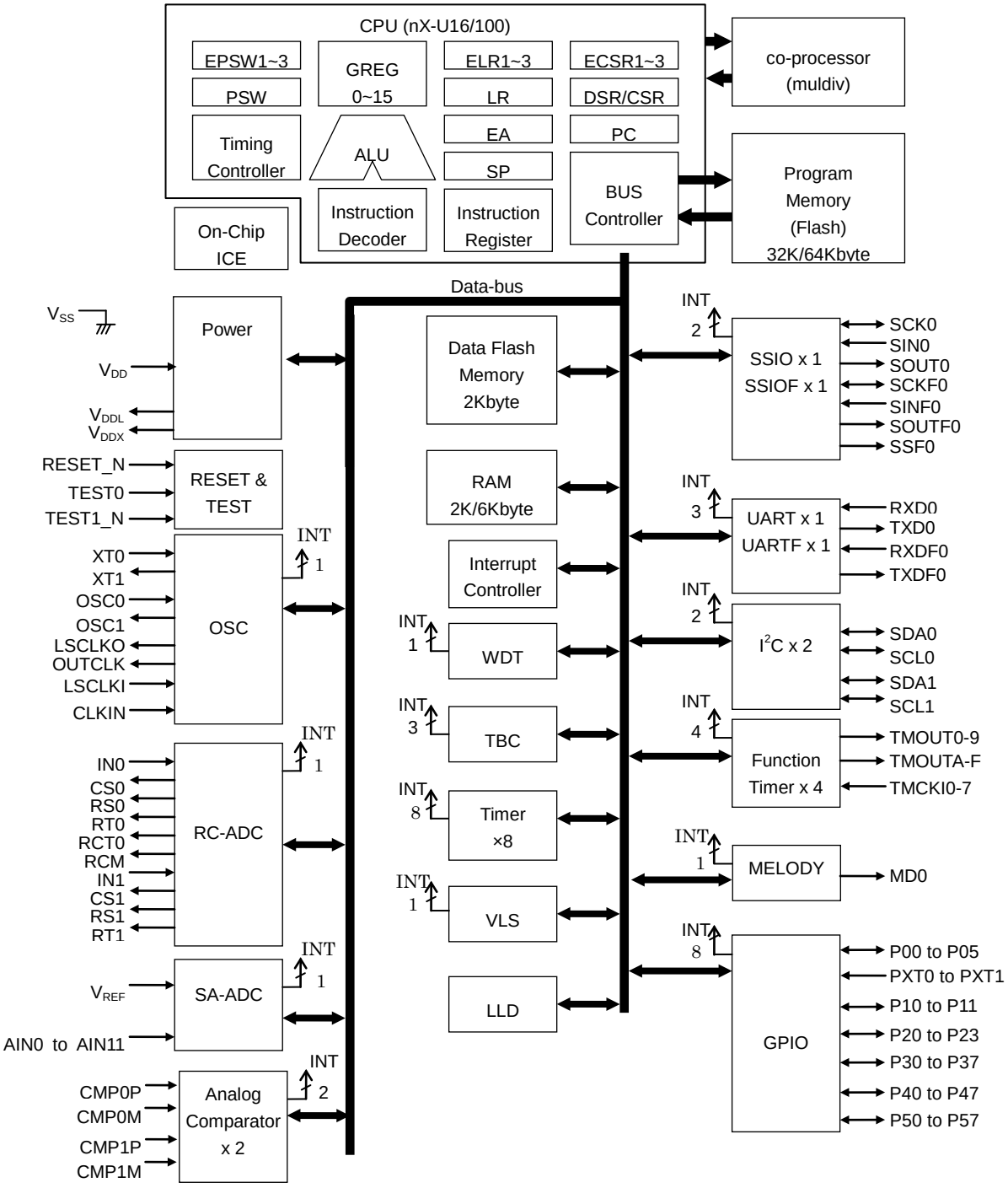


Figure 1. Block Diagram of ML620Q503H/Q504H

PKG Pin No.	1st Function				2nd/3rd/4th Function								
	Pin name	I/O	Reset State	Function	pin name	I/O	function	pin name	I/O	function	pin name	I/O	function
37	P54/ EXI54	I/O	Hi-Z output	Input-Output port/ External interrupt	SDA1	I/O	I^2C data input/output	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
38	P55/ EXI55	I/O	Hi-Z output	Input-Output port/ External interrupt	SCL1	O	I^2C clock output	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
39	P56/ EXI56/ TMCKI6	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	LSCLKO	O	Low-speed clock output	SCKF0	I/O	SSIOF clock input/output	TMOUTE	O	FTM output
40	P57/ EXI57/ TMCKI7	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	OUTCLK	O	High-speed clock output	SSF0	I/O	SSIOF select input/output	TMOUTF	O	FTM output

PIN DESCRIPTION

The pin name represents the function pin name of the primary function of each terminal, The pin mode represents the set of mode register of Port Control.
(1st:primary function, 2nd:secondary function, 3rd: tertiary function, 4th: quartic function)

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
System					
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	RESET_N	—	L
XT0	I	Crystal connection pin for low-speed clock. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS} as required.	PXT0	1st	—
XT1	O		PXT1	1st	—
LSCLKI	I	External clock input for Low-speed clock.	PXT1	1st	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock (16 MHz max.). Capacitors C_{DH} and C_{GH} are connected across this pin and V_{SS}.	P10	1st	—
OSC1	O		P11	1st	—
CLKIN	I	External clock input for High-speed clock.	P11	1st	—
LSCLKO	O	Low-speed clock output pin.	P46,P56	2nd	—
OUTCLK	O	High-speed clock output pin.	P47,P57	2nd	—
General-purpose input/output port					
PXT0-PXT1	I	General-purpose input port(without pull-up/pull-down resister).	PXT0-PXT1	1st	—
P00-P05	I/O	General-purpose input/output port.	P00-P05	1st	—
P10-P11	I/O	General-purpose input/output port.	P10-P11	1st	—
P20-P23	I/O	General-purpose input/output port.	P20-P23	1st	—
P30-P37	I/O	General-purpose input/output port.	P30-P37	1st	—
P40-P47	I/O	General-purpose input/output port.	P40-P47	1st	—
P50-P57	I/O	General-purpose input/output port.	P50-P57	1st	—
External interrupt					
EXII0-EXII1 EXI00-05 EXI20-23 EXI30-37 EXI40-47 EXI50-57	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software.	PXT0-PXT1 P00-P05 P20-P23 P30-P37 P40-P47 P50-P57	1st	H/L
LED					
LED	O	N-channel open drain output pins to drive LED.	P40,P41,P52,P53	1st	—
Melody/Buzzer					
MD0	—	Melody/buzzer signal output pin.	P33,P43,P53	2nd	H
UART					
TXD0	O	UART0 data output pin.	P01,P31,P41,P51	4th	—
RXD0	I	UART0 data input pin.	P00,P30,P40,P50	4th	—
TXDF0	O	UART with FIFO data output pin.	P21,P35,P45,P55	4th	—
RXDF0	I	UART with FIFO data input pin.	P20,P34,P44,P54	4th	—

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
Successive approximation type A/D converter					
V_{REF}	I	Reference voltage input pin for successive approximation type A/D converter.	V_{REF}	—	—
AIN0-11	I	Channel 0 analog input for successive approximation type A/D converter.	P34,P35,P36,P37, P20,P21,P22,P23, P00,P01,P02,P03	1st	—
Analog comparator					
CMP0P	I	Comparator0 Non-inverted input pin.	P30	1st	—
CMP0M	I	Comparator0 Inverted input pin.	P31	1st	—
CMP1P	I	Comparator1 Non-inverted input pin.	P32	1st	—
CMP1M	I	Comparator1 Inverted input pin.	P33	1st	—
For testing					
TEST0	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	TEST0	—	—
TEST1_N	I	Input pin for testing. A pull-up resistor is internally connected.	TEST1_N	—	—
Power supply					
V_{SS}	—	Negative power supply pin.	V_{SS}	—	—
V_{DD}	—	Positive power supply pin.	V_{DD}	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors C_{L0} and C_{L1} are connected between this pin and V_{SS}.	V_{DDL}	—	—
V_{DDX}	—	Positive power supply pin (internally generated) for low-speed oscillation. Capacitor C_{X1} is connected between this pin and V_{SS}.	V_{DDX}	—	—

Recommended Operating Conditions

(V_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambience)	T_{OP}	—	-40 to +85	°C
Operating voltage	V_{DD}	—	1.8 to 5.5	V
Reference voltage	V_{REF}	—	1.8 to V_{DD}	V
Operating frequency （CPU）	f_{OP}	—	30k to 16.8M	Hz
Low-speed external clock input	f_{EXTL}	—	30k to 36k	Hz
High-speed external clock input	f_{EXTH}	—	2M to 16M	Hz
Low speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low speed crystal oscillation external capacitor 1	C_{DL}	Using VT-200-FL(from SII）	6.8 to 12	pF
	C_{GL}		6.8 to 12	
Low speed crystal oscillation external capacitor 2	C_{DL}	Using DT-26(from Daishinku)	12 to 16	pF
	C_{GL}		12 to 16	
Low speed crystal *1 oscillation external capacitor 3	C_{DL}	Using VT-200-F(from SII）	12 to 22	pF
	C_{GL}		12 to 22	
High speed Crystal/ Ceramic oscillation frequency	f_{XTH}	—	16M	Hz
High speed crystal oscillation external capacitor	C_{DH}	Using NX8045GB (from Nihon Denpa Kogyo)	12 to 20	pF
	C_{GH}		12 to 20	
Ceramic oscillation External capacitor	C_{DH}	Using FCSTCE16M0V53 (from Murata manufacturing) Build in CL type	0 to 5	pF
	C_{GH}		0 to 5	
V_{DDL} external capacitor *2	C_L	ESR ≦ 500mΩ	2.2 ± 30%	μF
V_{DDX} external capacitor	C_X	—	0.33 ± 30%	μF

*1：Please use this crystal except DEEPHALT mode because this LSI may not be functioning at DEEPHALT mode with the crystal. Please evaluate the matching when other crystal oscillator/ ceramic oscillator is used.

*2：Please evaluate on user's conditions, put on C_{L0}(= 0.1uF) if necessary.

Operating Conditions of Flash Memory

(V_{SS}= 0V)

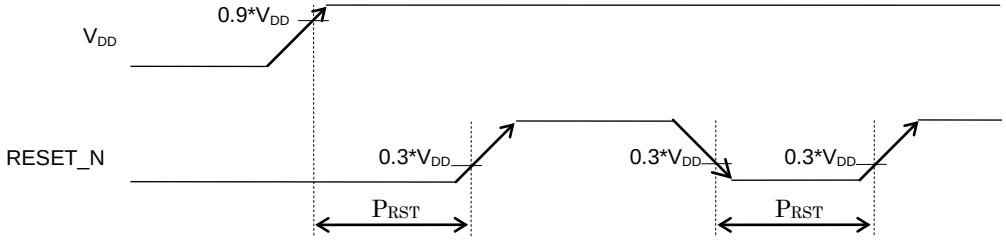
Parameter	Symbol	Condition		Range	Unit
Operating temperature (Ambience)	T_{OP}	Data area : write/erase		-40 to +85	°C
		Program area : write/erase		0 to +40	°C
Operating voltage Write time	V_{DD}	Write/erase		1.8 to 5.5	V
	C_{EPD}	Data area (1,024B x 2)		10,000	times
	C_{EPP}	Program area		100	times
Erase unit	—	Block erase	Program area	8	KB
			Data area	2	
		Sector erase		1	KB
Erase time(Maximum)	—	Block erase/Sector erase		100	ms
Write unit	—	—		1 word (2 byte)	—

AC characteristics (Oscillation, reset)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C , unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Low speed crystal oscillation start time	T_{XTL}	—	—	—	2	s	
High speed crystal oscillation start time	T_{XTH}	—	—	—	20	ms	
Low speed built-in RC oscillation frequency*1*2	f_{LCR}	Ta=25°C	typ -1.5%	32.768	typ +1.5%	kHz	
		Ta=-40 ~ 85°C	typ -5%	32.768	typ +5%		
High speed build-in RC oscillation frequency*1*2	f_{HCR}	Ta=25°C	typ -1%	16	typ +1%	MHz	1
		Ta=-40 to 85°C	typ -5%	16	typ +5%		
Reset pulse width	P_{RST}	—	200	—	—	us	
Reset noise elimination pulse width	P_{NRST}	—	—	—	0.3	us	
Power-on reset activation power rise time	T_{POR}	–	–	–	10	ms	

*1 : Mean value of 1024 cycle.
*2 : Guarantee value at the time of the shipment.



External reset sequence

Power on reset sequence

DC Characteristics (VLS)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating*1			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS judge voltage (V_{DD}=fall)	V_{VLS}	vlscon = 3H	1.798	1.898	1.998	V	1
		vlscon = 4H	1.900	2.000	2.100		
		vlscon = 5H	1.993	2.093	2.193		
		vlscon = 6H	2.096	2.196	2.296		
		vlscon = 7H	2.209	2.309	2.409		
		vlscon = 8H	2.309	2.409	2.509		
		vlscon = 9H	2.505	2.605	2.705		
		vlscon = AH	2.700	2.800	2.900		
		vlscon = BH	2.968	3.068	3.168		
		vlscon = CH	3.294	3.394	3.494		
		vlscon = DH	3.697	3.797	3.897		
		vlscon = EH	4.126	4.226	4.326		
		vlscon = FH	4.567	4.667	4.767		
V_{VLS} Hysteresis width (V_{DD}=rise)	H_{VLS}	−	V_{VLS} x 1.8%	V_{VLS} x 3.8%	V_{VLS} x 6.3%	V	

DC characteristics (LLD)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
LLD judge Voltage	VLLR	—	1.60	1.80	2.00	V	1

DC characteristics (Analog comparator)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Common input voltage range	V_{CMPIN}	—	0.2	—	V_{DD} -0.2	V	1
Input offset voltage	V_{CMPOF}	—	-30	—	30	mV	
Comparator judge time	T_{CMP}	CMPP- CMPM =40mV	—	—	2	μs	

DC characteristics (IIHL)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating*1			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-900	-300	-20		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	20	300	900		
	IIL2	VIL2=V_{SS}	-1	—	—		
Input current 3 (PXT0-PXT1, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57)	IIH3	VIH3=V_{DD} (at pull down)	1	15	200		
	IIL3	VIL3=V_{SS} (at pull up)	-200	-15	-1		
	IIH3Z	VIH3=V_{DD} (at high impedance)	—	—	1		
	IIL3Z	VIL3=V_{SS} (at high impedance)	-1	—	—		
Input current 4 (P10-P11)	IIH4	VIH4=V_{DD} (at pull down)	1	15	200		
	IIL4	VIL4=V_{SS} (at pull up)	-200	-15	-1		
	IIH4Z	VIH4=V_{DD} (at high impedance)	—	—	2		
	IIL4Z	VIL4=V_{SS} (at high impedance)	-2	—	—		

*1 : typ.rating is Ta=25°C , V_{DD}=3.0V

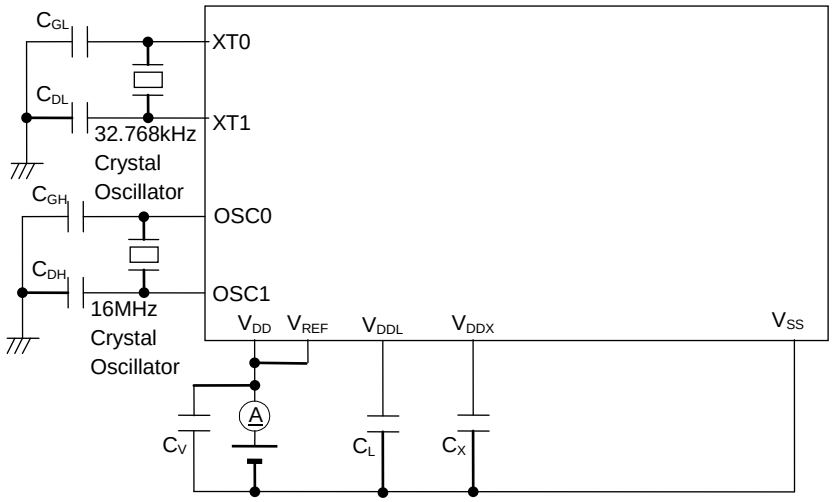
DC characteristics (VIHL)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N, TEST0, TEST1_N, PXT0-PXT1, P00-P05, P10-P11, P20-P23, P30-P37, P40-P47, P50-P57)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3 ×V_{DD}		
Input terminal capacitance (RESET_N, TEST0, TEST1_N, PXT0-PXT1,, P00-P05, P10-P11, P20-P23, P30-P37, P40-P47, P50-P57)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	10	pF	—

Measuring circuit

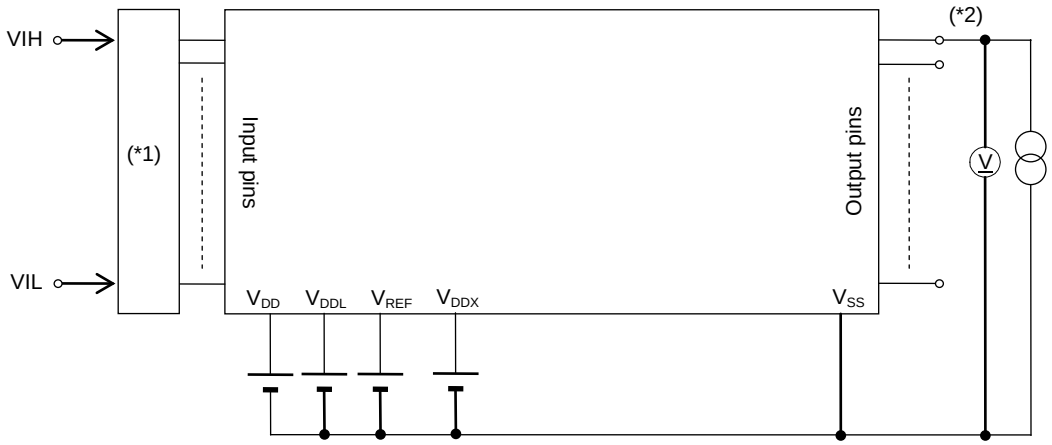
Measuring circuit 1



C_V	:	1.0µF
C_L	:	2.2µF
C_X	:	0.33µF
C_{GL}	:	12pF
C_{DL}	:	12pF
C_{GH}	:	16pF
C_{DH}	:	16pF

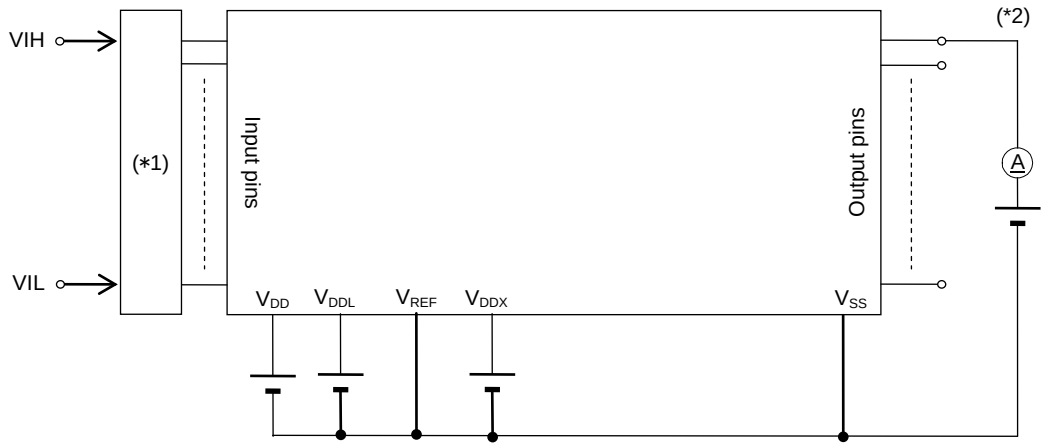
32.768kHz crystal oscillator : DT-26 (from Daishinku)
16MHz crystal oscillator : NX8045GB (from Nihon denpa kogyo)

Measuring circuit 2



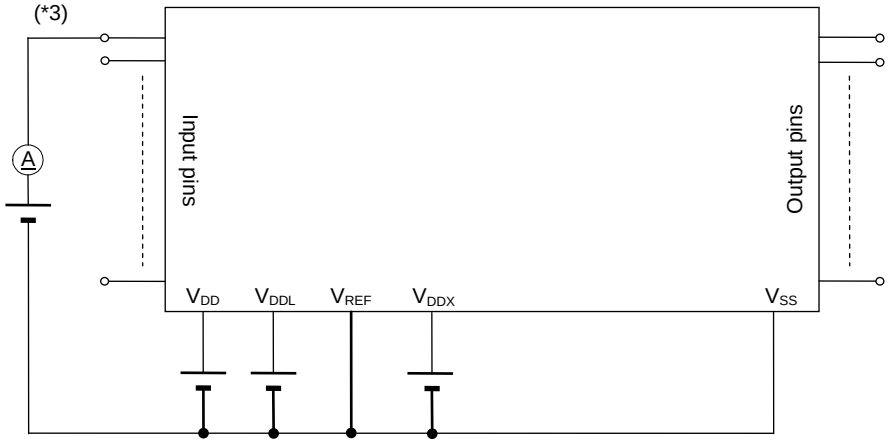
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 3



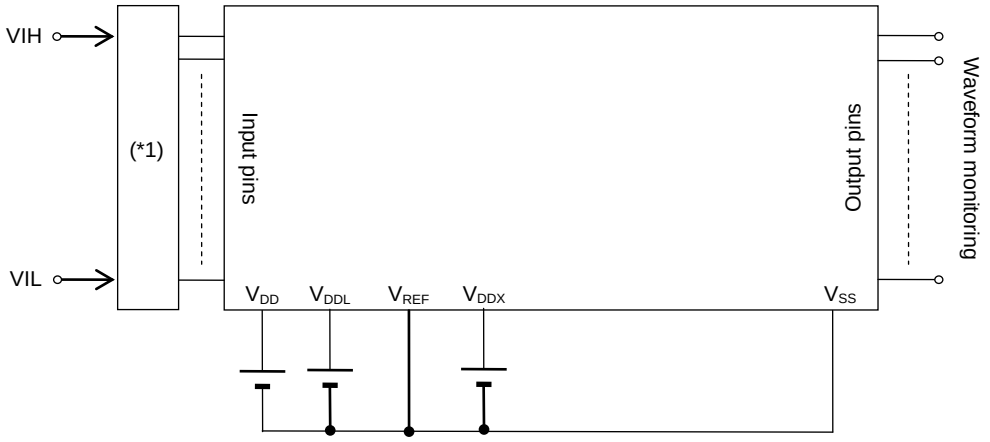
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 4



(*3) Measured at the specified output pins.

Measuring circuit 5



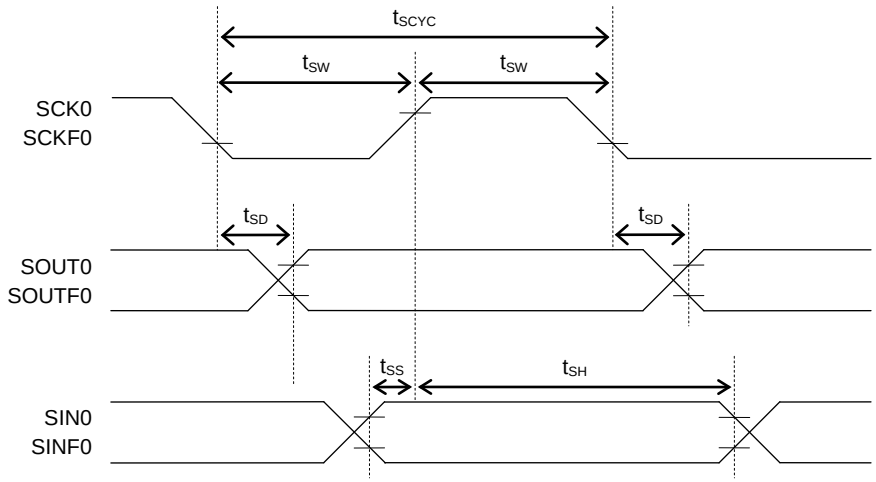
(*1) Input logic circuit to determine the specified measuring conditions.

AC characteristics (synchronous serial port)

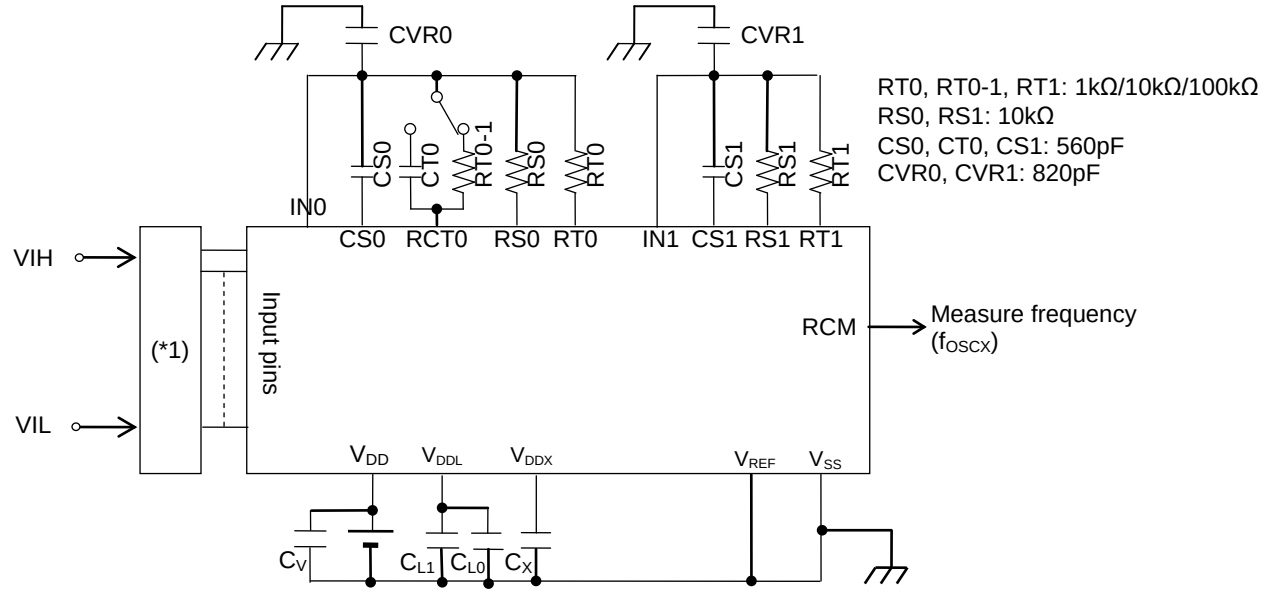
(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation is not active	10	—	—	µs
		High speed oscillation is active	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK*[1]	—	s
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation is not active	4	—	—	µs
		High speed oscillation is active	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input Setup time (slave mode)	t_{SS}	—	50	—	—	ns
SINinput Hold time	t_{SH}	—	50	—	—	ns

*1 : The clock period which is selected by the below registers(min:250ns@reguraly, min:500ns@P02, P22 is used)
In case of SSIO : S0CK2-0 of serial port 0 mode register(SIO0MOD).
In case of SSIOF : SF0BR9-0 of SIOF0 port register(SF0BRR)



Measuring circuit



(*1) Input logic circuit to determine the specified measuring conditions.

【Note】

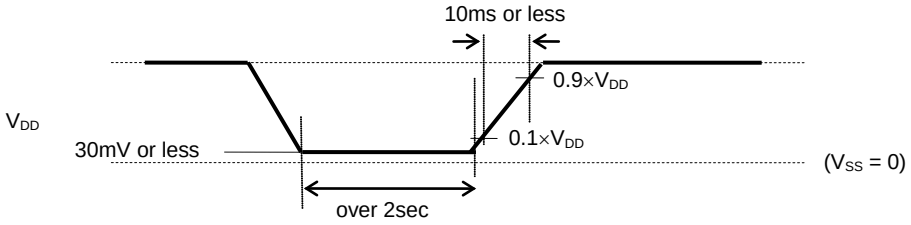
・Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

・When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please shield the signal by V_{SS}(GND) .

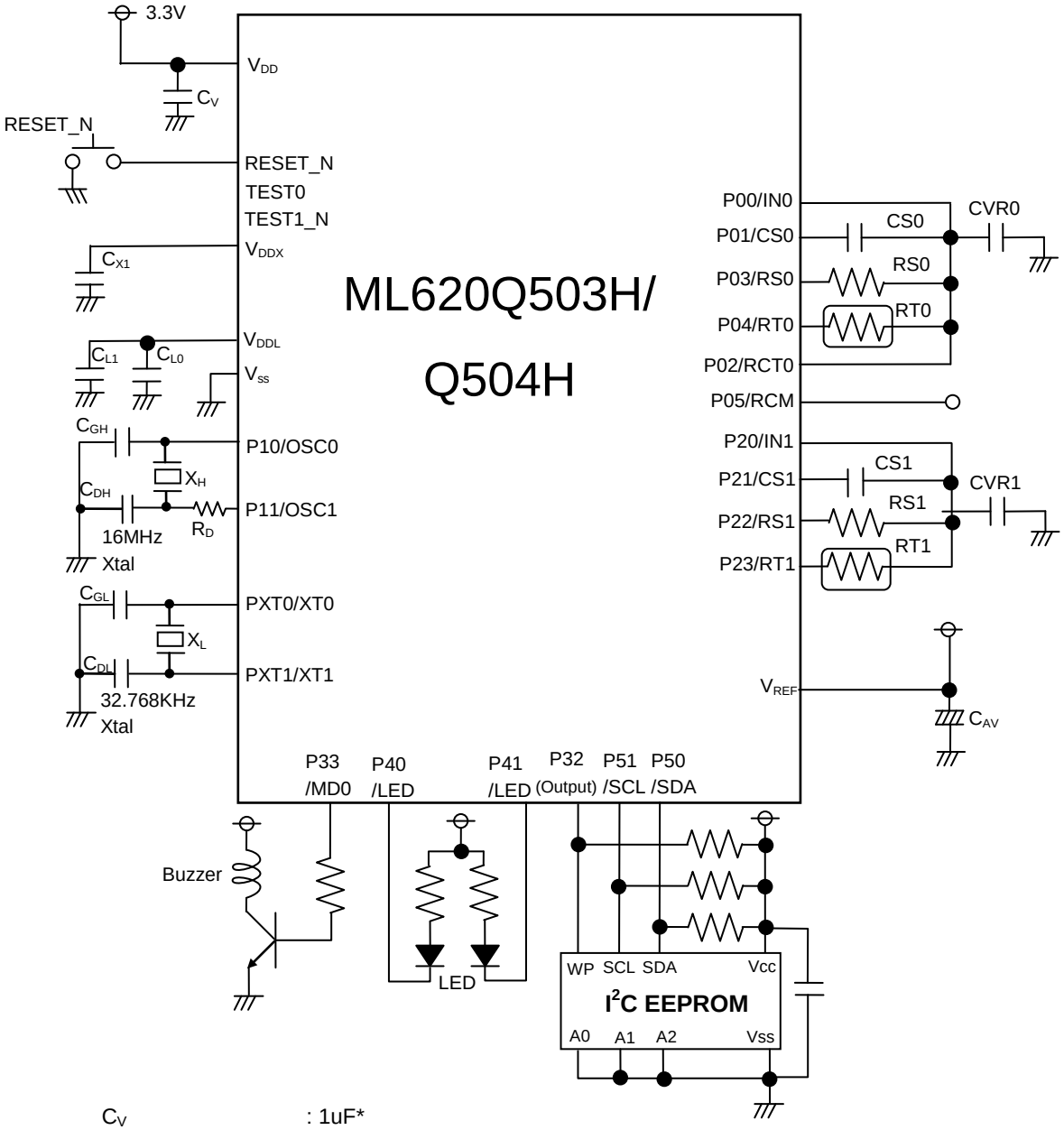
・Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Power-on and shutdown Procedures

In case of power-on or shutdown of V_{DD}, the procedures and constraints are shown as following.



APPLICATION CIRCUIT EXAMPLE

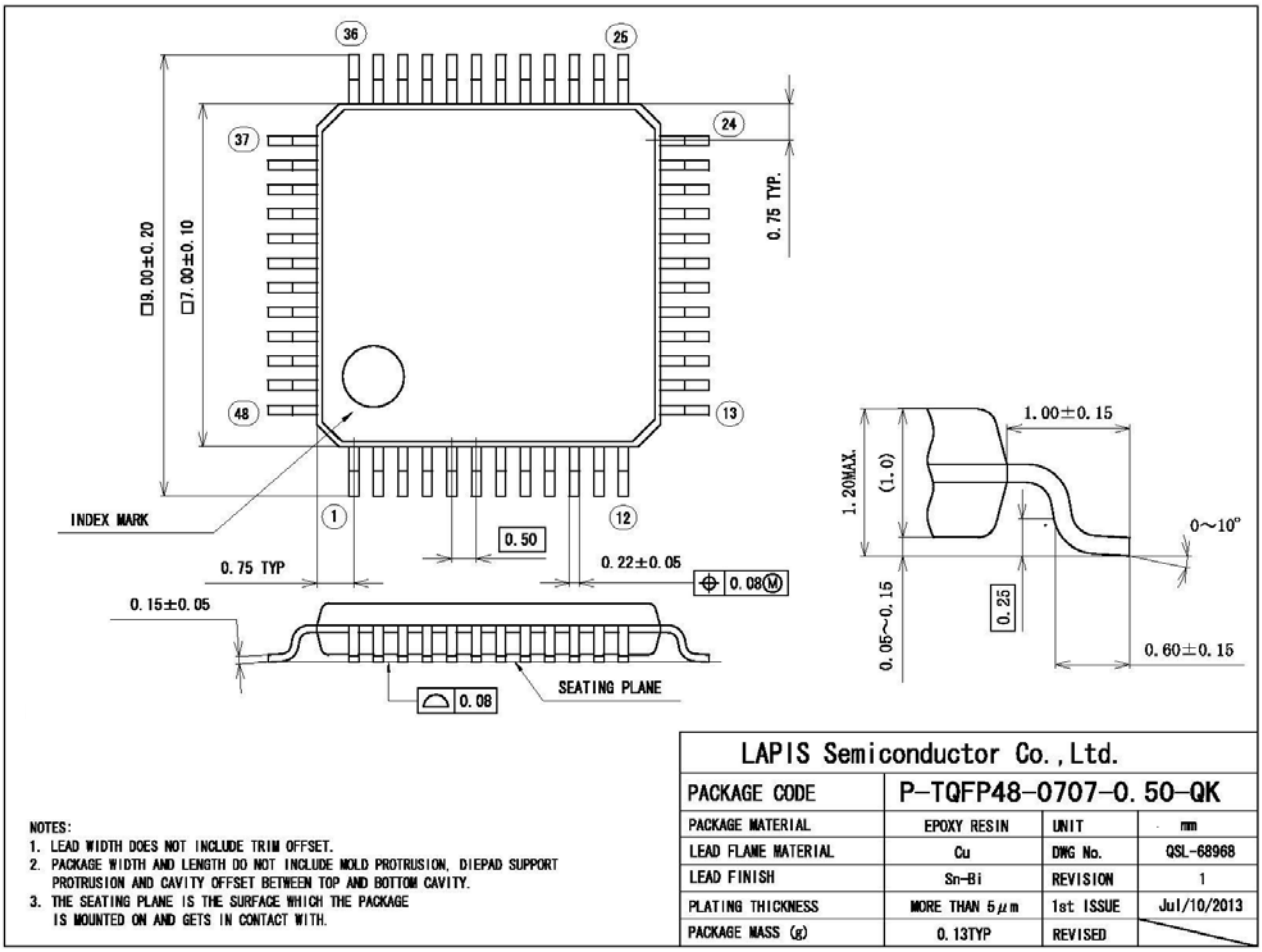


C_V	: 1uF*		
C_{L1}	: 2.2uF	C_{L0}	: open*
C_{X1}	: 0.33uF		
C_{GL}	: 12~16pF*	C_{DL}	: 12~16pF*
C_{GH}	: 12~20pF*	C_{DH}	: 12~20pF*
R_D	: 0Ω*		
C_{AV}	: 1uF*	RS0, RS1	: 10 KΩ
CS0, CS1	: 560 pF	CVR0, CVR1	: 820 pF
RT0, RT1	: Thermistor (103AT/Semitec)		
X_H	: NX8045GB/16.000MHz, Nihon Denpa Kogyo		
X_L	: DT-26, Daishinku		

*: Make a decision the parameters after evaluating on an user's conditions when designing circuits for mass production.

PACKAGE DIMENSIONS

ML620Q503H/Q504H Package Dimensions



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-QK		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu	DWG No.	QSL-68968
LEAD FINISH	Sn-Bi	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/10/2013
PACKAGE MASS (g)	0.13TYP	REVISED	

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions(reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL620Q504H-01	Aug.31.2015	–	–	Final Edition issued

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